A89307

Automotive FOC BLDC Motor Controller

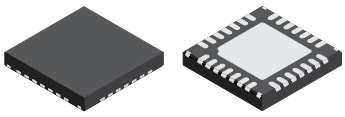
FEATURES AND BENEFITS

- Code-free sensorless field-oriented control (FOC)
- Constant speed, constant torque, constant power, and open-loop operating modes
- I²C interface for speed control and status readback
- Programmable, flexible in-to-output transformer
- Ultra-quiet low speed operation
- Proprietary non-reverse fast startup
- Soft-On Soft-Off (SOSO) for quiet operation
- Analog / PWM / Clock mode speed control
- Closed-loop speed control
- Configurable current limit
- Windmill startup operation
- Lock detection
- Short-circuit protection (OCP)
- Brake and direction inputs
- Adjustable gate drive
- Automotive AEC-Q100 qualified

APPLICATIONS

- Battery cooling fan
- Radiator fan
- Fuel, oil pump

PACKAGE



Not to scale

28-contact QFN
with exposed thermal pad
and wettable flank
5 mm × 5 mm × 0.90 mm
(ET package)

DESCRIPTION

The A89307 is a 3-phase, sensorless, brushless DC (BLDC) motor driver (gate driver) which can operate from 5.5 to 50 V.

A field-oriented control (FOC) algorithm is fully integrated to achieve the best efficiency and acoustic noise performance. Constant torque and constant power mode are provided as well as constant speed and open-loop operating modes.

The device also optimizes the motor startup performance in a stationary condition, a windmill condition, and even in a reverse windmill condition.

Motor speed is controlled through analog, PWM, or CLOCK input. Closed-loop speed control is optional, and RPM-to-clock frequency ratio is programmable.

A simple I²C interface is provided for setting motor-rated voltage, rated current, rated speed, resistance, and startup profiles. The I²C interface is also used for on/off control, speed control, and speed readback.

The A89307 is available in a 28-contact 5 mm × 5 mm QFN with exposed thermal pad (suffix ET) and wettable flank. The package is lead (Pb) free, with 100% matte-tin leadframe plating.

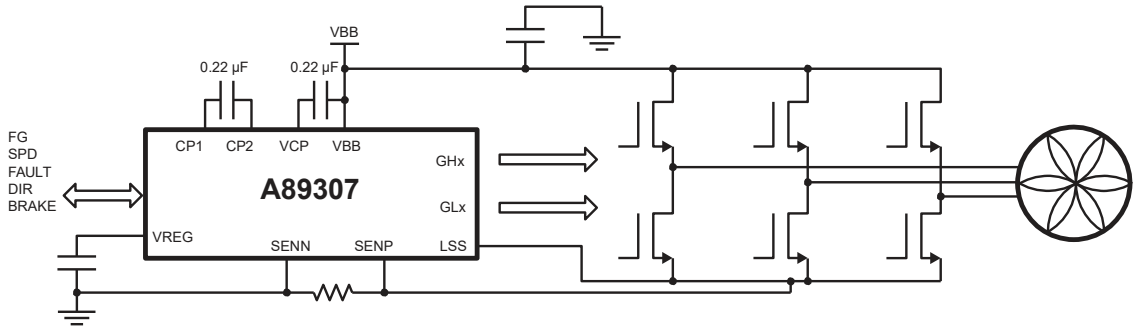


Figure 1: Typical Application – Functional Block Diagram

SELECTION GUIDE

Part Number	Packaging	Packing
A89307KETSR-J	28-contact QFN with exposed thermal pad and wettable flank	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		50	V
Logic Input Voltage Range	V_{IN}	SPD, BRAKE, DIR	–0.3 to 6	V
Logic Output	V_O	FG, FAULT (I < 5 mA)	6	V
LSS	V_{LSS}	DC	±500	mV
		t_W < 500 ns	±4	V
VREG	V_{REG}		–0.3 to 4	V
SENN, SENP	V_{SENN}, V_{SENP}	DC	±500	mV
		t_W < 500 ns	±4	V
Output Voltage	V_{OUT}	SA, SB, SC	–2 to V_{BB} + 2	V
		SA, SB, SC, t_W < 50 ns	–4 to V_{BB} + 4	V
GHx	V_{GHx}		V_{Sx} – 0.3 to V_{CP} + 0.3	V
GLx	V_{GLx}		V_{LSS} – 0.3 to 8.5	V
VCP	V_{CP}		V_{BB} – 0.3 to V_{BB} + 8	V
CP1	V_{CP1}		–0.3 to V_{BB} + 0.3	V
CP2	V_{CP2}		V_{BB} – 0.3 to V_{CP} + 0.3	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	28-contact QFN (package ET), on 2-sided PCB 1-in.^{2} copper	40	°C/W

*Additional thermal information available on the Allegro website.

Table of Contents

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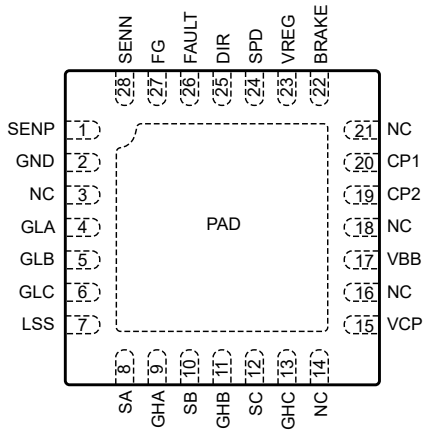
TERMINAL DIAGRAM AND LIST



ET Package Terminals

Terminal List

Name	Function	Number
BRAKE	Logic input	22
CP1	Charge pump	20
CP2	Charge pump	19
DIR	Direction control	25
FAULT	Fault indicator output	26
FG	Motor speed output	27
GHA	High-side gate drive output	9
GHB	High-side gate drive output	11
GHC	High-side gate drive output	13
GLA	Low-side gate drive output	4
GLB	Low-side gate drive output	5
GLC	Low-side gate drive output	6
GND	Ground	2
LSS	Low-side source	7
NC	No connect	3, 14, 16, 18, 21
SA	Motor output	8
SB	Motor output	10
SC	Motor output	12
SENN	Current sense negative terminal	28
SENP	Current sense positive terminal	1
SPD	PWM or clock mode speed control	24
VBB	Power supply	17
VCP	Charge pump	15
VREG	2.8 V regulator voltage	23
PAD	Exposed pad for enhanced thermal dissipation	PAD

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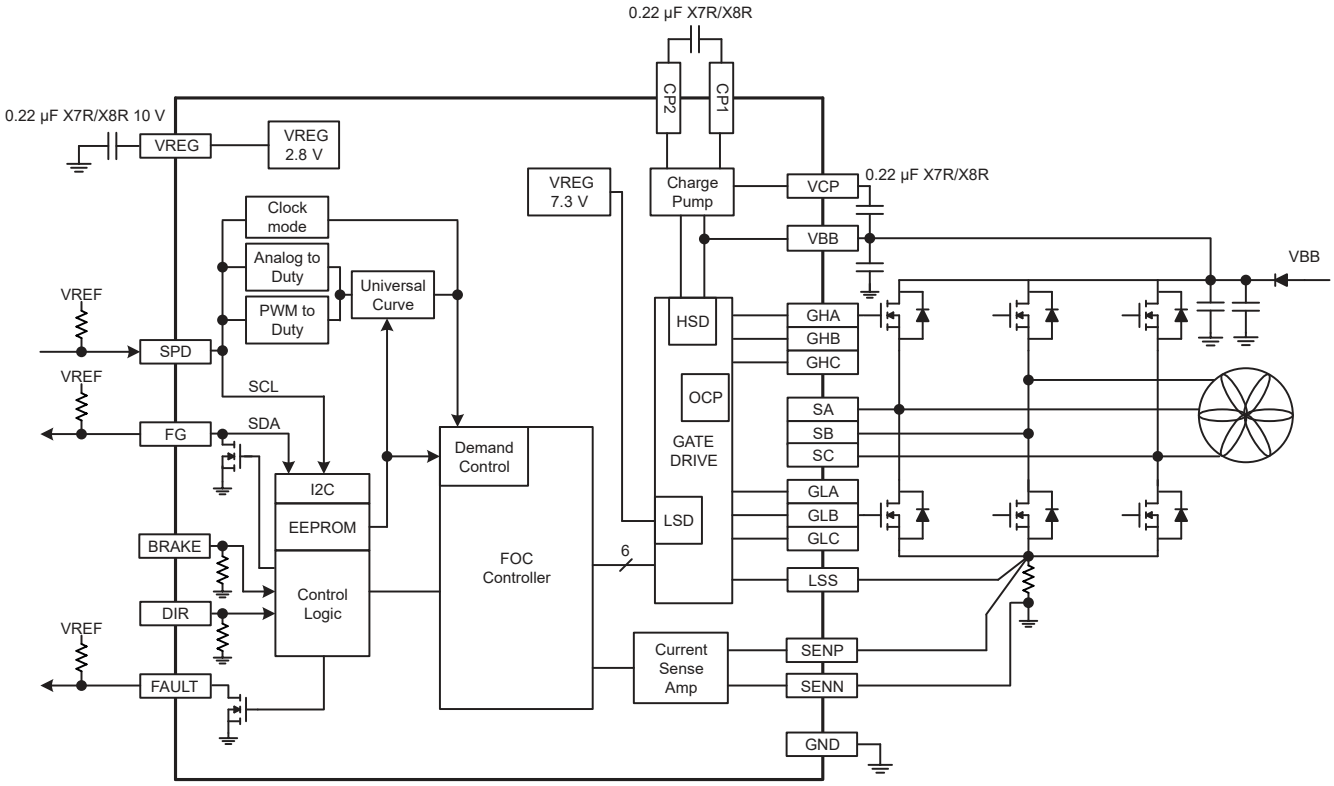
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40 to 125°C, V_{BB} = 5.5 to 28 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
Supply Voltage Range	V_{BB}	Driving	5.5	–	48	V
		Operating	5.5	–	50	V
VBB Supply Current	I_{BB}	I_{VREG} = 0 mA	–	8	12	mA
		Standby mode	–	10	20	µA
Reference Voltage	V_{REG}	I_{OUT} = 10 mA	2.70	2.86	2.95	V
VREG Current Limit	$I_{VREGOCL}$	V_{REG} = 0 V	25	50	127	mA
Charge Pump [2]	V_{CP}	V_{BB} = 8 V, I_{CPAVG} = 4.5 mA, relative to V_{BB}	6.4	6.7	7.5	V
		V_{BB} = 5 V, I_{CPAVG} = 1 mA, relative to V_{BB}	4.15	5	–	V
GATE DRIVE UNIT						
High-Side Gate Drive Output	V_{GH}	V_{BB} ≥ 8 V	6.75	6.9	–	V
Low-Side Gate Drive Output	V_{GL}	V_{BB} ≥ 8 V	7.0	7.3	–	V
Gate Drive Source Current	I_{SO}	Level 0, 45 V ≥ V_{BB} ≥ 7 V	4.4	6.6	8.8	mA
		Level 1, 45 V ≥ V_{BB} ≥ 7 V	9.6	13	16.6	mA
		Level 2, 45 V ≥ V_{BB} ≥ 7 V	20.7	26.5	32.3	mA
		Level 3, 45 V ≥ V_{BB} ≥ 7 V	43.8	53.7	63.5	mA
Gate Drive Sink Current	I_{SI}	Level 0, 45 V ≥ V_{BB} ≥ 7 V	5.6	13.3	21.0	mA
		Level 1, 45 V ≥ V_{BB} ≥ 7 V	13.2	25.0	37.0	mA
		Level 2, 45 V ≥ V_{BB} ≥ 7 V	33.8	50	66.5	mA
		Level 3, 45 V ≥ V_{BB} ≥ 7 V	73.5	98.4	123.3	mA
MOTOR DRIVE						
PWM Duty On Threshold	PWM_{ON}	Relative to target	–0.5	–	+0.5	%
PWM Duty Off Threshold	PWM_{OFF}	Relative to target	–0.5	–	+0.5	%
PWM Input Frequency Range	f_{PWM}	PWM input frequency setting = 0	2.5	–	100	kHz
		PWM input frequency setting = 1	80	–	3200	Hz
Clock Input Frequency Range	f_{CLOCK}	CLOCK mode	1	–	2000	Hz
SPD Standby Threshold (Analog Enter)	$V_{SPD(TH\_ENT)}$		50	100	150	mV
SPD Standby Threshold (Analog Exit)	$V_{SPD(TH\_EXIT)}$		0.4	0.75	1.0	V
SPD On Threshold	$V_{SPD(ON)}$	ON/OFF setting = 10%	200	245	290	mV
SPD Maximum	$V_{SPD(MAX)}$		–	2.5	–	V
SPD ADC Resolution	$V_{SPDADC(RES)}$		–	9.78	–	mV
SPD ADC Accuracy	$V_{SPDADC(ACC)}$	V_{SPD} = 0.2 to 2.5 V	–45	–	45	mV
Speed Closed-Loop Accuracy	$f_{SPD(ACC)}$	PWM mode or Analog mode	–5	–	5	%
		Clock mode	–0.1	–	0.1	rpm
Dead Time	t_{DT}	Code = 9	–	400	–	ns
Motor PWM Frequency	f_{PWM}		23.06	24.4	25.74	kHz

Continued on next page...

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40 to 125°C, V_{BB} = 5.5 to 28 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
VBB UVLO	$V_{BB(UVLO)}$	V_{BB} rising	–	4.75	4.95	V
VBB UVLO Hysteresis	$V_{BB(HYS)}$		200	300	450	mV
VREG UVLO	$V_{REGUVLO}$	V_{REG} falling	–	2.6	–	V
VCP UVLO	V_{CPUVLO}	V_{CP} falling	3.6	3.9	4.2	V
		V_{CP} rising	3.9	4.2	4.5	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	175	–	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
VDS Comparator Threshold	V_{DS_THR}	Level 0	0.89	1	1.11	V
		Level 1	1.75	2	2.15	V
LOGIC, IO, I²C						
Input Current (SPD, FG)	I_{IN}	V_{IN} = 0 to 5.5 V	–5	1	5	µA
Input Current (BRAKE, DIR)	I_{IN}	V_{IN} = 5 V	–	50	–	µA
Logic Input Low Level	V_{IL}		0	–	0.8	V
Logic Input High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
FG output leakage	I_{FG}	V = 5.5 V	–	–	1	µA
FG, Fault saturation voltage	V_{LOGIC_SAT}	I = 4 mA	–	–	0.3	V
SCL Clock Frequency	f_{CLK}		7	–	100	kHz
EEPROM						
Number of Programming	N_{PROG}		–	–	1000	times

[1] Specified limits are tested at 25°C and 125°C and statistically assured over operating temperature range by design and characterization.
[2] The charge pump capacitors between CP1 and CP2, VBB and VCP are 220 nF ceramic capacitors.

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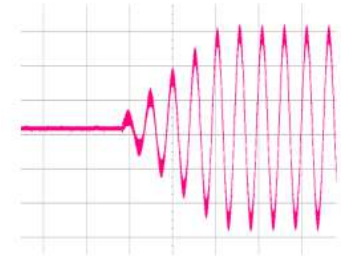
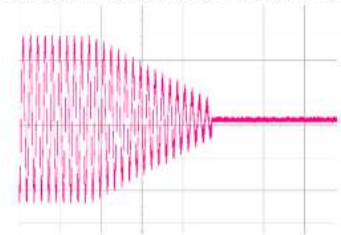
FUNCTIONAL DESCRIPTION

The A89307 is a three-phase BLDC controller with integrated gate driver. It operates from 5.5 to 50 V, and targets battery cooling fan applications.

The integrated FOC control algorithm achieves the best efficiency and dynamic response and minimizes acoustic noise. Allegro's proprietary Non-Reverse Startup algorithm improves the startup performance. The motor will startup towards the target direction after power up without reverse shaking or vibration. The Soft-On-Soft-Off feature gradually increases the current to the motor at "on" command (windmill condition), and gradually reduces the current from the motor at the "off" command, further reducing the acoustic noise and operating the motor smoothly.



Current Waveform of Soft On



Current Waveform of Soft Off

Speed Control

Speed demand is provided via the SPD pin. Three speed control modes are selectable through the EEPROM. The A89307 also features closed-loop speed, torque, and power functions, which can be enabled or disabled via the EEPROM.

PWM Mode: In this mode, the motor speed is controlled by the PWM duty cycle on the SPD pin, and higher duty cycle represents higher speed demand. If open-loop mode is selected, the output voltage amplitude will be proportional to the PWM duty cycle. If closed-loop speed is enabled, the motor speed is proportional to the PWM duty cycle, and 100% duty represents the rated speed of the motor, when speed curve transformer is not active, which can be programmed in the EEPROM. The equivalent is true for closed-loop torque and power modes.

$$CLOSE\_LOOP\_SPEED = RATED\_SPEED \times DUTY\_INPUT$$

The SPD PWM frequency range is 80 Hz to 100 kHz. If it is higher than 2.8 kHz, set PWMIN_RANGE = 0; if it is lower than 2.8 kHz, set PWMIN_RANGE = 1.

Analog Mode: In the clock speed control mode, the closed-loop speed is always enabled. Higher frequency on the SPD pin will drive a higher motor speed as follows:

$$CLOSED\_LOOP\_SPEED = RATED\_SPEED \times ANALOG\_INPUT / SPD_{MAX}$$

The equivalent is true for closed-loop torque and power modes.

CLOCK Mode: When using clock mode, closed-loop speed is always enabled. The default input for clock mode is the SPD terminal, but there are options to use either the DIR or BRAKE terminals instead. Either of these options allows use of the I^2C interface and clock mode at the same time. Higher frequency on the clock input will drive a higher motor speed as follows:

$$CLOSE\_LOOP\_SPEED\ (rpm) = CLOCK\_INPUT \times CLOCK\_SPEED\_RATIO,$$

where the SPEED_CTRL_RATIO can be programmed in the EEPROM. For example, if the ratio is 4 and the clock input frequency is 60 Hz, the motor will operate at 240 rpm. Note the number of motor pole pairs must be set properly in the programming application for the rated speed (RPM) setting to be accurate.

If the clock frequency commands a speed that is higher than twice the rated speed, A89307 treats it as a clock input error, and stops the motor.

For all the three speed control modes with closed-loop speed enabled, if the demand speed is higher than the maximum speed the system can run at a certain supply voltage and load condition, the A89307 will just provide the maximum output voltage (if current limit is not triggered), or the maximum output current (if current limit is triggered).

The SPD pin is also used as SCL in the I^2C mode.

Power Control: The A89307 has integrated power control with speed control. The speed control will receive the reference speed from the demand interfaces. When the motor runs below the current limit, the motor will operate as speed control. If the driving DC current reach to the DC current limit, I_{LIM}, the control overrides the speed control and provide the constant DC current control.

The power control has two modes depending on V_{BB}. If V_{BB} is less than V_{POW}, the control will provide the DC current limit.

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When the motor runs with a load, which does not require I_{LIM}, the motor will run a constant speed as the demand interface requires. If the connected load requires I_{LIM} to achieve the target speed, the current control will be active and speed control will be ignored. If V_{BB} is greater than V_{POW}, the power control is active, and the controlled power is defined as P_{LIM}. If the connected load requires greater than P_{LIM}, the speed control is ignored and operates as constant power control.

V_{POW} can be selected by POWCON_VOL_LIM. The DC current limit, I_{LIM}, can be selected by POWCON_DCCUR_LIM. When V_{BB} is above V_{POW}, then the power limit, P_{LIM}, is defined as $V_{POW} \times I_{LIM}$.

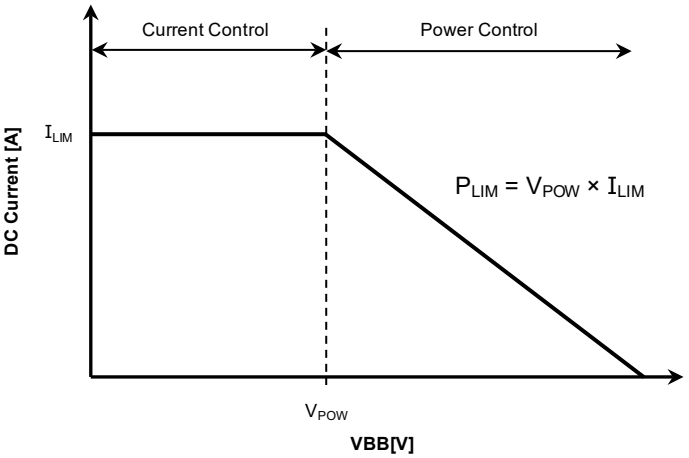

Figure 2 : Power Limit

Motor Stop and Standby Mode: If the speed demand is less than the programmed threshold, the motor will stop.

On/Off setting	On threshold	Off threshold
5.8%	7.9%	5.8%
9.7%	11.8%	9.7%
12.8%	15.0%	12.8%
19.5%	21.6%	19.5%

For example, consider 10% is set as the threshold. If PWM duty is less than 9.8% (in PWM mode), or the analog voltage is less than 250 mV (in Analog mode), or the CLOCK input frequency is less than 9.8% of the RATED_SPEED (in CLOCK mode), the IC will stop the motor and enter idle mode.

In order to enter standby, two conditions must be met:

1. The motor must be stationary (this requirement can be removed by setting the EEPROM), and
2. PWM or CLOCK signal remains logic low (in PWM and CLOCK mode), or the analog voltage remains less than V_{SPDTH_ENT} (in Analog mode) for longer than one second.

A rising edge on PWM or CLOCK will wake the IC in PWM and CLOCK mode, and in Analog mode, the SPD voltage must be higher than V_{SPDTH_EXIT} to wake up the IC.

Standby Mode will turn off all circuitry including the charge pump and VREG.

After powering on, the device will always be in active mode before entering standby mode.

Standby mode can be disabled in the EEPROM.

Direction Input: Logic Input to control motor direction. For logic high, the motor phases are ordered A→B→C. For logic low, the motor phases are ordered A→C→B. The A89307 supports changing the direction input while the motor is running. The direction can also be controlled through register.

BRAKE: Active High signal turns on all low sides for braking function. The brake function overrides speed control input. Care should be taken to avoid stress on the MOSFET when braking while motor is running. With braking, the current will be limited only by VBEMF/RMOTOR. The A89307 includes an optional feature which holds off braking until the motor speed drops to a low enough (configurable) level so that the braking current will not damage the MOSFET.

FAULT: Open-drain output provides motor operation fault status. Default is high when there is no fault.

The detail of FAULT signal pattern is shown below. The priority indicates that when multiple faults occur, higher priority signal will be indicated.

Fault type	Priority	FAULT pin
Lock detected	5	low
OCP	4	0.67 seconds high 0.67 seconds low
OTP	6	0.67 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high
system error	2	0.08 seconds low 0.08 seconds high 0.08 seconds low 1.09 seconds high
OVP	1	0.17 seconds high 0.17 seconds low
zero speed demand	3	0.25 seconds high 0.08 seconds low 0.34 seconds high 0.67 seconds low

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FG: Open-drain output provides motor speed information to the system. The open-drain output can be pulled up to V_{REG} or an external 3.3 or 5 V supply.

The FG pin is also used as SDA in the I²C mode. The first I²C command can pass only when FG is high (open drain off). After the first I²C command, the FG pin is no longer used for speed information, and the FG pin is dedicated as a data pin for the I²C interface.

FG is default high after power on and exit from standby mode, and it remains high for at least 9.8 ms. To ensure successful I²C communication, it is recommended to have the first I²C demand within 9.8 ms after power up or exit from standby mode.

FG function can be disabled in EEPROM; then the FG pin will be dedicated as the SDA signal for I²C. If observing FG signal is required in I²C mode, the FG signal can be reassigned to the FAULT pin by sending the I²C command 0x00A0 to address 195 (decimal). To return Fault to normal operation, send the I²C command 0x0000 to address 195 (decimal).

VREG: Voltage reference (2.8 V) to power internal digital logic and analog circuitry. VREG can be used to power external circuitry with up to 10 mA bias current if desired. A ceramic capacitor with 0.22 µF or greater is required on the pin to stabilize the supply (X8R rating or better is recommended).

When VREG is loaded externally, the power consumption of the internal LDO is calculated by the equation:

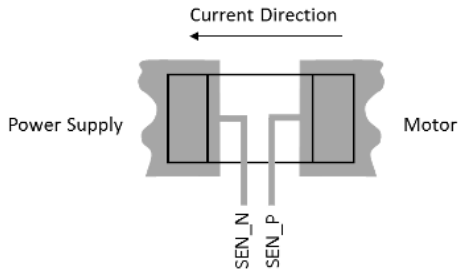
$$P_{LDO} = (I_{LOAD} + I_{INTERNAL}) \times (V_{BB} - V_{REG}).$$

Ensure that the system has sufficient power dissipation and the temperature remains within the operating temperature range. A89307 thermal shutdown function does not protect the LDO.

Bus Current Sensing

A single shunt-resistor connecting between SENN and SENP is used to measure the bus current for FOC algorithm and current limit. The resistor value is about tens of a milliohm, depends on the rated current of the system. The integrated shunt-resistor amplifier has a gain of 14.5, and the output range is 0 to 1 V. The voltage difference between SENN and SENP should be less than 65 mV to prevent the signal saturation. For example, if the rated current is 4 A, using a 15 mΩ sensing resistor is recommended, so that 4 A × 15 mΩ is between 55 and 65 mV.

Use Kelvin sensing connection for the shunt resistor.



Lock Detect: A logic circuit monitors the motor position to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for the configurable t_{LOCK} time, before an auto-restart is attempted. For additional information, refer to the application note.

Current Control: The motor's rated current at rated speed and normal load must be programmed to the EEPROM for proper operation. The A89307 will limit the motor current (phase current peak value) to 1.3 times the programmed rated current during acceleration or increasing load, which protects the IC and the motor. The current profile during startup can also be programmed.

Overcurrent Protection (Short Protection): The VDS voltage across each power MOSFET is monitored by the A89307. When a MOSFET is switched on, its VDS is ignored for the programmable blank time. Also, the VDS comparator is always filtered with a programmable filter time. If an enabled MOSFET VDS is higher than the threshold after blank time and for longer than filter time, an OCP fault is triggered and the IC will latch all MOSFETs off.

Motor Startup

The A89307 provides a robust open-loop startup to ensure the motor spins in feedback control. When the motor is in standstill, there is no BEMF information available, so the open-loop startup is required.

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Motor Startup State Machine

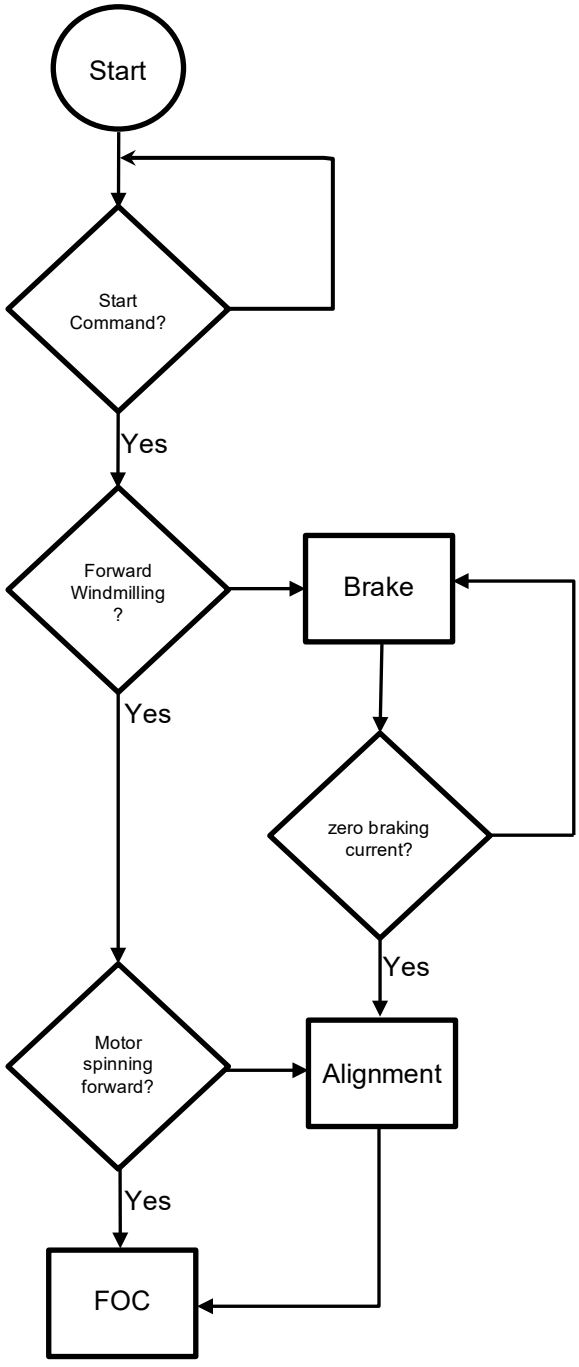
The A89307 has its own dedicated state machine to determine motor rotation conditions to provide robust startup. The following flowchart displays mode processing.

When the device accepts the start command, the controls check the BEMF comparator to determine windmilling condition.

If the motor is spinning backwards, the controller applies brake until the brake current disappears.

If the motor spinning is forward, the controller synchronizes driving frequency and goes into full sensorless control.

When the motor is at a standstill, the controller applies the rotor alignment and starts the motor control.



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Rotor Alignment: When the A89307 is commanded to spin the motor, the controller will execute motor rotor alignment to ensure the rotor is parked at a known position. There are four different modes to achieve rotor alignment or detection.

The first option is Align&Go. The A89307 applies a low driving frequency with current control to the winding in order to generate a known position flux into the rotor. The permanent magnet integrated rotor will be gravitated to the flux.

The second option is two-pulse IPD. This method uses salient and winding saturation characteristics to determine rotor position. There are two stages to complete two-pulse IPD. The first stage applies test pulse sequences to the motor. If there is enough saliency, the A89307 will lock up the rotor position within 30 degrees, from 0 to 180 degrees or 180 to 360 degrees.

When the first stage is completed, the A89307 will apply a test sequence to check the inductance saturation in order to check the magnet pole. Once these entire sequences are completed, the A89307 can determine the rotor angle within 30-degree accuracy.

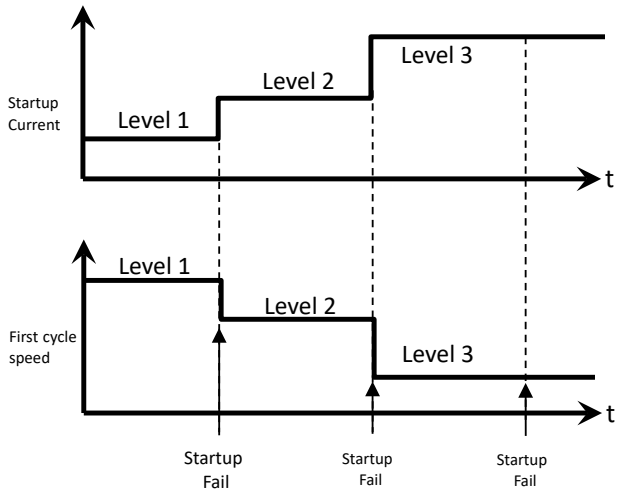
The third option is six-pulse IPD. In this mode, the A89307 will only use inductance saturation characteristics to determine the rotor position. Once the sequence is completed, the A89307 will determine rotor angle within 60 degrees.

The fourth option is slight-move mode. In this mode, a test sequence will be inserted to check saliency characteristics, which are described in the second option. When the test sequence is completed, the controller determines a rough position. At this stage, the error might be 180 degrees or none. After it completes, the controller will energize the winding based on the determined position. Two of the three phases are driven with duty cycle control, which can be programmed by SLIGHT_MV_DEMAND [2:0] and the remaining phase is undriven. While the controller is energizing the bridge, the controller will wait for a BEMF zero-crossing edge on undriven phase. When the zero-crossing event is happening, the rotor will spin and gravitate to the energized angle. After completion, the controller inserts the saliency characterization sequence again for comparison. If there is no error, the determined parked position is correct; if there is an error, the controller accounts for it and determines the parked position.

Open-Loop Startup: When the A89307 completes rotor alignment, an open-loop startup will be executed. In this mode, the amplitude of phase current will be regulated to provide a stable torque. The driving frequency will be ramping up until stable BEMF is generated. Once the open-loop startup is completed, the A89307 will be in sensorless FOC control technique.

The regulated open-loop startup current can be selectable by predetermined levels, which are stored in EEPROM. The A89307 provides three levels of configurations. There is an activation bit in the I²C register, STRP_LOCK_RTRY_CURR_LVL_EN. When it is 0, the startup current will be always constant. If it is 1, the automatic startup current level control is active.

At the first startup attempt, the A89307 always use Level 1, STARTUP_CURRENT_LVL1 [2:0], and if the startup is ended up with fail, stopped by stall detection, next startup attempt will be Level 2, STARTUP_CURRENT_LVL2 [2:0]. The startup current level will be increased until Level 3, STARTUP_CURRENT_LVL3 [2:0]. If the startup fails using Level 3, the A89307 will continue using Level 3. When the demand is set to idle state, the current leveling system will be reset to Level 1. The current level sequence is shown below.



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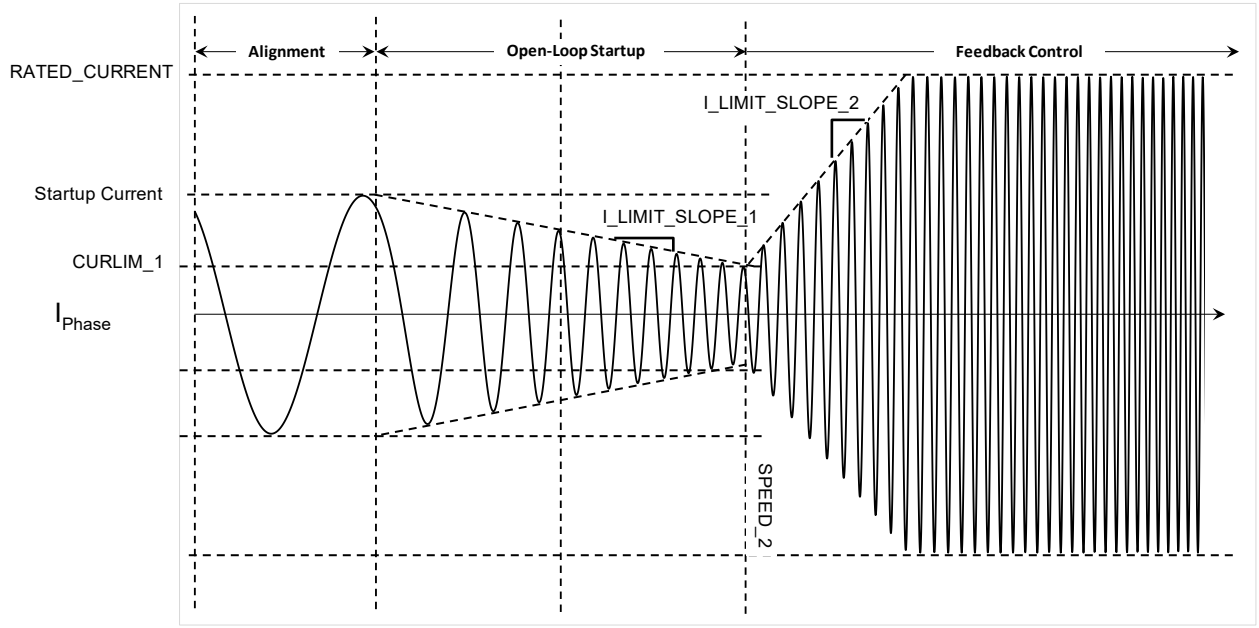
Open-Loop Startup Current Profile: The A89307 has a feature to modify the ramp-up period. This feature helps minimize acoustic noise from the open-loop startup to the sensorless control. Current amplitude is a factor at any given driving speed and load to maintain the appropriate phase advance. The appropriate current level depends on motor property and connected load. For reliable startup, the startup current must be high enough to spin the motor. The startup current is usually set higher than the required current to gain enough startup torque, but this incurs phase advance error. It is also necessary to meet various startup load conditions to have robust startup. To achieve a quieter transition, it may be possible to reduce the current towards the end of the open-loop startup period if load conditions permit. When the current level is closer to the required current level in feedback control, then transition noise may be able to be minimized.

The startup current profile can be enabled via TWO_SLOPE_M. When it is 1, two slope system is active. There are several parameters that define startup current: I_LIMIT_SLOPE_1, I_LIMIT_SLOPE_2, SPEED_2, RATED_CURRENT, STARTUP_CURRENT. Startup current is defined by STARTUP_CURRENT when STRTP_LOCK_RTRY_CURR_LVL_EN is 0. When STRTP_LOCK_RTRY_CURR_LVL_EN is 1, STARTUP_CURRENT_LVX will be used to determine the Startup Current level. Refer to Open-Loop Startup section for further details.

After the alignment period is executed, the phase current limit will be ramping down by following I_LIMIT_SLOPE_1 until the driving frequency reaches SPEED_2. When the driving frequency is greater than SPEED_2, then the phase current limit will be ramping up by following I_LIMIT_SLOPE_2 until it reaches RATED_CURRENT.

Note that the phase current limit should be sufficient to drive at any given driving condition; otherwise, the driving performance may be insufficient.



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External MOSFET Gate Drive

The A89307 is designed to work with external, low on-resistance power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side MOSFETs are provided from an internal regulated supply. The charge current for the high side is provided from VCP supply, which is delivered from the integrated charge pump. The VCP voltage is regulated at 6.8 V in order to supply enough voltage to turn on the high-side MOSFETs. The VCP voltage is monitored by dedicated monitor circuit. If the VCP voltage drops to a certain level, defined as V_{CPUVLO}, then the A89307 stops the control and the MOSFETs will be turned off in order to protect the external MOSFET from an abnormal situation.

Gate Control: The A89307 provides multiple gate driving strengths to optimize the emission level. Fast slewing rate on VDS makes the emission level high, but it reduces switching loss. If the slewing rate is slow, then the emission level is low but switching loss is increased. It is essential to assess the tradeoff to ensure target performance.

The A89307 has a four-level current control to drive the gate. The gate control has two stage current control to turn on the external MOSFET. When the controller gives the command to turn on, it provides a constant current source, I_1 in the figure, which can be programmed by the register DRIVE_GATE_SLEW [1:0] to the gate. The charging currents are defined in the Electrical Characteristics table. When VDS voltage is reached lower than VDS threshold voltage, defined by VDS_THRESHOLD_SEL, the control provides maximum current to reach the higher gate voltage as quickly as possible to minimize the on-resistance on the external MOSFET.

The gate control has a three-stage current control to turn off the external MOSFET. This provides faster switching speed compared with two-stage control. Until reaching the Miller region, VDS will not start slewing, so a faster rate can be applied in order to minimize dead time without compromising emission performance.

It is required to enable three-stage current control; otherwise, two-stage current control is applied. If GDPULSE [2:0] is set to a value other than 000, then the three-stage current control will be enabled. If it is set to a non-zero value, the period of t_{slew} is defined. The amount of I_{slew} is defined by GD_PULSECURRENT [1:0]. If it is 00, three-stage current control is disabled.

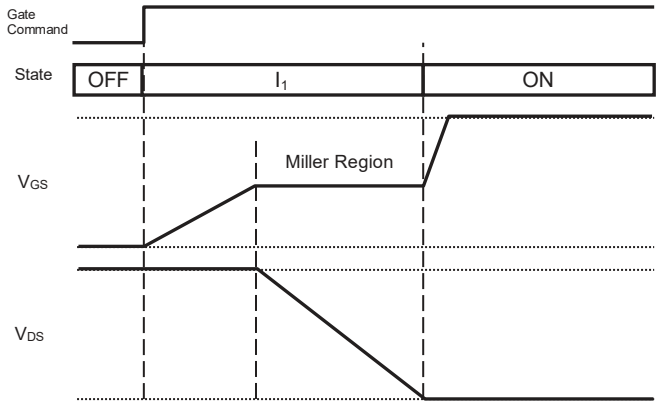

Figure 3: Off-to-On Transition (Slew Rate Control)

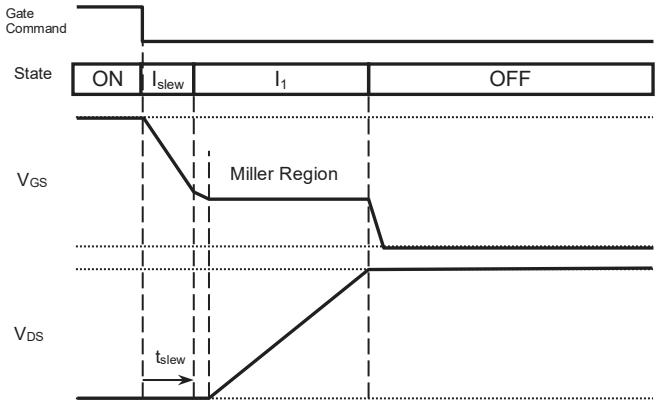

Figure 4: On-to-Off Transition (Slew Rate Control)

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Input-to-Output Transformer

The A89307 implements an optional, highly flexible input-to-output mapping ability. The configuration is stored in EEPROM addresses 32 through 63. Fundamentally, the transformer is a 9-bit (0 to 511) to 9-bit (0 to 511) transfer function, where the meaning of the output values changes depending on the selected control mode. The transformer operates in whichever of the four control modes is chosen: as a speed curve transformer, a torque curve transformer, a power curve transformer, or as a demand transformer in open-loop control mode.

If open-loop mode is selected, the specified output value determines the duty cycle applied to the motor. Thus, a value of 511 will cause the peak voltage applied to the motor to be the full VBB voltage. If one of the closed-loop modes is selected, the output range is determined by the control loop range setting. That setting specifies the maximum speed, torque, or power that the application requires, and corresponds to the value 511. For example, in closed-loop speed mode, if the control loop range setting is set to 1000 rpm, then a transformer output value of 255 will result in the motor spinning at 500 rpm.

Only the corner points of the desired curve are stored in the EEPROM, one point per address, and the remaining points are calculated using linear interpolation. The 9 MSBs of the EEPROM address are the input demand at the corner point, and the 9 LSBs of the address are the output demand for that point.

Only as many addresses that are needed to define the desired curve must be programmed. The last point defining the curve must have 511 as the input value, and all the following addresses in the EEPROM will be ignored. As many as 32 corner points can be stored, allowing for precise control of the demand.

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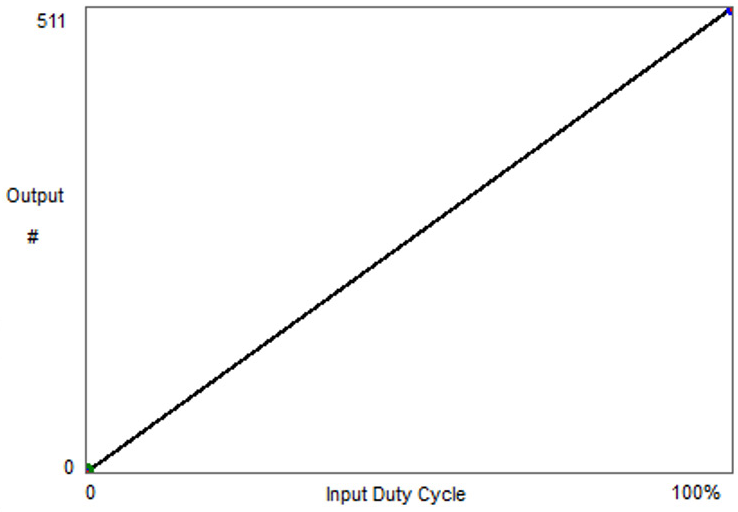
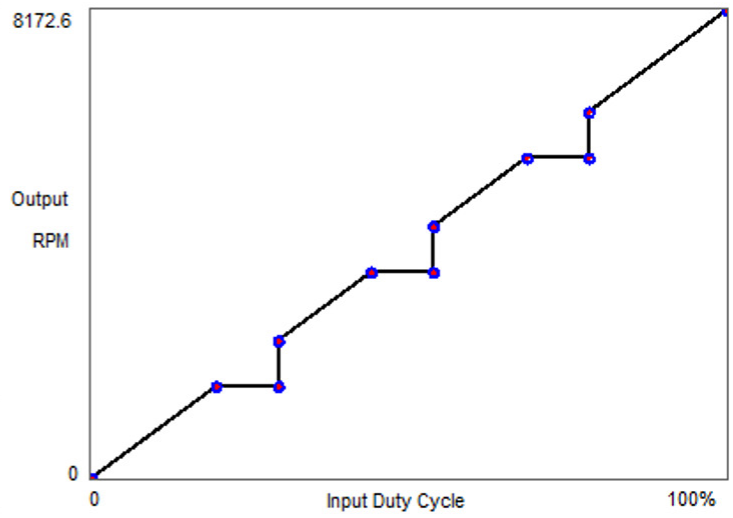
	In #	In %	Out #	Out %	#
32	0	0.0%	0	0.0%	0.0
33	511	100.0%	511	100.0%	511.0
34	0	0.0%	0	0.0%	0.0



Example 1: These screenshots are taken from the A89307 application—white boxes are the entered values. This is the most trivial example, where input = output. This is the curve that is used when the transformer is disabled. Because 511 is the input value in the second address, the 30 following addresses are ignored.

	In #	In %	Out #	Out %	Speed
32	0	0.0%	0	0.0%	0.0
33	100	19.6%	100	19.6%	1599.3
34	150	29.4%	100	19.6%	1599.3
35	150	29.4%	150	29.4%	2399.0
36	225	44.0%	225	44.0%	3598.5
37	275	53.8%	225	44.0%	3598.5
38	275	53.8%	275	53.8%	4398.2
39	350	68.5%	350	68.5%	5597.7
40	400	78.3%	350	68.5%	5597.7
41	400	78.3%	400	78.3%	6397.3
42	511	100.0%	511	100.0%	8172.6



Example 2: In this example, the control loop is set to closed-loop speed, and so the resulting rpm is shown in the last column of the table where the curve is defined. This curve is designed to avoid this motor's resonant frequency at 2000 rpm, and its harmonics at 4000 rpm and 6000 rpm.

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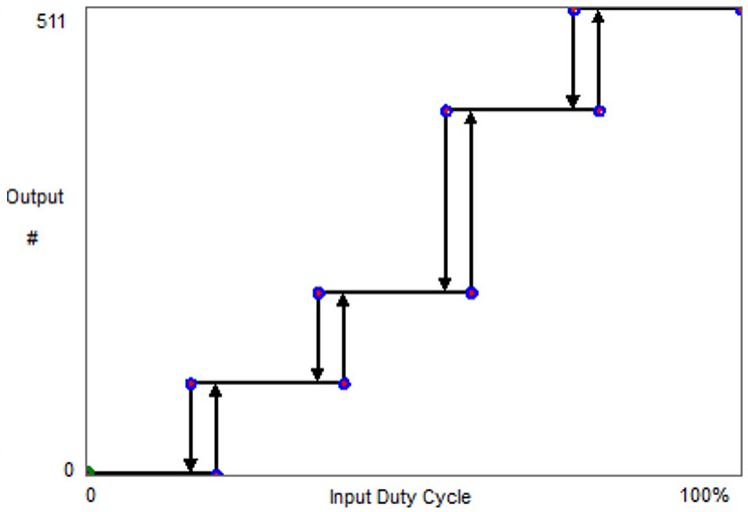
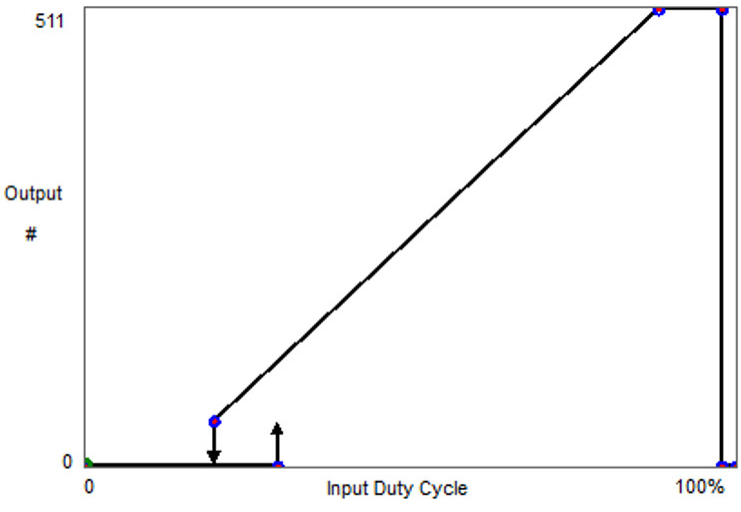
	In #	In %	Out #	Out %	#
32	0	0.0%	0	0.0%	0.0
33	100	19.6%	0	0.0%	0.0
34	80	15.7%	100	19.6%	100.0
35	200	39.1%	100	19.6%	100.0
36	180	35.2%	200	39.1%	200.0
37	300	58.7%	200	39.1%	200.0
38	280	54.8%	400	78.3%	400.0
39	400	78.3%	400	78.3%	400.0
40	380	74.4%	511	100.0%	511.0
41	511	100.0%	511	100.0%	511.0



Example 3: Hysteresis can be implemented by setting the input value of an address lower than the input value in the previous address. In this example, as the input demand is rising, the output demand will jump to next higher level at the vertical lines on the right of each transition. When the input demand is falling, the output demand will drop to next lower level following the vertical lines on the left of each transition. This prevents output jitter when the input is around a boundary.

	In #	In %	Out #	Out %	#
32	0	0.0%	0	0.0%	0.0
33	150	29.4%	0	0.0%	0.0
34	100	19.6%	50	9.8%	50.0
35	450	88.1%	511	100.0%	511.0
36	500	97.8%	511	100.0%	511.0
37	500	97.8%	0	0.0%	0.0
38	511	100.0%	0	0.0%	0.0



Example 4: In this example, the motor won't turn on until the input is about 30% and will turn off when the output falls below about 20%. The output will be at maximum when the input is between about 88% to 98%, and the motor will stop when the input is > 98%.

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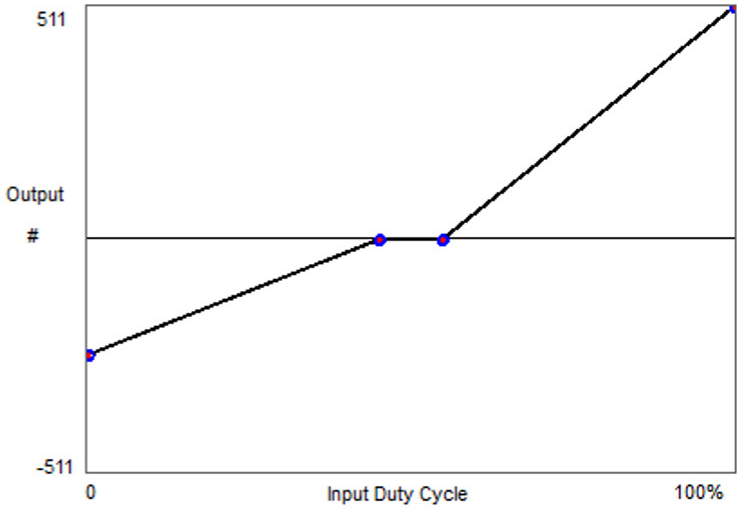
	In #	In %	Out #	Out %	#
32	0	0.0%	128	-49.8%	-254.5
33	230	45.0%	255	0.0%	0.0
34	280	54.8%	255	0.0%	0.0
35	511	100.0%	511	100.0%	511.0



Example 5: The curve can be set to control bi-directional operation as well. When the bidirectional option is selected, the output value 511 is still the highest output in one direction, but the output value 255 will stop the motor, and the output value 0 is the highest output in the reverse direction. Here, the motor will run at half speed reverse when input demand is 0, will stop when the input is between 230 and 280, and will run at full speed forward when the input is 511.

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Diagnostics

Lock Detect: The A89307 provides two lock detection options. The first option is a BEMF lock detection scheme. The A89307 has Kt, a mechanic constant observer to monitor the motor rotation. When it is active, the observer continuously estimates Kt based on the given control parameters, and the control is compared with the given Kt. When the estimated Kt exceeds the threshold, the control detects a stall.

The second option is startup lock detection. When the motor start to rotate, the controller is forcing the frequency to ramp up speed, and at the same time, the internal observer monitors the generated phase advance. At the end of the ramp-up period, the measurement is taken of the motor phase advance; if the generated phase advance is more than the specified angle, the control detects a stall. The threshold angle can be set via ANGLE_ERROR_LOCK.

When a stall is detected, motor control is stopped, and the motor will be coasting. The controller will attempt to restart after the period of 5 or 10 seconds, which can be selected by LOCK_RESTART_SET. When LOCK_RESTART_CM is set as 0, the hold period is specified as LOCK_RESTART_SET. If LOCK_RESTART_CM is 1, there will be no hold period prior to restart.

The number of repeats can be set to 3, 5, 10, or always. When always is selected, the controller will always restart the motor. When non-always values are selected, the controller will attempt to restart up to the specified number; when exceeded, the controller will hold at the lock detect state until zero-demand is inserted. When the controller receives zero-demand, then the lock detect counter is reset.

OCP: The A89307 has overcurrent detection in order to protect the external power MOSFET. The OCP fault has highest priority; when it is detected, the control immediately takes an action.

The OCP monitors all six VDS voltages on the external power MOSFETs when it is commanded on. When excessive voltage appears, then the control will detect the fault and turn off all MOSFETs. The control will be in OCP fault mode. Fault recovery depends on configuration, OCP_RESET_MODE. When it is 0, the motor will only restart when the zero-speed demand is inserted. When it is 1, the control automatically restarts the motor after 5 seconds. If OCP_RST_CNT is set as 0, the hold period specified as OCP_RESET_MODE. If OCP_RST_CNT is 1, there will be no hold period prior to restart. The external power FET devices may overheat due to repeated overcurrent conditions while the fault remains, and overheating may cause damage to the MOSFET. Care must be taken by the user for any abnormal conditions.

There are two filter systems to avoid mis-triggering OCP. When a gate command is inserted, OCP detection is masked for the period of t_{BLANK}. The period and target MOSFET can be selected via OCP_MASKING. The blanking timer should cover up to the Miller region to have robust operation. There is also an additional filter, which is filtering timer. While the gate is on, an overvoltage will be masked for the blanking time, t_{FIL} to avoid misdetection. The filtering time can be selected via OCP_ENABLE. The timing chart is described in the OCP timing diagram below. OCP threshold voltage can be selected via VDS_THRESHOLD_SEL. The threshold is specified in the Electrical Characteristics table as V_{DS_THR}.

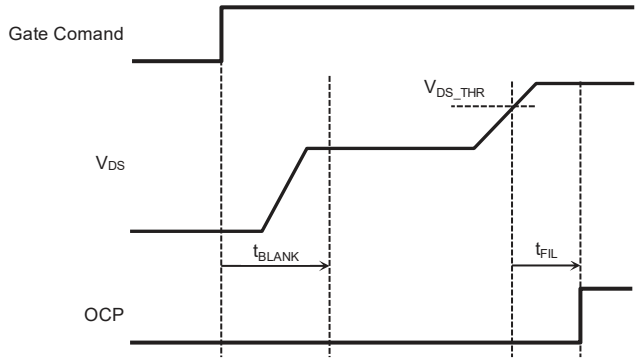

Figure 5: OCP timing diagram

System Error: A system error occurs when the charge pump voltage or the internal regulator which supplies the low-side gate drivers falls below the respective undervoltage threshold, VBB voltage rises above the threshold voltage or a demand PWM frequency error is detected. The motor outputs are disabled on a system error and will remain off until the voltage that caused the error rises above the respective UVLO threshold plus hysteresis. The FAULT terminal indicates system when it is triggered. The detail is described in FAULT section.

OVP: The A89307 has VBB overvoltage protection. If OVP_EN is set as enable, when V_{BB} exceed 18 V, the motor control will be stopped, and the motor will coast. The exact overvoltage threshold is specified as V_{BBOV_RIS}. When V_{BB} goes below the level, V_{BBOV_FAL} then motor will try to restart immediately.

If OVP_EN is set as disable, VBB overvoltage protection is disabled. There will be no flag on FAULT terminal by this fault and no protection will be applied.

Zero Speed Demand: The A89307 provides zero-speed demand indication. When the curve transformer is active, the resultant demand will be considered. When the device receives

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zero demand, it will be detected. The zero-speed demand is indication only. When the device receives a demand other than zero speed, the flag will be removed automatically.

Overtemperature: The A89307 has internal self-protection from overheating. When the internal temperature exceeds the threshold, T_{JTSD}, the motor control is stopped, and the motor will coast. When the temperature returns to normal operating range, $T_{JTSD} - \Delta T_J$, then the motor will automatically restart if the demand is inserted.

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I²C Operation and EEPROM/Register Map

The I²C interface allows the user to write to and read from the internal registers, and to program parameters into the EEPROM (writing to EEPROM is explained later in this document). The A89307 I²C 7-bit slave address, also referred to as the device ID, is fixed at 0x55. The figures below show the I²C interface timing.

Upon power-up, the data in the EEPROM is loaded into a group of the internal registers (referred to as shadow registers), and those registers control the system operation. The register values can then be overwritten via the I²C port, and this will change the system operation on the fly. Any changes to the shadow registers will be overwritten upon the next power-up. Likewise, any changes made to the EEPROM will have no effect until the next power-up. The one exception to this is the data defining the input transformer curve, which does not have associated shadow registers—the data defining the curve is read directly from EEPROM during operation.

The addresses of the shadow registers are offset from their associated EEPROM addresses by 64. For example, EEPROM address 10 is loaded into shadow register 74 upon power-up. To change a parameter on the fly that is contained in EEPROM address 10, the data must be written to register 74 using the I²C port. There are no shadow registers associated with EEPROM addresses 0 through 7, or with addresses 32 through 63.

The following diagrams illustrate how to read and write to the registers using the I²C port.

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Write to a register:

- Start condition
- 7-bit I²C slave address (1010101), R/W Bit = 0 (write)
- Internal register address
- 3 data bytes, MSB first
- Stop condition

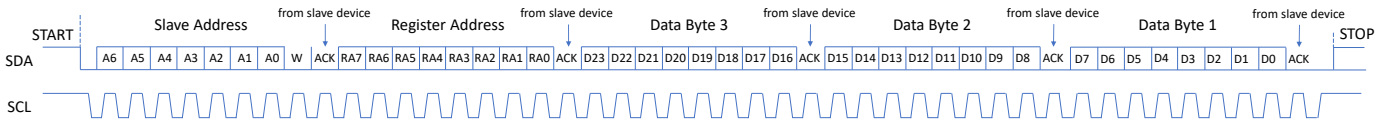
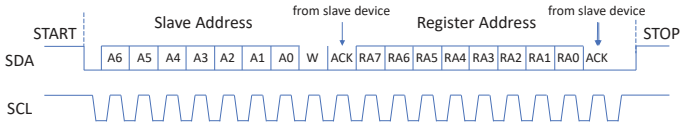


Figure 6: Write to an I²C register

Read from a register: a two-step process:

- Start condition
- 7-bit I²C slave address (1010101), R/W bit = 0 (write)
- Internal register address to be read
- Stop condition



- Start condition
- 7-bit I²C slave address (1010101), R/W Bit = 1 (read)
- Read 3 data bytes
- Stop condition

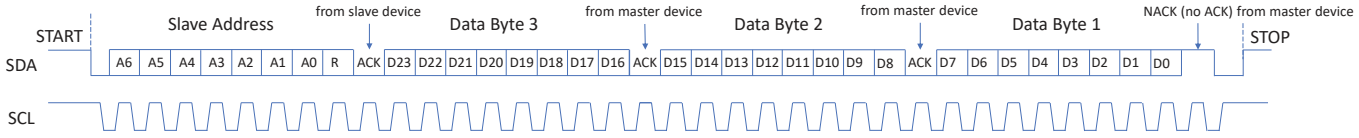


Figure 7: Read from an I²C register

I²C Continuous Read

Note the master sends an ACK after each byte is received. After the 3 bytes of one register address is received, the master typically sends a NACK (no ACK) to indicate the transmission is complete. Alternatively, the master may continue reading from the next address by sending an ACK after the last byte, and the A89307 will begin sending data byte 3 of the next higher register address on the next clock edge. The A89307 will continue sending data from the next higher address until it receives a NACK. This allows for reading data from multiple registers quickly, without needing to write each specific address per the first step of this process.

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REGISTER AND EEPROM MAP

Each register bit is associated with one EEPROM bit. The register address is the associated EEPROM bit address plus 64. For example, RATED_SPEED is in EEPROM address 8, bits[10:0]; the associated register address is 72, bits[10:0].

In the following table, the bits that are not described should be kept at their default values. Changing these values may cause malfunction or damage to the part. If programming the EEPROM with a custom programmer, it is recommended to use the A89307 application to determine the appropriate settings, save the settings file, and use the file contents to program to the EEPROM. The application's settings file contains one line for each EEPROM address, containing addresses 8 through 63, but skipping address 31 (55 lines/addresses total).

Addresses 0 through 5 and address 31 are factory-locked and cannot be changed.

Registers not shown in the table are not for users to access. Changing the value in undocumented registers may cause malfunction or damage to the part.

EEPROM address 6, (No shadow register associated)

Bits	Name	Description
17:0	Reserved	The contents shall be kept as default.

EEPROM address 7, (No shadow register associated)

Bits	Name	Description
17:0	Reserved	The contents shall be kept as default.

EEPROM address 8, Shadow register address 72

Bits	Name	Description
17:16	Reserved	The contents shall be kept as default.
15:15	PWMIN_RANGE	Input PWM frequency range selection: 0: > 2.8 kHz 1: ≤ 2.8 kHz
14:14	DIRECTION	Direction of motor rotation: 0: A→C→B 1: A→B→C
13:13	ACCELERATE_RANGE	Acceleration range used for Startup Acceleration setting (Hz/s): 0: 0 to 816 1: 0 to 12.75
12:11	CLOCK_PWM	SPD input mode: 0: PWM mode 1: Clock mode (using PWM input) 2: Clock mode (using BRAKE input) 3: Clock mode (using DIR input)
10:0	RATED_SPEED	This is the max speed used in the application. In clock mode, this sets the max frequency, when PMW = 100%. Rated Speed (Hz) = RATED_SPEED_REGISTER_VALUE × 0.530.

EEPROM address 9, Shadow register address 73

Bits	Name	Description
17:8	I_LIMIT_SLOPE_1	Quieter Startup current slope configuration 1
7:0	ACCELERATION	Specifies the motor acceleration rate at startup. This setting's range is selected with the ACCELERATE_RANGE setting, (Hz/s)

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EEPROM address 10, Shadow register address 74

Bits	Name	Description
17:16	Reserved	The contents shall be kept as default.
15:13	STARTUP_CURRENT	Initial startup current limit (scale factor relative to Rated Current). 1 through 7: Startup Current = Rated Current × 1/8 × (value + 1). Do not set to 0.
12:12	Reserved	The contents shall be kept as default.
11:11	SPD_MODE	SPD input mode: 0: Digital (PWM or Clock mode). 1: Analog.
10:0	RATED_CURRENT	This is the motor current when running at the Rated_speed setting. Rated Current (mA) = RATED_CURRENT_REGISTER_VALUE / (SENSE_RESISTOR_REGISTER_VALUE / 125).

EEPROM address 11, Shadow register address 75

Bits	Name	Description
17:7	SPEED_2	Quieter startup current slope transition frequency.
6:6	MAX_CURR_START	Startup current setting: 0: Startup current is limited by STARTUP_CURRENT. 1: Ignore the control demand for the startup use 100% demand.
5:5	Reserved	Shall set this bit as 0.
4:4	OPEN_PH_PROTECTION	Open-phase protection: 0: Disabled. 1: Enabled.
3:3	OPEN_DRIVE	Open-drive debug control: 0: Normal operation. 1: Motor will be driven in open loop, Rated speed is then the target speed. Internally, the PID control coefficient Kp will be set 0.
2:1	Reserved	The contents shall be kept as default.
0:0	FG_STANDB_EN	FG feedback enable at standby mode: 0: Disabled. 1: Enabled.

EEPROM address 12, Shadow register address 76

Bits	Name	Description
17:17	Reserved	The contents shall be kept as default.
16:16	OPEN_WINDOW	Opens a window for inductance tuning – see Application Note: 0: Normal operation. 1: Window opened.
15:5	PWM_OUTPUT_FREQUENCY	Controls the output PWM frequency.
4:0	PID_P	Position observer PI loop proportional constant.

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EEPROM address 13, Shadow register address 77

Bits	Name	Description
17:15	Reserved	The contents shall be kept as default.
14:14	DELAY_START	Delay startup (for startup modes other than Align & Go): 0: V_{BB} must be stable within 25 ms after applying start signal. 1: V_{BB} must be stable within 100 ms after applying start signal.
13:8	Reserved	The contents shall be kept as default.
7:6	STARTUP_MODE	00: 6-pulse mode. 01: 2-pulse mode. 10: Slight-move mode. 11: Align & Go.
5:4	Reserved	The contents shall be kept as default.
3:3	POWER_CTR_EN	Power Control Enable: 0: Disable the current and accelerate and decelerate buffers. 1: Enable the current limit and accelerate and decelerate buffers.
2:0	PID_I	Position observer PI loop integration constant.

EEPROM address 14, Shadow register address 78

Bits	Name	Description
17:0	Reserved	The contents shall be kept as default.

EEPROM address 15, Shadow register address 79

Bits	Name	Description
17:17	Reserved	The contents shall be kept as default.
16:14	SAFE_BRAKE_THRD	Current below which to allow braking, relative to Rated current: 00: 1× 01: 2× 10: 4× 11: 8×
13:8	DEADTIME_SETTING	Deadtime selection: 0 through 64: (value + 1) × 40 ns.
7:7	SOFT_ON	0: Disabled. 1: Gradually increases the current at startup during a windmilling startup.
6:6	SOFT_OFF	0: Disabled. 1: Gradually reduces the current at motor stop.
5:4	Reserved	The contents shall be kept as default.
3:2	ANGLE_ERROR_LOCK	Lock detect during startup: 00: disabled. 01: 5 degree. 10: 9 degree. 11: 13 degree.
1:0	Reserved	The contents shall be kept as default.

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EEPROM address 16, Shadow register address 80

Bits	Name	Description
17:14	Reserved	The contents shall be kept as default.
13:12	BEMF_LOCK_FILTER	Determines the filter time for the BEMF lock detection: 00: Lock detection disabled. 01: Robust. 10: Medium. 11: Sensitive.
11:10	DECELERATE_BUFFER	Determines how quickly the output command can slew: 00: No buffer. 01: Fast buffer. 10: Medium buffer. 11: Slow buffer.
9:8	ACCELERATE_BUFFER	Determines how quickly the output command can slew: 00: No buffer. 01: Fast buffer. 10: Medium buffer. 11: Slow buffer.
7:6	FIRST_CYCLE_SPEED	Determines the align duration for Align & Go startup mode: 00: 2.23 Hz (0.4484 seconds). 01: 0.53 Hz (1.9 seconds). 10: 0.265 Hz (3.78 seconds). 11: 0.132 Hz (7.55 seconds).
5:4	OCP_MASKING	OCP comparators mask/blank time. Mask/blank occurs at output on/off transition: 00: No masking. 01: 320 ns mask. 10: 640 ns mask. 11: 1280 ns mask.
3:3	OCP_RESET_MODE	Determines when to restart motor after OCP is tripped: 0: Upon motor restart. 1: After 5 seconds.
2:0	OCP_ENABLE	OCP filter time and HS/LS OCP enabling. If an overcurrent condition exists at the time the OCP mask expires, the OCP filter time must pass before an OCP fault is triggered. 000: No Filter, HS/LS OCP Enabled. 001: 120 ns, HS/LS OCP Enabled. 010: 240 ns, HS/LS OCP Enabled. 011: 360 ns, HS/LS OCP Enabled. 100: 480 ns, HS/LS OCP Enabled. 101: 480 ns, LS OCP Enabled, HS OCP Disabled. 110: 480 ns, LS OCP Disabled, HS OCP Enabled. 111: 480 ns, HS/LS OCP Disabled.

EEPROM address 17, Shadow register address 81

Bits	Name	Description
17:11	Reserved	This register needs to set TBD.
9:9	I2C_SPEED_MODE	Input command via I²C enable: 0: IC terminals are used for user input command, according to settings. 1: SPEED_DEMAND setting in this register is used for user input command.
8:0	SPEED_DEMAND	Speed demand input, when I2C_SPEED_MODE is enabled. 0→511 represents 0→100%.

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EEPROM address 18, Shadow register address 82

Bits	Name	Description
15:14	DRIVE_GATE_SLEW	Gate driver current control. Refer to the Electronics Characteristics table: 00: Level 0. 01: Level 1. 10: Level 2. 11: Level 3.
13:8	IPD_CURRENT_THR	IPD current threshold (A) = IPD_CURRENT_THRD_VALUE × 0.086
7:0	Reserved	This register needs to set TBD.

EEPROM address 19, Shadow register address 83

Bits	Name	Description
17:17	Reserved	The contents shall be kept as default.
16:16	BRAKE_CONTROL	I^2C brake mode input when BRK_FROM_REG = 1: 0: Normal running. 1: Brake mode applied.
15:12	MOSFET_COMP_FALLING	MOSFET CISS compensation, current falling. Refer to the application note.
11:8	MOSFET_COMP_RISING	MOSFET CISS compensation, current rising. Refer to the application note.
7:5	GDPULSE	Duration control of high-side and low-side turn off pulse current: 000: Disabled. 001: 40 ns. 010: 80 ns. 011: 120 ns. 100: 160 ns. 101: 200 ns. 110: 240 ns. 111: 280 ns.
4:3	GD_PULSECURRENT	Pulse current amplitude setting: 00: Disabled. 01: Level 1. 10: Level 2. 11: Level 3.
2:0	INDUCTANCE_SHIFT	Motor inductance multiplier – the inductance setting is multiplied by 2^n.

EEPROM address 20, Shadow register address 84

Bits	Name	Description
17:17	BRAKE_INPUT	Motor brake mode control option: 0: Brake is controlled via the device terminal. 1: Brake is controlled via the I^2C direction register.
16:16	DIR_FROM_REG	Motor direction control option: 0: Direction is controlled via the device terminal. 1: Direction is controlled via the I^2C direction register.
15:8	SENSE_RESISTOR	Sense resistor value (mΩ) = SENSE_RESISTOR_VALUE / 3.7.
7:0	RATED_VOLTAGE	Motor rated voltage (V) = RATED_VOLTAGE_REGISTER_VALUE / 5.

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EEPROM address 21, Shadow register address 85

Bits	Name	Description
17:8	I_LIMIT_SLOPE_2	Quieter Startup current slope configuration 2.
7:5	SLIGHT_MV_DEMAND	Amplitude demand used for slight move startup mode : (%) = value × 3.2 + 2.4
4:3	SPEED_INPUT_OFF_THRESHOLD	Input threshold below which the motor is turned off. If the input transformer curve is enabled, this is applied after (to the output of) the transformer curve. 00: 9.7%. 01: 5.8%. 10: 12.8%. 11: 19.5%.
2:2	TWO_SLOPE_M	Startup current profile enable: 0: Disabled. 1: Enabled.
1:0	Reserved	The contents shall be kept as default.

EEPROM address 22, Shadow register address 86

Bits	Name	Description
17:16	Reserved	The contents shall be kept as default.
15:15	VDS_THRESHOLD_SEL	Short-circuit protection VDS threshold: 0: 1 V. 1: 2 V.
12:12	DEADTIME_COMP	Deadtime compensation enable: 0: Disabled. 1: Enabled.
11:11	LOCK_RESTART_SET	How long to wait before restart after lock detect is triggered: 0: 5 seconds. 1: 10 seconds.
10:10	VIBRATION_LOCK	Vibration lock detect: 0: Disabled. 1: Enabled.
9:9	SOFT_OFF_4S	Soft-off duration: 0: 1 second. 1: 4 seconds.
8:8	BRAKE_MODE	Brake mode: 0: Brake when safe, according to the SAFE_BRAKE_THRD setting. 1: Always brake, 100% uncontrolled.
7:6	RESTART_ATTEMPT	When to restart after lock detect is triggered: 00: Always. 01: 3 times. 10: 5 times. 11: 10 times.
5:0	CLOCK_SPEED_RATIO	The ratio between input frequency and rpm, used during clock mode. (rpm/Hz) = CLOCK_SPEED_RATIO_VALUE × 0.25. The maximum CLOCK_SPEED_RATIO value is 41; higher values will cause errors.

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EEPROM address 23, Shadow register address 87

Bits	Name	Description
17:17	CHECK_CURVE	Input transformer curve enable: 0: Input curve disabled. 1: Input curve enabled.
16:16	SPEED_CUR_BIDIR	Input transformer curve single or bi-directional mode: 0: Input curve operates in a unidirectional mode and the direction is set by the device terminal or via I^2C register. 1: Input curve operates in a bidirectional mode where the value 0 is the fastest reverse direction, 511 is the fasted forward direction, and 255 will stop the motor.
15:13	Reserved	The contents shall be kept as default.
12:11	OPERATION_MODE	Control loop mode: 00: Open loop operation, output voltage magnitude set by input demand. 01: Constant torque operation, torque range is set by PARAMETERFULL (EEPROM_23 [10:0]) × demand (as ratio)). 10: Constant speed operation, speed range is set by PARAMETERFULL (EEPROM_23 [10:0]) × demand (as ratio)). 11: Constant power operation, power range is set by PARAMETERFULL (EEPROM_23 [10:0]) × demand (as ratio)).
10:0	PARAMETERFULL	Used in constant speed/torque/power control loops to set the maximum control setpoint. This value is the setpoint when the input demand is 100%.

EEPROM address 24, Shadow register address 88

Bits	Name	Description
17:8	Reserved	The contents shall be kept as default.
7:0	MOTOR_RESISTOR	Motor phase terminal to center-tap resistance (phase-phase resistance / 2).

EEPROM address 25, Shadow register address 89

Bits	Name	Description
17:15	STARTUP_CURRENT_LVL3	Retry startup current level 3.
14:12	STARTUP_CURRENT_LVL2	Retry startup current level 2.
11:11	STRP_LOCK_RTRY_CURR_LVL_EN	Startup lock retry current level enable: 0: Disable. 1: Enable.
9:8	POWCON_VOL_LIM	Power control with speed regulation VBB voltage threshold, V_{POW}: 00: Disabled. 01: 12 V. 10: 12.5 V. 11: 14 V.
7:0	INDUCTANCE	Motor inductance, set along with the INDUCTANCE_SHIFT setting—this value is multiplied by $2^{INDUCTANCE\_SHIFT}$.

EEPROM address 26, Shadow register address 90

Bits	Name	Description
17:9	Reserved	The contents shall be kept as default.
8:0	KT_SET	Motor Kt constant.

EEPROM address 27, Shadow register address 91

Bits	Name	Description
17:0	Reserved	The contents shall be kept as default.

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EEPROM address 28, Shadow register address 92

Bits	Name	Description
17:15	CURRENT_LOOP_I	Current PI loop integration constant.
14:10	POWER_LOOP_P	Power PI loop proportional constant.
9:5	SPEED_LOOP_P	Speed PI loop proportional constant.
4:0	CURRENT_LOOP_P	Current PI loop proportional constant.

EEPROM address 29, Shadow register address 93

Bits	Name	Description
16:16	OCP_RST_CNT	OCP restart period control: 0: Specify as OCP_RESET_MODE register. 1: Immediate.
15:15	LOCK_RESTART_CM	Lock detection restart period control: 0: Specify as LOCK_RESTART_SET register. 1: Immediate.
14:13	FIRST_CYCLE_SPEED_3	Alignment frequency for the third attempt for Align&Go mode: 00: 2.23 Hz (0.4484 seconds). 01: 0.53 Hz (1.9 seconds). 10: 0.265 Hz (3.78 seconds). 11: 0.132 Hz (7.55 seconds).
12:11	FIRST_CYCLE_SPEED_2	Alignment frequency for the second attempt for Align&Go mode: 00: 2.23 Hz (0.4484 seconds). 01: 0.53 Hz (1.9 seconds). 10: 0.265 Hz (3.78 seconds). 11: 0.132 Hz (7.55 seconds).
10:9	FIRST_CYCLE_SPEED_1	Alignment frequency for the first attempt for Align&Go mode: 00: 2.23 Hz (0.4484 seconds). 01: 0.53 Hz (1.9 seconds). 10: 0.265 Hz (3.78 seconds). 11: 0.132 Hz (7.55 seconds).
8:6	Reserved	This register needs to set TBD.
5:3	POWER_LOOP_I	Power PI loop integration constant.
2:0	SPEED_LOOP_I	Speed PI loop integration constant.

EEPROM address 30, Shadow register address 94

Bits	Name	Description
17:7	POWCON_DCCUR_LIM	DC current limit for power control with speed control.
6:4	STARTUP_CURRENT_LVL1	Startup lock retry current level 1.
3:0	Reserved	The contents shall be kept as default.

EEPROM address 31, Shadow register address 95

Bits	Name	Description
15:0	OUTPUT_ARRAY_TRIM	Allegro-determined trim values (locked)

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EEPROM addresses 32-63 (No shadow registers associated)

Bits	Name	Description
17:9	X_INTERPOLATION_POINT	Corner point input value for the input transformer curve. No shadow register associated.
8:0	Y_INTERPOLATION_POINT	Corner point output value for the input transformer curve. No shadow register associated.

Note: Refer to application note and user interface for additional detail.

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PROGRAMMING EEPROM

The A89307 contains 64 words of EEPROM, and each word is 24 bits long. The 6 most significant bits of each word are used internally for error detection and correction (ECC), and the 18 least significant bits are used to store data. The handling of the ECC data is done automatically by the IC, and the user does not need to (and cannot) read or write the ECC data.

The EEPROM is programmed using the I²C interface. Before accessing the EEPROM, access must be enabled by writing the value 0x000001 I²C register address 196. There are three basic actions which can be performed on the EEPROM: read, erase, and write. Writing and erasing a single address in the EEPROM require 3 writes to the I²C port. These registers, addresses 161, 162, and 163, are described below and the sequence for writing to these registers is described on the following page. Reading a single address from the EEPROM requires only 1 read from the I²C port. Each EEPROM address is mapped to the corresponding I²C address. To read EEPROM address 8, for example, simply read I²C register address 8.

Each EEPROM address must be programmed individually. To change the contents of an EEPROM address, the word must first be erased before the new data is written. Programming each address requires about 30 ms (15 ms each for erasing and writing).

EEPROM Control – Register 191: Used to control programming of EEPROM

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Generate the high-voltage pulse required for writing or erasing. This bit self-clears when done, after 15 ms maximum.
1	ER	Set this bit high when erasing data to the EEPROM.
2	WR	Set this bit high when writing data to the EEPROM.
3	RD	This bit is for reading data but is not required for the method described in this datasheet to read the EEPROM.
23:4	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Address – Register 192: Used to set the EEPROM address to be altered

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	eeADDRESS					

Bit	Name	Description
5:0	eeADDRESS	Used to specify the EEPROM address to be erased or written. There are 64 addresses.
23:6	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Data_In – Register 193: Used to set the new EEPROM data to be programmed

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	eeDATAin																	

Bit	Name	Description
17:0	eeDATAin	Used to specify the new EEPROM data. This must be set to 0 when erasing the current contents.
23:18	n/a	Do not use; always set to zero (0) during programming process.

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Programming the EEPROM Examples

The example below is shown in the following format:

I²C Write/Read, I2C_REGISTER_ADDRESS [data] // comment

*Before accessing the EEPROM, the value 0x000001 must be written to I²C address 196.

Example #1: Write 261 (0x000105) to EEPROM address 7

1. Erase the existing data:
   - A. I²C Write, 192 [7] // set which EEPROM address to erase.
   - B. I²C Write, 193 [0] // set DATA_IN = 0x000000.
   - C. I²C Write, 191 [3] // set control to erase and set voltage high.
   - D. Wait 15 ms // requires 15 ms high-voltage pulse to erase.
   - E. I²C Write, 191 [3] // set control to erase and set voltage high.
   - F. Wait 15 ms // requires 15 ms high-voltage pulse to erase.
2. Write the new data:
   - A. I²C Write, 192 [7] // set which EEPROM address to write.
   - B. I²C Write, 193 [261] // set DATA_IN = 261 (0x000105).
   - C. I²C Write, 191 [5] // set control to write and set voltage high.
   - D. Wait 15 ms // requires 15 ms high-voltage pulse to write.

Example #2: Read EEPROM address 7 to confirm the data was properly programmed

1. Read the word:
   - A. I²C Read, 7 // read I2C register 7; this will be contents of EEPROM address 7.

*When done accessing the EEPROM, write the value 0x000000 to I²C address 196.

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APPLICATION INFORMATION

BOM Requirement

The A89307 requires several external passive components to provide correct operation. The choice of right components is essential to achieve desirable performance.

VBB Terminal (Input and Bypass Capacitors): The style and value of capacitors used with the A89307 determine input voltage and ripple. A low equivalent series resistance (ESR) multilayer ceramic capacitor is required to bypass the VBB pin. Additional bulk ceramic capacitors help to reduce AC impedance, reducing high frequency ringing and EMI. The value of the capacitor on VBB directly controls the amount of input ripple for a given input current pulse, such as during the PWM control of the three-phase bridges. Increasing the value of capacitor will reduce input ripple.

Multilayer ceramic chip capacitors (MLCC) typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions. There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R and X7S ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors are not recommended because of their extreme nonlinear characteristics of capacitance versus voltage and poor temperature stability.

Charge Pump Capacitors: Two charge pump capacitors are required for the high-side gate drive. One of capacitors should be between CP1 and CP2. This will be used to pump up the voltage above VBB. The internal dedicated charge pump requires the following capacitance to have good stability and performance.

Terminal	Min	Typ	Max	Unit
CP1, CP2	0.1	0.2	0.47	µF

A low ESR ceramic capacitor would be suitable for the charge pump.

An additional external capacitor is required for the high-side drive voltage purpose between VBB and VCP terminal. For this capacitor, a low ESR ceramic capacitor is required. The following capacitance value is required.

Terminal	Min	Typ	Max	Unit
VCP	0.1	0.2	0.47	µF

VREG Capacitor: A capacitor is required for the VREG terminal. The VREG internal regulator generates stable DC voltage for various internal use. A good low ESR capacitor is required to suppress a spike current from the device. A tight board layout to the terminals gives the best performance of stability and EMI. The following capacitor is required for the VREG terminal.

Terminal	Min	Typ	Max	Unit
VREG	0.22	–	4.7	µF

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TERMINAL DIAGRAMS

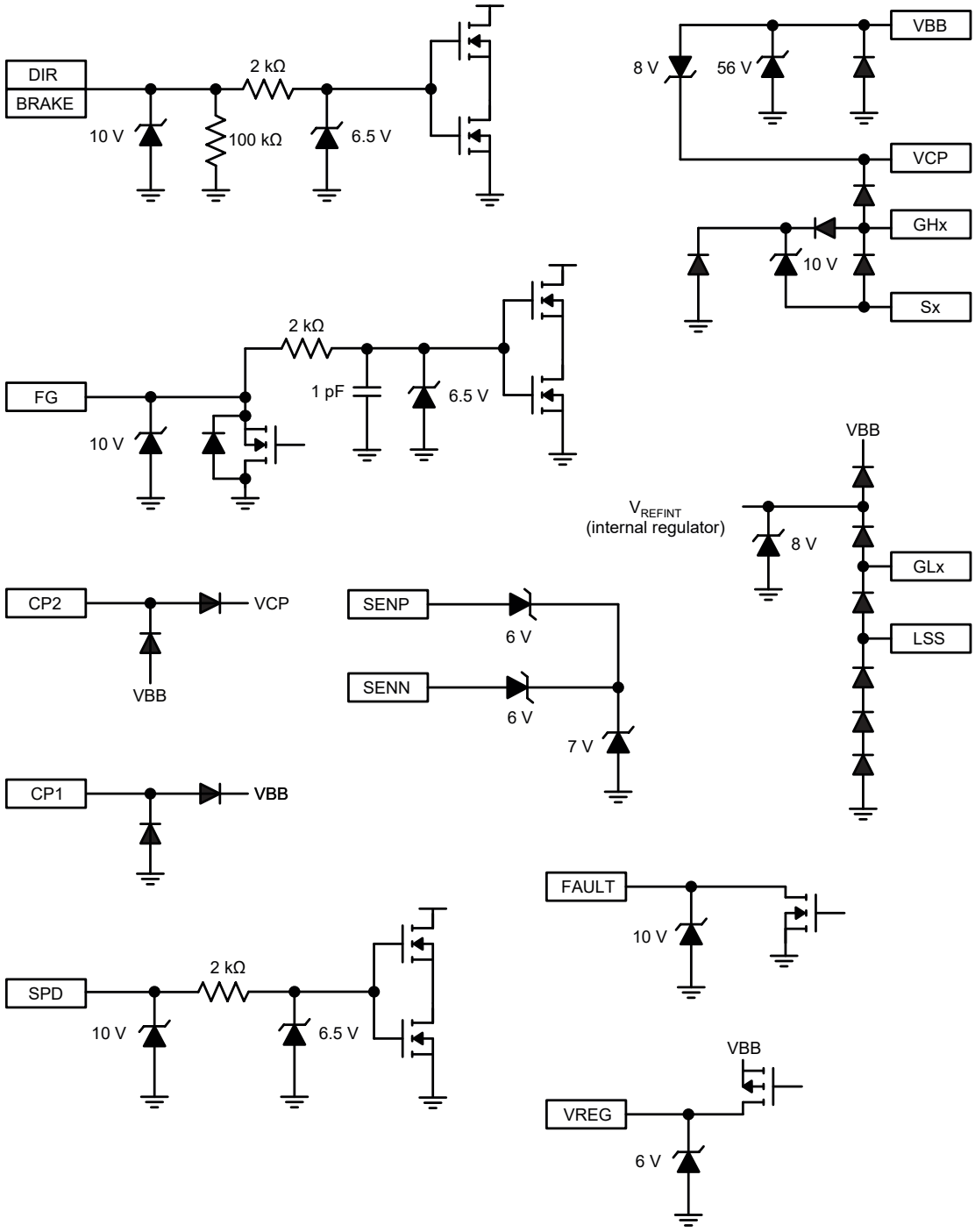

Figure 8: Terminal Diagrams

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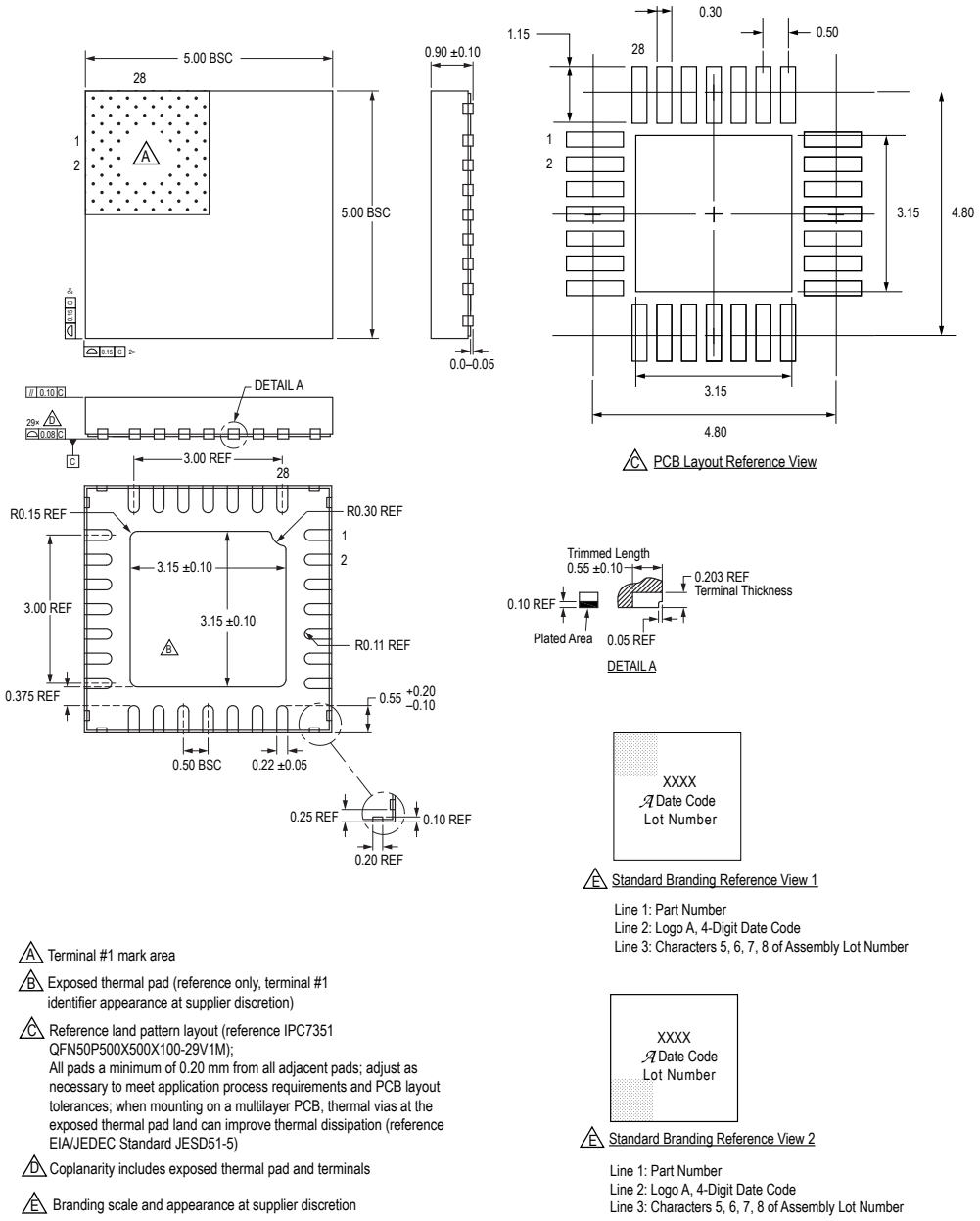
PACKAGE OUTLINE DRAWING

For Reference Only – Not For Tooling Use
(Reference Allegro DWG-0000378, Rev. 3 or JEDEC MO-220VHHD-1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

E Standard Branding Reference View 1

E Standard Branding Reference View 2

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 9: Package ET, 28-Contact QFN with Exposed Pad and Wettable Flank

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Revision History

Number	Date	Description
–	March 15, 2021	Initial release
1	March 16, 2022	Updated package drawing (page 35)
2	May 30, 2023	Updated functional block diagram capacitors (page 4) and minor editorial updates.

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