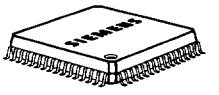
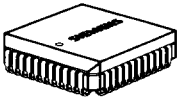
1.2 Features of PEB 2086

Enhanced version of the PEB 2085 with following new features:

- Symmetrical S/T-interface receiver
- B-channel mapping on SSI-interface
- Demultiplexed microprocessor interface in IOM®-1 mode
- Multiframe synchronization



P-MQFP-64-11



P-LCC-44-1

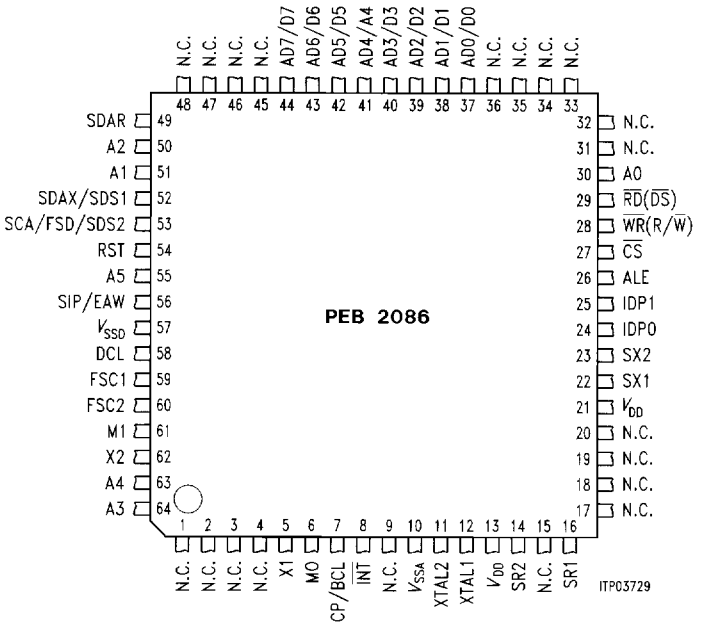
Type	Ordering Code	Package
PEB 2086H	Q67100-H6307	P-MQFP-64-1 (SMD)
PEB 2086N	Q67100-H6356	P-LCC-44-1 (SMD)

The PEB 2086 is an enhanced version of the PEB 2085. The PEB 2086 includes a symmetrical S/T-interface receiver and may use the M-bit of the S/T-interface frame for synchronization purposes.

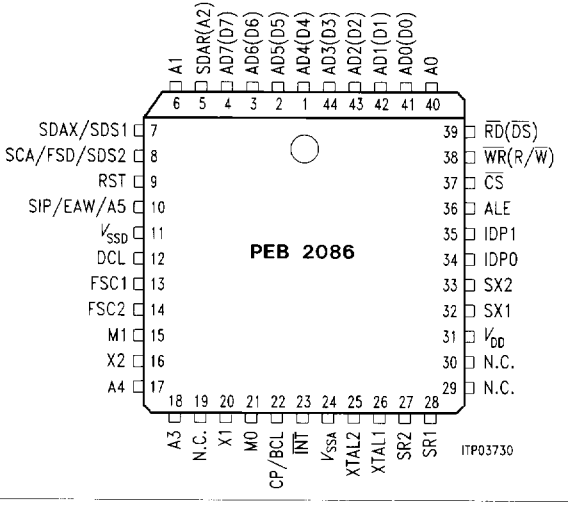
The PEB 2086 is software compatible to the PEB 2085.

Pin Configuration
(top view)

P-MQFP-64



P-LCC-44



1.2.1 Pin Definitions and Functions of PEB 2086

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
37 38 39 40 41 42 43 44	41 42 43 44 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/data bus transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. **Non-Multiplexed Bus Mode**: Data bus. Transfers data between the µP system and the ISAC-S.
27	37	$\overline{CS}$	I	**Chip Select**: A "Low" on this line selects the ISAC-S for a read/write operation.
28	38	R/$\overline{W}$	I	**Read/Write**: When "High" identifies a valid µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
28	38	$\overline{WR}$	I	**Write**: This signal indicates a write operation (Intel bus mode).
29	39	$\overline{DS}$	I	**Data Strobe**: The rising edge marks the end of a valid read or write operation (Motorola bus mode).
29	39	$\overline{RD}$	I	**Read**: This signal indicates a read operation (Intel bus mode).
8	23	INT	OD	**Interrupt Request**: The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
26	36	ALE	I	**Address Latch Enable**: A high on this line indicates an address on the external address bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non-multiplexed).

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
53	8	SCA	O	**Serial Clock Port A**, IOM-1 timing mode 0. A 128-kHz data clock signal for serial port A (SSI).
53	8	FSD	O	**Frame Sync Delayed**, IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1- and B2-channels is guaranteed.
53	8	SDS2	O	**Serial Data Strobe 2**, IOM-2 mode. A programmable strobe signal, selecting either one or two B- or IC-channels on the IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on its function only after a write access to SPCR is made.
54	9	RST	I/O	**Reset**: A "High" on this input forces the ISAC-S into reset state. The minimum pulse length is four DCL-clock periods or four ms. If the terminal specific functions are enabled, the ISAC-S may also supply a reset signal.
59	13	FSC1	I/O	**Frame Sync 1**: LT-S/NT/LT-T: input synchronization signal, IOM-1 and IOM-2 mode. TE: a programmable strobe output, selecting either B1- or B2-channel on the SSI-interface, IOM-1 mode. TE: frame sync output, "High" during channel 0 on the IOM-2 interface, IOM-2 mode.
60	14	FSC2	I/O	**Frame Sync 2**: LT-S/LT-T/NT: input synchronization signal, IOM-1 and IOM-2 mode. TE: programmable strobe output, selecting either B1- or B2-channel on the SSI-interface, IOM-1 mode. TE: Pull-up connection for IDP1, IOM-2 mode.

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
58	12	DCL	I/O	**Data Clock**: Clock of frequency equal to twice the data rate on the IOM-interface LT-S/LT-T: clock input 512-kHz IOM-1 mode 4096-kHz IOM-2 mode TE: clock output 512-kHz IOM-1 mode 1536-kHz IOM-2 mode NT: clock input 512-kHz
30	40	A0	I	**Address Bit 0** (Non-multiplexed bus type).
51	6	A1	I	**Address Bit 1** (Non-multiplexed bus type).
50	5	A2	I	**Address Bit 2** (Non-multiplexed bus type).
49	5	SDAR	I	**Serial Data Port A Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
64	18	A3	I	**Address Bit 3** (Non-multiplexed bus type).
63	17	A4	I	**Address Bit 4** (Non-multiplexed bus type).
55	10	A5	I	**Address Bit 5** (Non-multiplexed bus type).
56	10	SIP	I/O	**SLD Interface Port**, IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels.
56	10	EAW	I	**External Awake** (terminal specific function). If a falling edge on this input is detected, the ISAC-S generates an interrupt and, if enabled, a reset pulse.
52	7	SDAX	O	**Serial Data Port A Transmit**, IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.
52	7	SDS1	O	**Serial Data Strobe 1**, IOM-2 mode. A programmable strobe signal, selecting either one or two B- or IC-channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on its function only after a write access to SPCR is made.
61	15	M1	I	Setting of operating mode.
6	21	M0	I	

Pin Definitions and Functions of PEB 2086 (cont'd)

Pin No. P-MQFP-64	Pin No. P-LCC-44	Symbol	Input (I) Output (O) Open Drain (OD)	Function
62	16	X2	I/O	Mode specific function pins.
5	20	X1	I/O	
7	22	CP	I/O	**Clock Pulses**/Special purpose pin, IOM-1 mode and IOM-2 (except TE) mode.
7	22	BCL	O	**Bit Clock**: Clock of frequency 768 kHz, IOM-2 mode in TE.
57	11	V_{SSD}	–	Digital ground
10	24	V_{SSA}	–	Analog ground
13, 21	31	V_{DD}	–	Power supply (5 V ± 5 %)
12	26	XTAL1	I	Connection for crystal or external clock input.
11	25	XTAL2	O	Connection for external crystal. Left unconnected if external clock is used.
14	27	SR2	I	**S-Bus Receiver Input**
16	28	SR1	I	**S-Bus Receiver Input**
22	32	SX1	O	**S-Bus Transmitter Output** (positive)
23	33	SX2	O	**S-Bus Transmitter Output** (negative)
24	34	IDP0(DD)	I/O	**IOM-Data Port 0 (DD)**
25	35	IDP1(DU)	I/O	**IOM-Data Port 1 (DU)** IOM-1: IDP1:Open-drain with internal pull-up resistor IDP0: Push-pull IOM-2: Open drain without internal pull-up resistor or push-pull (ADF2:ODS)

1.2.2 Logic Symbol of PEB 2086

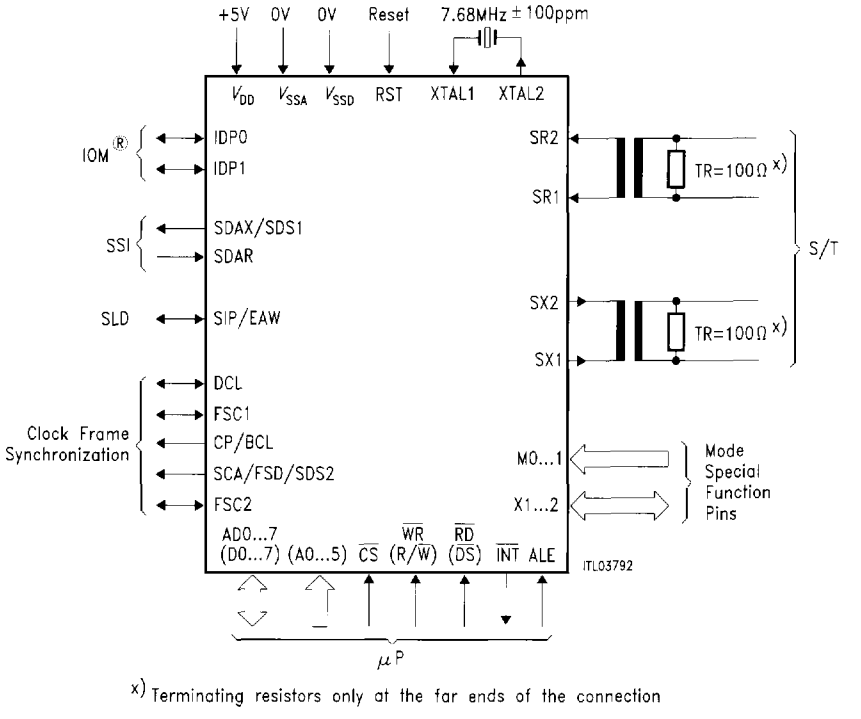


Figure 2
Logic Symbol of the ISAC®-S

1.3 Functional Block Diagram

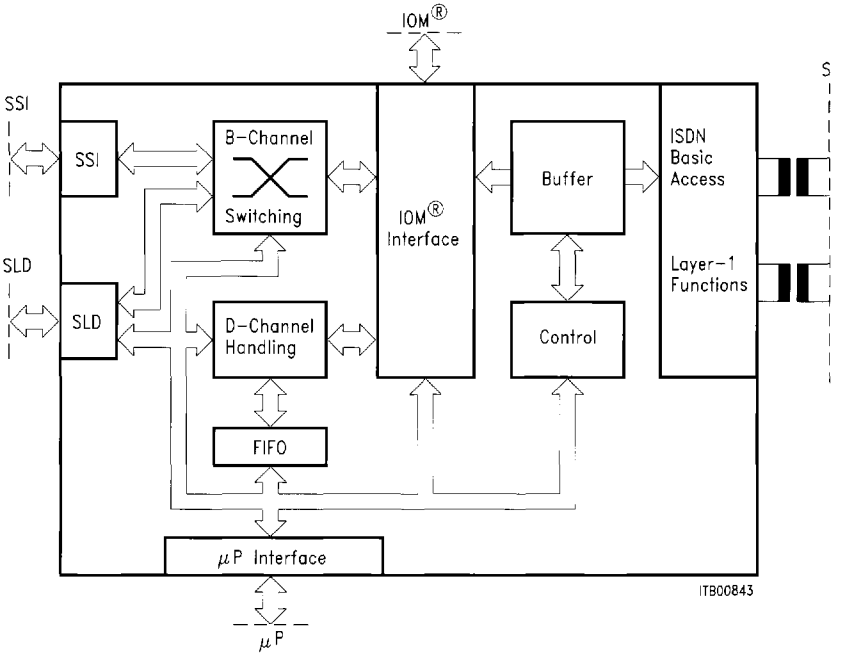


Figure 3
Block Diagram of the ISAC®-S

1.4 System Integration

1.4.1 ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 4.**

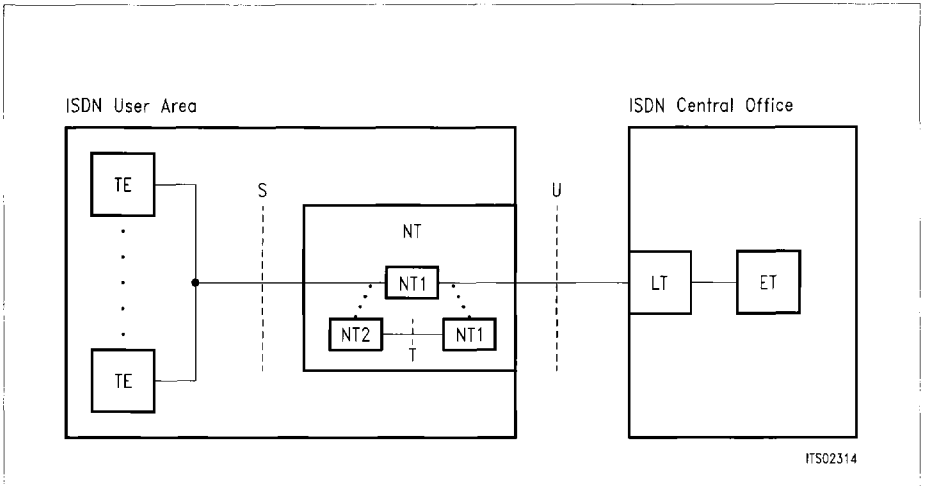


Figure 4
ISDN Basic Subscriber Access Architecture

The NT equipment serves as a converter between the U interface at the exchange and the S interface at the user premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PABX.

The ISAC-S is designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interfaces. **Figure 5** illustrates the general applications of the ISAC-S.

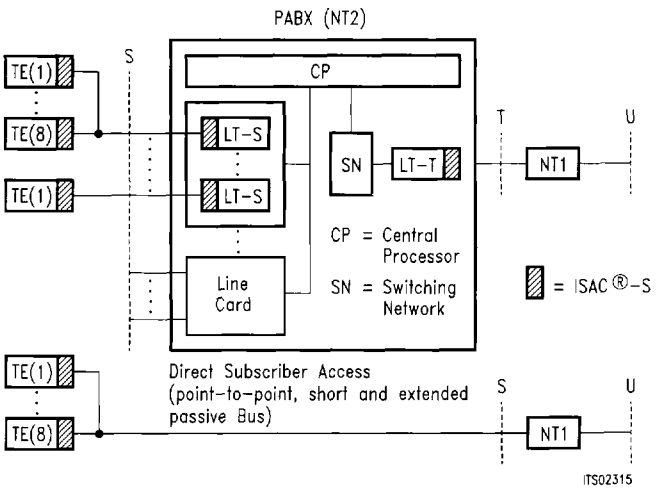


Figure 5
Applications of the ISAC®-S (ISDN Basic Access)

Terminal Applications

The concept of the ISDN basic access is based on two circuit-switched 64 kbit/s B channels and a message oriented 16 kbit/s D channel for packetized data, signaling and telemetry information.

Figure 6 shows an example of an integrated **multifunctional ISDN-S** terminal using the ISAC-S. The ISAC-S provides the interface to the bus and separates the B and D channels.

The D channel, containing signaling data and packet switched data, is processed by the LAPD controller contained in the ISAC-S and routed via a parallel µP interface to the terminal processor. The high level support of the LAPD protocol which is implemented by the ISAC-S allows the use of a low cost processor in cost sensitive applications.

The IOM-2 interface generated by the ISAC-S is used to connect different voice/data (V/D) application modules:

- sources/sinks for the D channel
- sources/sinks for the B1 and B2 channels.

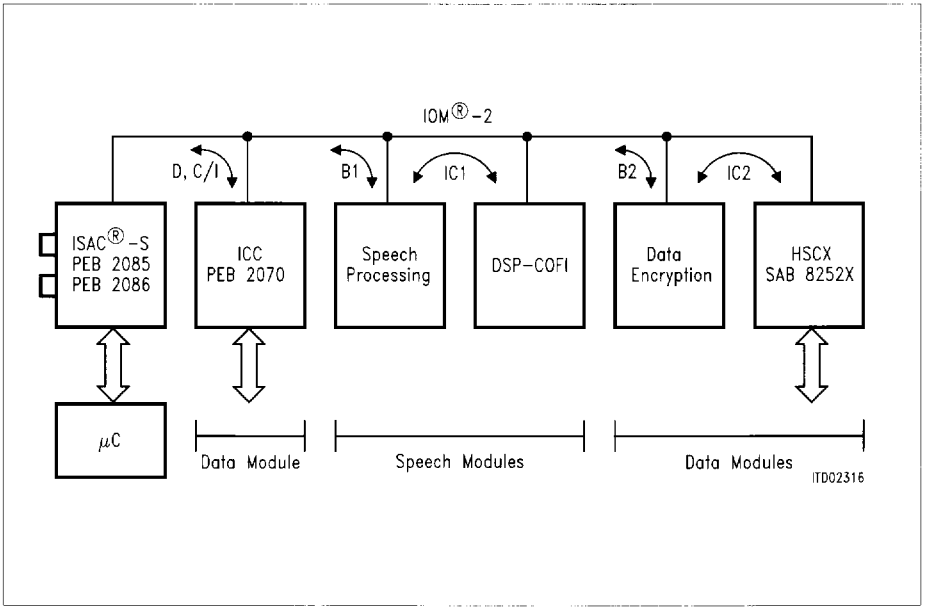


Figure 6
Example of an ISDN®-S Voice/Data Terminal

Up to eight D channel components (ICC: ISDN Communication Controller PEB 2070) may be connected to the D and C/I (Command/Indication) channels (TIC bus). The ISAC-S and ICC handle contention autonomously.

Data transfers between the ISAC-S and the voice/data modules are done with the help of the IOM MONITOR channel protocol. Each V/D module can be accessed by an individual address. The same protocol enables the control of IOM terminal modules and the allocation of intercommunication channels inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 × 64 kbit/s transfer rate between voice/data modules.

In the example above (**figure 6**), one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ISAC-S ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable. **Figure 7** shows the implementation of a basic ISDN feature telephone using the ISAC-S and the Audio Ringing Codec Filter featuring speakerphone (ARCOFI®-SP: PSB 2165).

Line Card Applications

An example of the use of the ISAC-S on an **ISDN PABX line card** (decentralized architecture) is shown in **figure 8**.

The ISAC-S is connected to an Extended PCM Interface Controller (EPIC™ PEB 2055) via an IOM interface.

This interface carries the control and data for up to eight subscribers using time division multiplexing. The ISAC-S's are connected in parallel on the IOM (IDP0 output; IDP1, DCL, FSC1/2 as inputs), one ISAC-S per subscriber.

The EPIC performs dynamic B- and D-channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accommodated.

1.4.2 Microprocessor Environment

The ISAC-S is especially suitable for cost-sensitive applications with single-chip microcontrollers (e.g. 8048, 8031, 8051). However, due to its programmable micro- processor interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$) of the Siemens/Intel non-multiplexed bus type (with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$) or of the Siemens/Intel multiplexed address/data bus type ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE).

An example how to connect the ISAC-S to a Siemens/Intel microcontroller is shown in **figure 9**.

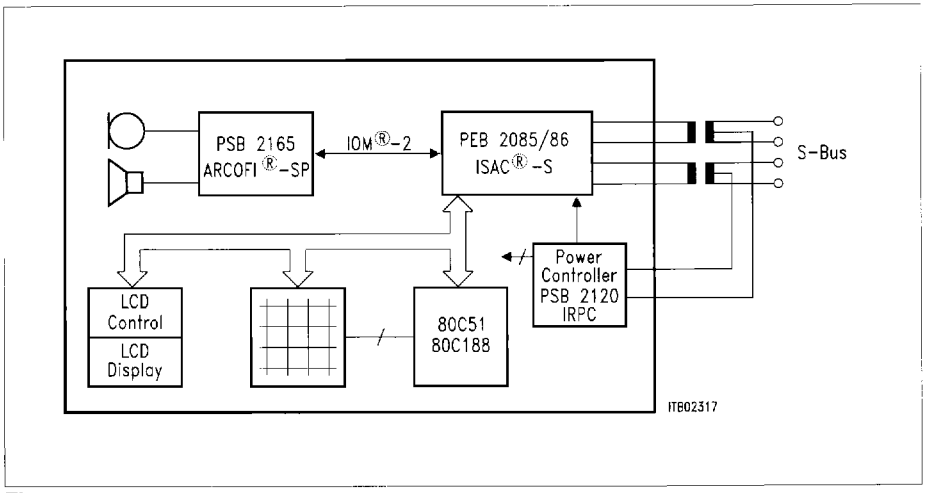


Figure 7
Basic ISDN Feature Telephone

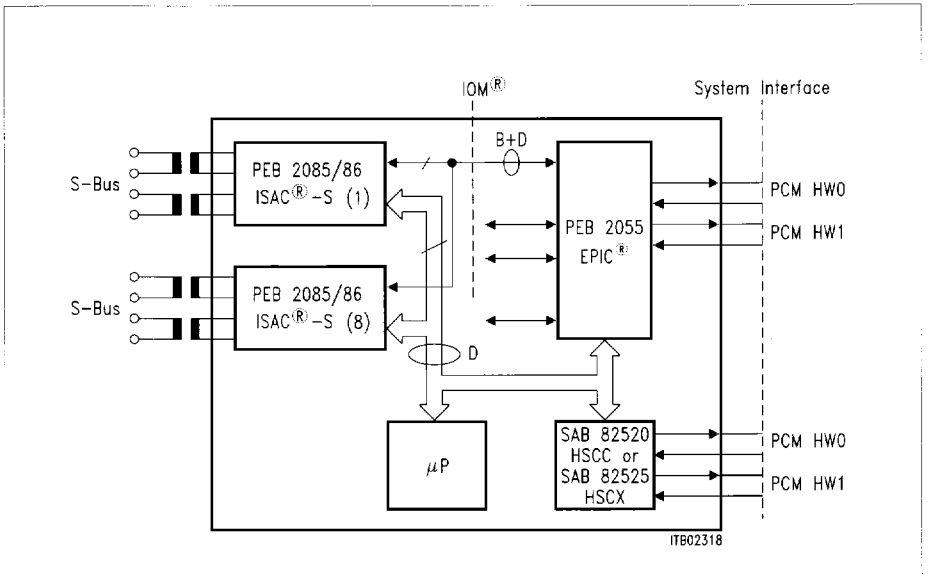


Figure 8
ISDN PABX Line Card Implementation

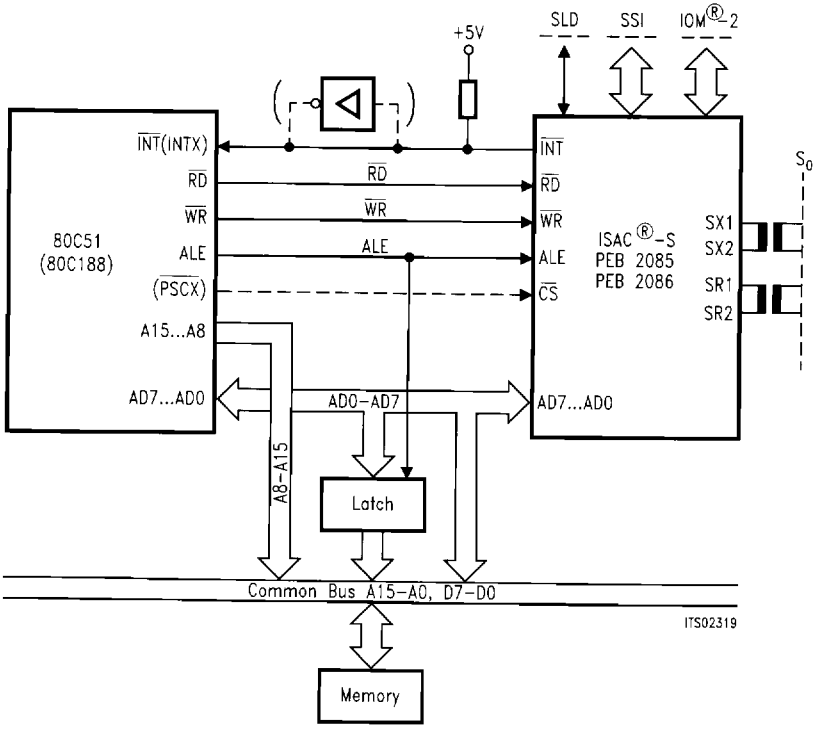


Figure 9
Connecting the ISAC®-S to Siemens/Intel Microcontroller