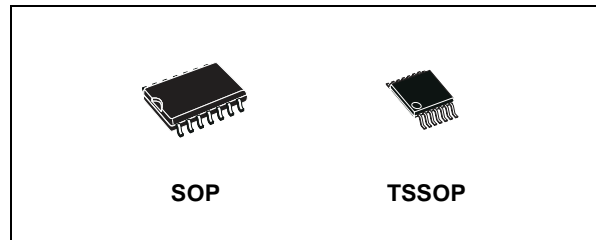




# 74LCX08

## LOW VOLTAGE CMOS QUAD 2-INPUT AND GATE WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED :  
 $t_{PD} = 4.1ns$  (MAX.) at  $V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24mA$  (MIN) at  $V_{CC} = 3V$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(OPR) = 2.0V$  to  $3.6V$  (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 08
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:  
 $HBM > 2000V$  (MIL STD 883 method 3015);  
 $MM > 200V$



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LCX08M	74LCX08MTR
TSSOP		74LCX08TTR

technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

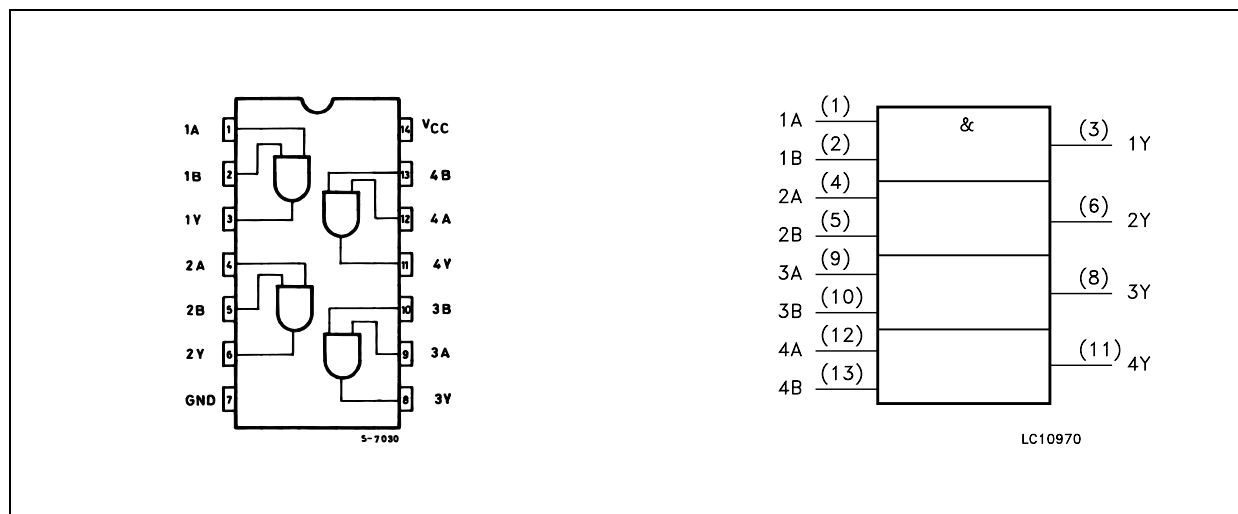
It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

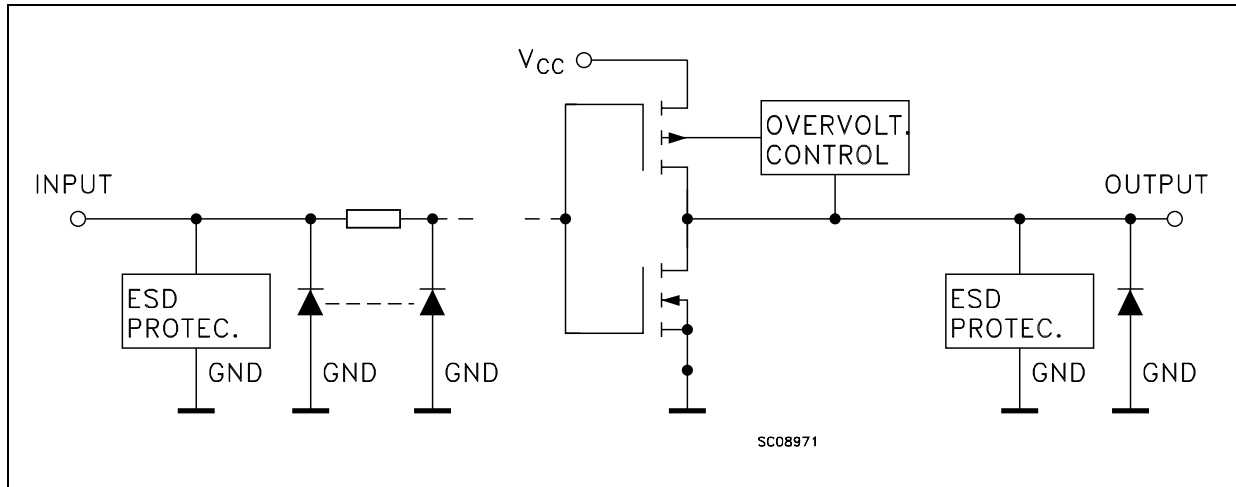
### DESCRIPTION

The 74LCX08 is a low voltage CMOS QUAD 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage (V <sub>CC</sub> = 0V)	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage (High or Low State) (note 1)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	- 50	mA
I <sub>OK</sub>	DC Output Diode Current (note 2)	- 50	mA
I <sub>O</sub>	DC Output Current	± 50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	± 100	mA
I <sub>GND</sub>	DC Ground Current per Supply Pin	± 100	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

- 1) I<sub>O</sub> absolute maximum rating must be observed
- 2) V<sub>O</sub> < GND

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2.0 to 3.6	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage ( $V_{CC} = 0V$ )	0 to 5.5	V
$V_O$	Output Voltage (High or Low State)	0 to $V_{CC}$	V
$I_{OH}, I_{OL}$	High or Low Level Output Current ( $V_{CC} = 3.0$ to $3.6V$ )	$\pm 24$	mA
$I_{OH}, I_{OL}$	High or Low Level Output Current ( $V_{CC} = 2.7V$ )	$\pm 12$	mA
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.5V to 3.6V

2)  $V_{IN}$  from 0.8V to 2V at  $V_{CC} = 3.0V$ 

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		$V_{CC}$ (V)		-40 to 85 $^{\circ}C$		-55 to 125 $^{\circ}C$		
				Min.	Max.	Min.	Max.	
$V_{IH}$	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
$V_{IL}$	Low Level Input Voltage					0.8		0.8
$V_{OH}$	High Level Output Voltage	2.7 to 3.6	$I_O = -100 \mu A$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V
		2.7	$I_O = -12 mA$	2.2		2.2		
		3.0	$I_O = -18 mA$	2.4		2.4		
			$I_O = -24 mA$	2.2		2.2		
$V_{OL}$	Low Level Output Voltage	2.7 to 3.6	$I_O = 100 \mu A$		0.2		0.2	V
		2.7	$I_O = 12 mA$		0.4		0.4	
		3.0	$I_O = 16 mA$		0.4		0.4	
			$I_O = 24 mA$		0.55		0.55	
$I_I$	Input Leakage Current	2.7 to 3.6	$V_I = 0$ to $5.5V$		$\pm 5$		$\pm 5$	$\mu A$
$I_{off}$	Power Off Leakage Current	0	$V_I$ or $V_O = 5.5V$		10		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	2.7 to 3.6	$V_I = V_{CC}$ or GND		10		10	$\mu A$
			$V_I$ or $V_O = 3.6$ to $5.5V$		$\pm 10$		$\pm 10$	
$\Delta I_{CC}$	$I_{CC}$ incr. per Input	2.7 to 3.6	$V_{IH} = V_{CC} - 0.6V$		500		500	$\mu A$

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		$V_{CC}$ (V)		$T_A = 25 \text{ }^{\circ}C$			
				Min.	Typ.	Max.	
$V_{OLP}$	Dynamic Low Level Quiet Output (note 1)	3.3	$C_L = 50pF$ $V_{IL} = 0V, V_{IH} = 3.3V$		0.8		V
$V_{OLV}$					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

**AC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition				Value				Unit
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	R <sub>L</sub> (Ω)	t <sub>s</sub> = t <sub>r</sub> (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time	2.7	50	500	2.5		4.8		4.8	ns
		3.0 to 3.6				1.0	4.1	1.0	4.1	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

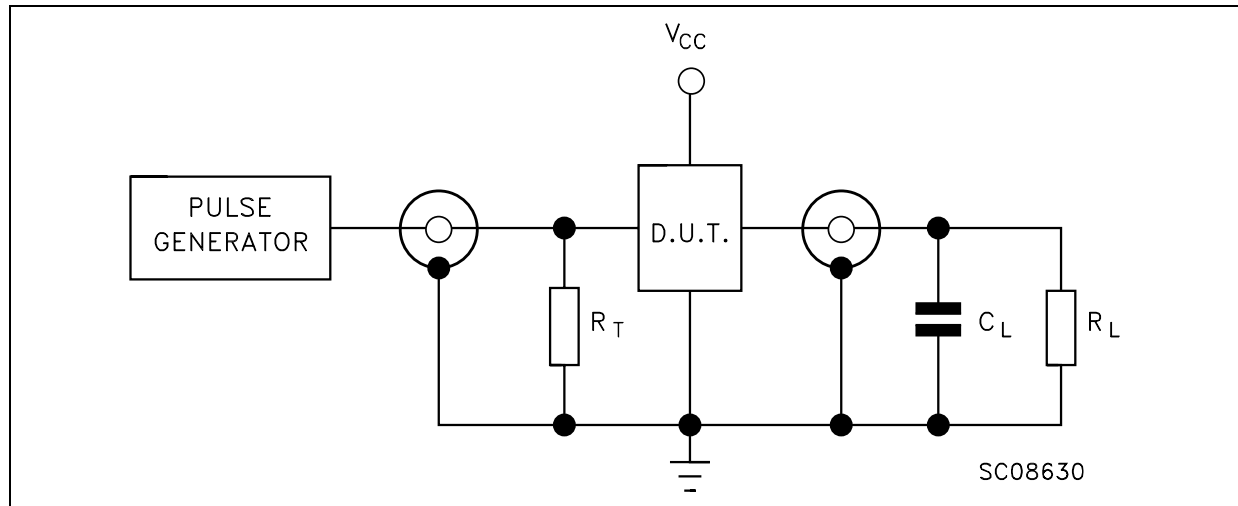
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t<sub>OSLH</sub> = | t<sub>PLHm</sub> - t<sub>PLHn</sub> |, t<sub>OSHL</sub> = | t<sub>PHLm</sub> - t<sub>PHLn</sub> |)  
 2) Parameter guaranteed by design

**CAPACITIVE CHARACTERISTICS**

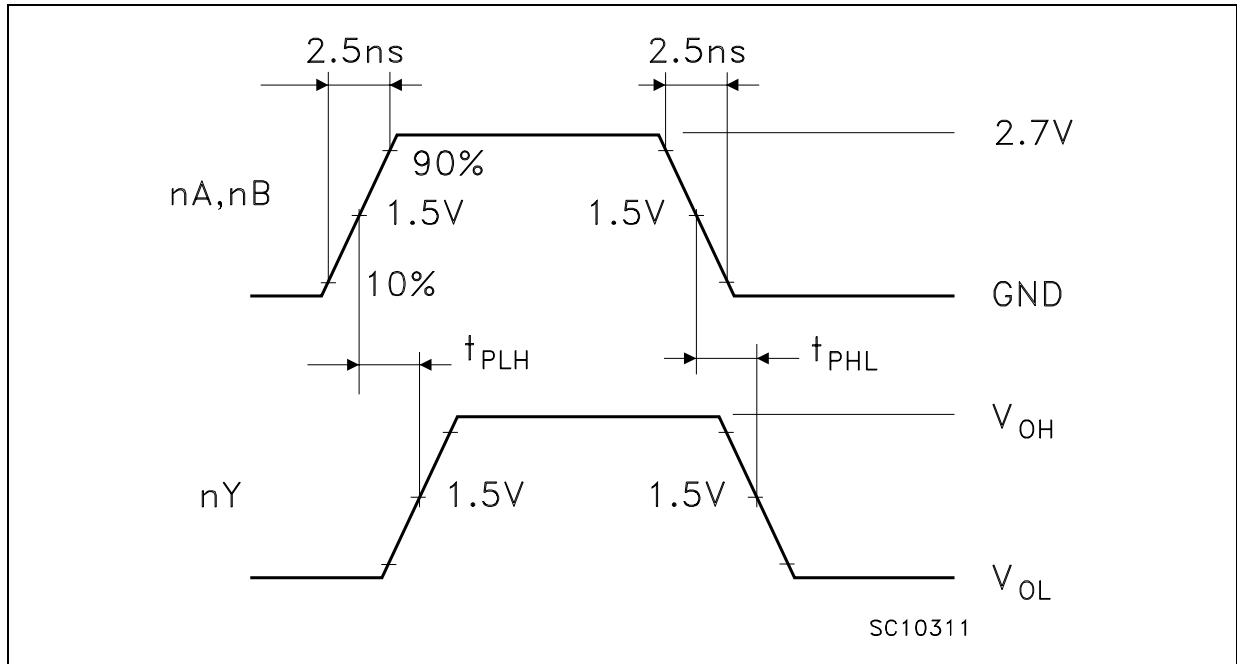
Symbol	Parameter	Test Condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min.	Typ.	Max.	
C <sub>IN</sub>	Input Capacitance	3.3	V <sub>IN</sub> = 0 to V <sub>CC</sub>		6		pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	f <sub>IN</sub> = 10MHz V <sub>IN</sub> = 0 or V <sub>CC</sub>		38		pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/4 (per gate)

**TEST CIRCUIT**

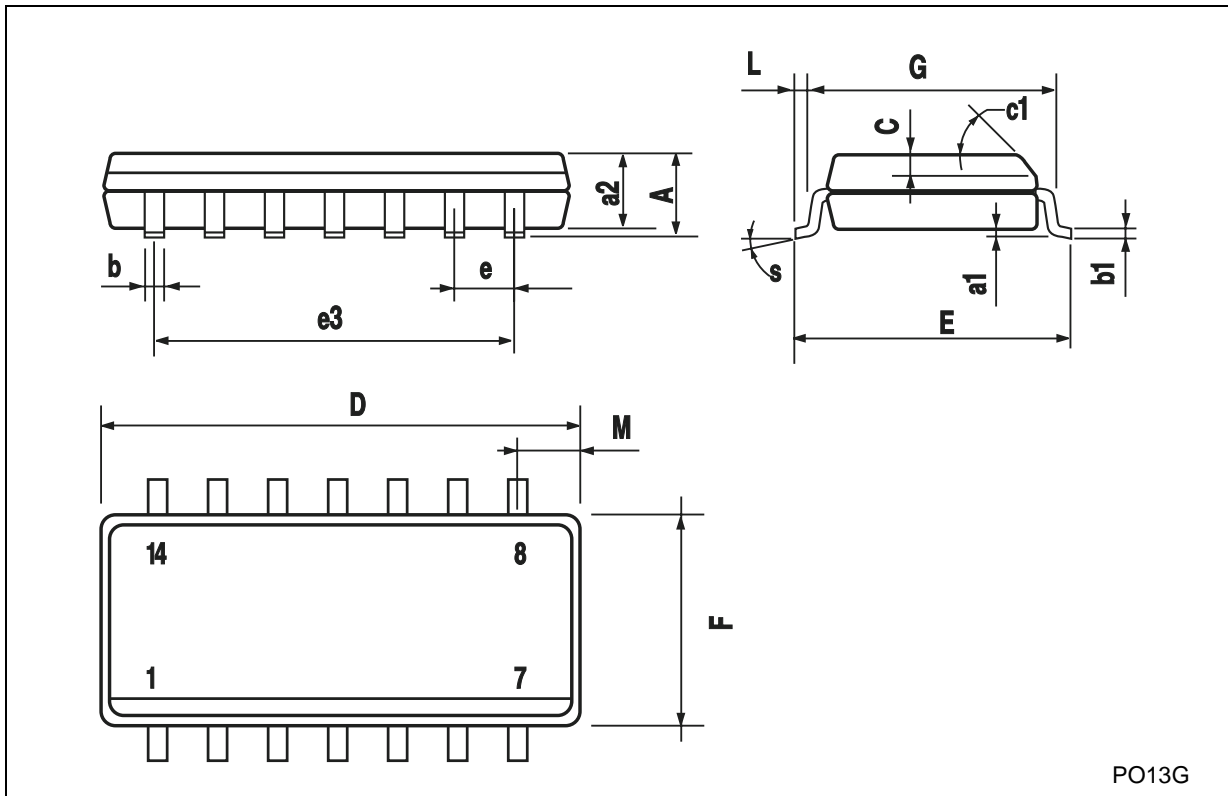


C<sub>L</sub> = 50 pF or equivalent (includes jig and probe capacitance)  
 R<sub>L</sub> = 500Ω or equivalent  
 R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

**WAVEFORM: PROPAGATION DELAY** ( $f=1\text{MHz}$ ; 50% duty cycle)

**SO-14 MECHANICAL DATA**

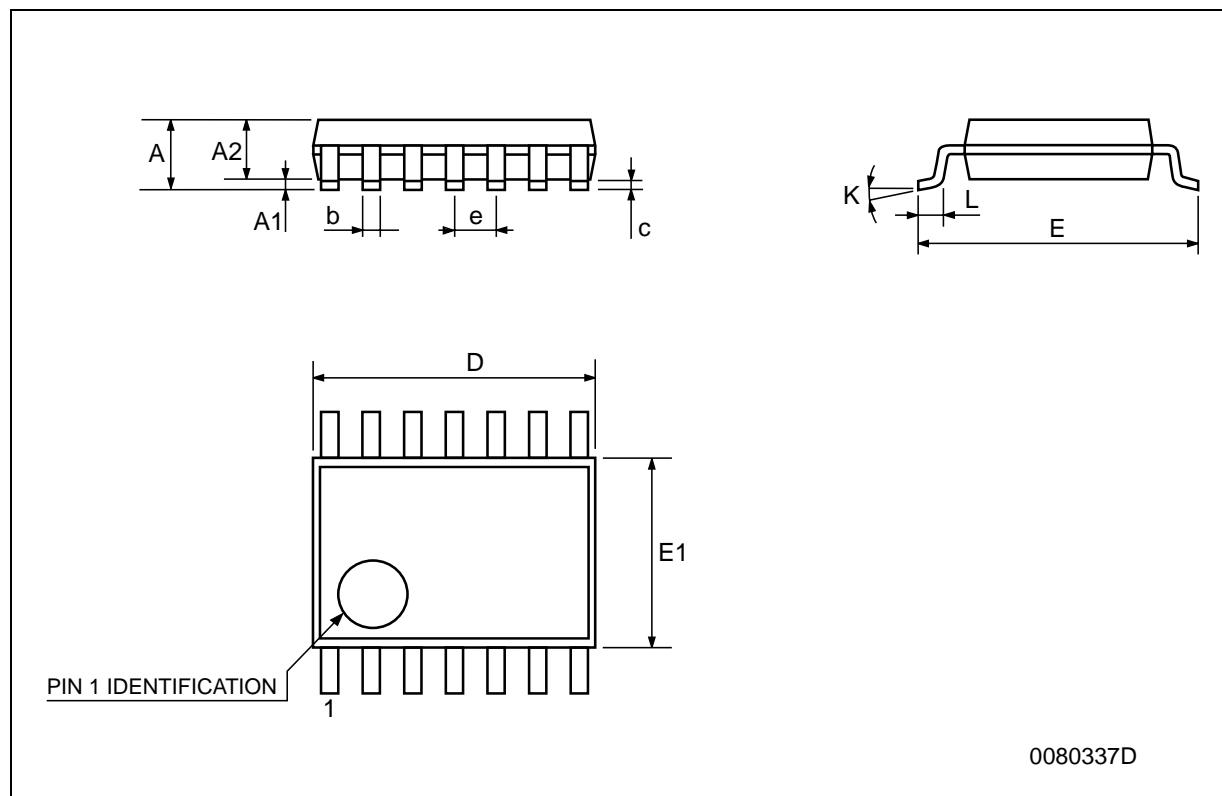
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G

## TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2000 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>