AAT2601B

Total Power Solution for Portable Applications

General Description

The AAT2601B is a member of Skyworks' Total Power Management IC (TPMIC™) product family. It contains a single-cell Lithium Ion/Polymer battery charger, a fully integrated step-down converter and 5 low dropout (LDO) regulators. The device also includes 2 load switches for dynamic power path/sleep mode operation, making it ideal for small handheld portable navigation devices.

The battery charger is a complete thermally regulated constant current/constant voltage linear charger. It includes an integrated pass device, reverse blocking protection, high accuracy current and voltage regulation, charge status, and charge termination. The charging current, charge termination current, and recharge voltage are programmable with an external resistor and/or by a standard I²C interface.

The step-down DC/DC converter is integrated with internal compensation and operates at a switching frequency of 1.5MHz, thus minimizing the size of external components while keeping switching losses low and efficiency greater than 92%.

The five LDOs offer 60dB power supply rejection ratio (PSRR) and low noise operation making them suitable for powering noise-sensitive loads.

All six voltage regulators operate with low quiescent current. The total no load current when the step-down converter and 2 LDOs are enabled is only 170μA.

The AAT2601B is available in a thermally enhanced low profile 5x5x0.75mm 36-pin TQFN package.

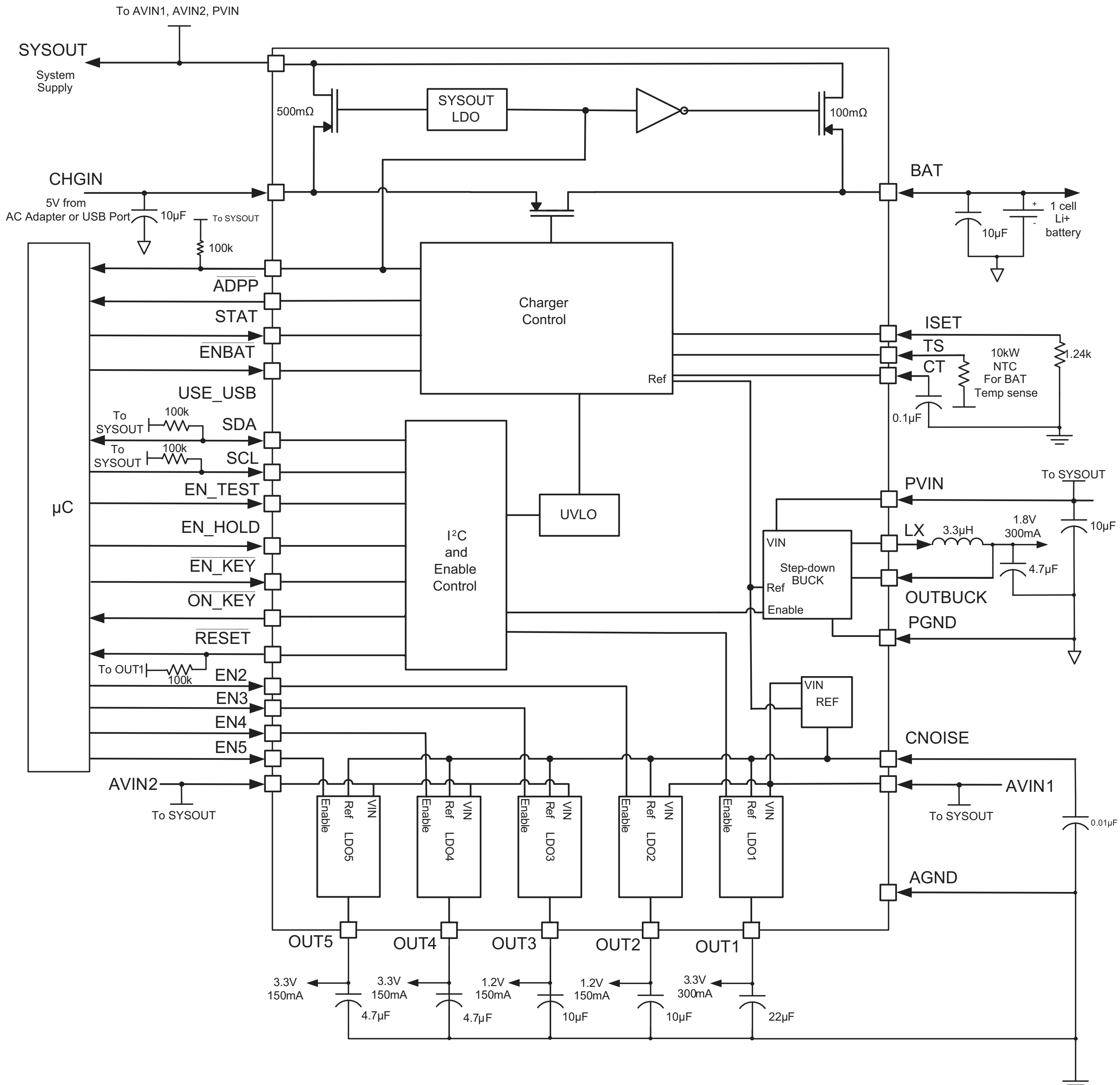
Features

- Voltage Regulator V_{IN} Range: 4.5V to 6V
- Complete Power Integration
  - Integrated Load Switches to Power Converters from AC Adapter or Battery Automatically
- Low Standby Current
  - 170μA (typ) w/ Buck, LDO1, and LDO2 Active, No Load
- One Step-Down Buck Converter
  - 1.8V, 300mA Output
  - 1.5MHz Switching Frequency
  - Fast Turn-On Time (100μs typ)
- Five LDOs Programmable with I²C
  - LDO1: 3.3V, 300mA Programmable with I²C
  - LDO2: 1.2V, 150mA
  - LDO3: 1.2V, 150mA
  - LDO4: 3.3V, 150mA Programmable with I²C
  - LDO5: 3.3V, 150mA Programmable with I²C
  - PSRR: 60dB@10kHz
  - Noise: 50μVrms for LDO3, LDO4, and LDO5
- One Battery Charger
  - Digitized Thermal Regulation
  - Charge Current Programming up to 1.4A
  - Charge Current Termination Programming
  - Automatic Trickle Charge for Battery Preconditioning (2.8V Cutoff)
- Adapter OK ($\overline{\text{ADPP}}$) and Reset ($\overline{\text{RESET}}$) Timer Outputs
- Separate Enable Pins for Supply Outputs
- Over-Current Protection
- Over-Temperature Protection
- 5x5mm TQFN55-36 Package

Applications

- Digital Cameras
- GPS and PND
- Handheld Instruments
- PDAs and Handheld Computers
- Portable Media Players

Typical Application

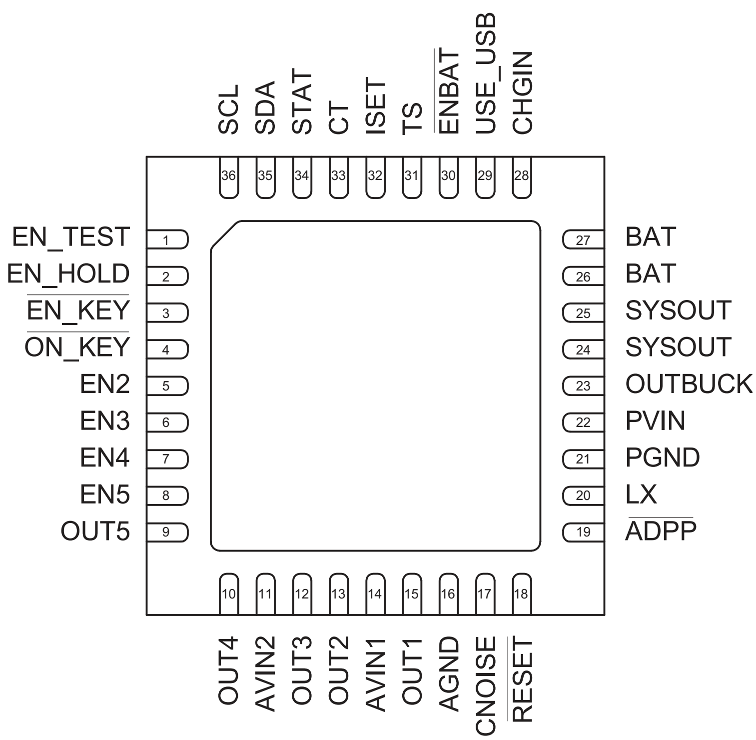


Pin Descriptions

Pin #	Symbol	Function
1	EN_TEST	Similar to EN_HOLD but intended for use with the automatic tester or as a hands free enable input pin indicating hands free phone operation with a headset. It is also internally pulled to GND when floating.
2	EN_HOLD	Enable for the system. EN_HOLD must be held high by the processor to maintain core power. It is internally pulled to GND when floating.
3	$\overline{\text{EN\_KEY}}$	Enable for the system. An internal pull-up resistor keeps the pin pulled up to an internal supply to keep the system off when there is no CHGIN input. Connect a normally-open pushbutton switch from this pin to GND. There is an internal 300ms debounce delay circuit to filter noise.
4	$\overline{\text{ON\_KEY}}$	Buffered logic output of the $\overline{\text{EN\_KEY}}$ pin with a logic signal from ground to OUT1.
5	EN2	Enable for LDO2 (Internally pulled low when floating).
6	EN3	Enable for LDO3 (Internally pulled low when floating).
7	EN4	Enable for LDO4 (Internally pulled low when floating).
8	EN5	Enable for LDO5 (Internally pulled low when floating).
9	OUT5	Output for LDO5 (when shut down, pulled down with 10kΩ)
10	OUT4	Output for LDO4 (when shut down, pulled down with 10kΩ)
11	AVIN2	Analog voltage input. Must be tied to SYSOUT on the PCB.
12	OUT3	Output for LDO3.
13	OUT2	Output for LDO2.
14	AVIN1	Analog voltage input. Must be tied to SYSOUT on the PCB.
15	OUT1	Output for LDO1.
16	AGND	Signal ground.
17	CNOISE	Noise Bypass pin for the internal reference voltage. Connect a 0.01µF capacitor to AGND.
18	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is the open drain output of a 50ms reset timer. $\overline{\text{RESET}}$ is released after the 50ms timer times out. $\overline{\text{RESET}}$ is active low and is held low during shutdown. $\overline{\text{RESET}}$ should be tied to a 10K or larger pullup to OUTBUCK.
19	$\overline{\text{ADPP}}$	Open Drain output. Will pull low when V_{CHGIN} > 4.5V. When this happens, depending on the status of the USE_USB pin, the charge current will be reset to the default values (see Battery Charger and I²C Serial Interface and Programmability section)
20	LX	Step-down Buck converter switching node. Connect an inductor between this pin and the output.
21	PGND	Power Ground for step-down Buck converter.
22	PVIN	Input power for step-down Buck converter. Must be tied to SYSOUT.
23	OUTBUCK	Feedback input for the step-down Buck converter.
24, 25	SYSOUT	System Power output. Connect to the input voltage pins PIN, AVIN1/2 for the step-down converter and LDOs and other external supply requirements.
26, 27	BAT	Connect to a Lithium Ion battery.
28	CHGIN	Power input from either external adapter or USB port.
29	USE_USB	When pulled high, fast charge current is set to 100mA regardless of the resistor value present on the ISET pin. Additionally, the CHGIN-SYSOUT LDO will be disabled and the BAT-SYSOUT load switch will be enabled.
30	$\overline{\text{ENBAT}}$	Active low enable for the battery charger (Internally pulled low when floating)
31	TS	Battery Temperature Sense pin with 75µA output current. Connect the battery's NTC resistor to this pin and ground.
32	ISET	Charge current programming input pin (Tie a 1.24k to GND for 800mA fast charge current). Can be used to monitor charge current.
33	CT	Charger Safety Timer Pin. A 0.1µF ceramic capacitor should be connected between this pin and GND. Connect directly to GND to disable the timer function.
34	STAT	Battery charging status pin output. Connected internally between GND and OUT1. Used to monitor battery charge status.
35	SDA	I²C serial data pin, open drain; requires a pullup resistor.
36	SCL	I²C serial clock pin, open drain; requires a pullup resistor.
EP	EP	The exposed thermal pad (EP) must be connected to board ground plane and pins 16 and 21. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline).

Pin Configuration

TQFN55-36
(Top View)



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Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
V_{IN}	Input Voltage, CHGIN, BAT	-0.3 to 6.5	V
Power and logic pins	Maximum Rating	V_{IN} + 0.3	V
T_A	Operating Junction Temperature Range	-40 to 85	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Recommended Operating Conditions[2]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	25	°C/W
P_D	Maximum Power Dissipation	4	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Thermal Resistance was measured with the AAT2601B device on the 4-layer FR4 evaluation board in a thermal oven. The amount of power dissipation which will cause the thermal shutdown to activate will depend on the ambient temperature and the PC board layout ability to dissipate the heat. See Figures 11-14.

Electrical Characteristics[1]

V_{IN} = 5V, V_{BAT} = 3.6V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	CHGIN Input Voltage		4.5		6	V
I_Q	Battery Standby Current	Buck, LDO1 + LDO2, no load		170		μA
I_{SHDN}	Battery Shutdown Current	EN_TEST, EN_HOLD, EN2, EN3, EN4, EN5 = GND, $\overline{EN\_KEY}$ floating			10.0	μA
UVLO	Under-Voltage Lockout for CHGIN	CHGIN rising		4.25	4.5	V
		CHGIN falling		4.15		V
	Battery Under-Voltage Lockout	BAT rising		2.6		V
		BAT falling		2.35		V
I_{BAT}	Leakage Current from BAT Pin	V_{BAT} = 4V, V_{CHGIN} = 0V		2	5	μA
Startup Timers						
$\overline{RESET}$	Reset Timer	Initiated when OUT1 = 90% of final value	35			ms
Charger Voltage Regulation						
V_{BAT_REG}	Output Charge Voltage Regulation	0°C ≤ T_A ≤ +70°C	4.158	4.200	4.242	V
V_{MIN}	Preconditioning Voltage Threshold	(No trickle charge option available)	2.6	2.8	3.0	V
V_{RCH}	Battery Recharge Voltage Threshold	I^2C Recharge Code = 00 (default)		4.00		V
		I^2C Recharge Code = 01		4.05		V
		I^2C Recharge Code = 10		4.10		V
		I^2C Recharge Code = 11		4.15		V
Charger Current Regulation						
I_{CH_CC}	Constant-Current Mode Charge Current	R_{ISET} = 1.24k (for 0.8A), USE_USB = Low, I^2C ISET code = 000, V_{BAT} = 3.6V, V_{CHGIN} = 5.0V	720	800	880	mA
		USE_USB = High, I^2C ISET Code = 000, V_{BAT} = 3.6V	85	100	115	
KI_SET	Charge Current Set Factor: I_{CH_CC}/I_{ISET}	Constant Current Mode, V_{BAT} = 3.6V		800		mA/mA
I_{CH_PRE}	Preconditioning Charge Current	R_{ISET} = 1.24kΩ, USE_USB = Low		12		% I_{CH_CC}
		I^2C ISET Code = 000, USE_USB = High		50		mA
I_{CH_TERM}	Charge Termination Threshold Current	I^2C Term Code = 00 (default)		5		% I_{CH_CC}
		I^2C Term Code = 01		10		
		I^2C Term Code = 10		15		
		I^2C Term Code = 11		20		
Charging Devices						
$R_{DS(ON)}$	Charging Transistor ON Resistance	V_{IN} = 5V		0.6	0.9	Ω
Logic Control / Protection						
V_{EN_HOLD}, $V_{\overline{EN\_KEY}}$, V_{EN_TEST}	Input High Threshold		1.4			V
	Input Low Threshold				0.4	V
$V_{\overline{ADPP}}$	Output Low Voltage	Pin Sinks 4mA			0.4	V
$I_{\overline{ADPP}}$	Output Pin Current Sink Capability				8	mA
V_{STAT}	Output High Voltage				V_{OUT1}	V
I_{STAT}	Output Pin Current Source Capability				1.5	mA
V_{OVP}	Over-Voltage Protection Threshold			4.3		V

1. Specification over the –40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

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Electrical Characteristics[1]

V_{IN} = 5V, V_{BAT} = 3.6V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Logic Control / Protection (continued)						
V_{OCP}	Over Current Protection Threshold			105		%V_{CS}
T_C	Constant Current Mode Time Out	C_{CT} = 100nF, V_{CHGIN} = 5V		3		Hours
T_K	Trickle Charge Time Out	C_{CT} = 100nF, V_{CHGIN} = 5V		T_C/8		Hours
T_V	Constant Voltage Mode Time Out	C_{CT} = 100nF, V_{CHGIN} = 5V		3		Hours
I_{TS}	Current Source from TS Pin		71	75	79	µA
TS_1	TS Hot Temperature Fault	Falling Threshold	318	331	346	mV
		Hysteresis		25		mV
TS_2	TS Cold Temperature Fault	Rising Threshold	2.30	2.39	2.48	V
		Hysteresis		25		mV
T_{LOOP_IN}	Thermal Loop Entering Threshold			115		°C
T_{LOOP_OUT}	Thermal Loop Exiting Threshold			85		°C
T_{REG}	Thermal Loop Regulation			100		°C
Load Switches / SYSOUT LDO						
$R_{DS(ON),BAT-SYSOUT}$	On-Resistance of BAT-SYSOUT Load Switch	V_{BAT} = 3.6V		100	150	mΩ
$R_{DS(ON),CHGIN-SYSOUT}$	On-Resistance of CHGIN-SYSOUT Load Switch	V_{CHGIN} = 4.5V		0.5	0.75	Ω
	Sysout LDO Input Voltage Range		4.5			V
	Sysout LDO Output Voltage	I_{SYSOUT} < 900mA, V_{CHGIN} = 4.5V ~ 6.0V	3.4	3.9	4.2	V
Step-Down Buck Converter						
$V_{OUTBUCK}$	Output Voltage Accuracy	$I_{OUTBUCK}$ = 0 ~ 300mA; V_{IN} = 2.7V ~ 5.5V	1.71	1.80	1.89	V
$I_{LIMOUTBUCK}$	P-Channel Current Limit			0.8		A
$R_{DS(ON)L}$	High Side Switch On-Resistance			0.8		Ω
$R_{DS(ON)H}$	Low Side Switch On-Resistance			0.8		Ω
F_{OSC}	Oscillator Frequency	T_A = 25°C		1.5		MHz
T_S	Start-Up Time	From Enable to Regulation; $C_{OUTBUCK}$ = 4.7µF, C_{NOISE} = On		100		µs
LDO1 (3.3V)						
V_{OUT1}	Output Voltage Accuracy	AV_{IN} = 3.7V to 4.2V, I_{OUT1} = 1mA ~ 300mA	-3		+3	%
I_{OUT1}	Output Current		300			mA
I_{LIM1}	Output Current Limit			1000		mA
V_{DO1}	Dropout Voltage	I_{OUT1} = 300mA		160	320	mV
$\Delta V_{OUT1}(V_{OUT1}\Delta V_{IN1})$	Line Regulation	I_{OUT1} = 100mA		0.07		%/V
ΔV_{OUT1}	Load Regulation	I_{OUT1} = 0.5mA ~ 150mA		40		mV
PSRR	Power Supply Rejection Ratio	I_{OUT1} = 10mA, C_{OUT1}=22µF, 100Hz ~ 10KHz		60		dB
T_S	Start Up Time	From Enable to Regulation; C_{OUT1} = 22µF, C_{NOISE} = On		175		µs

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Electrical Characteristics[1]

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Symbol	Description	Conditions	Min	Typ	Max	Units
LDO2, LDO3 (1.2V)						
V_{OUT2}	Output Voltage Accuracy	AV_{IN} = 2.7V to 4.2V, I_{OUTX} = 1mA ~ 150mA	-3		+3	%
I_{OUT2}	Output Current		150			mA
I_{LIM2}	Output Current Limit			1000		mA
V_{DO2}	Dropout Voltage	I_{OUT2} = 150mA		150		mV
ΔV_{OUT2}/ ($V_{OUT2}\Delta V_{IN2}$)	Line Regulation	I_{OUT2} = 100mA, 3.3V<V_{AVINx}<5.5V		0.07		%/V
ΔV_{OUT2}	Load Regulation	Load: 0.5mA~150mA		14		mV
PSRR	Power Supply Rejection Ratio	I_{OUT2} = 10mA, C_{OUT2} = 4.7μF, 10 ~ 10KHz		60		dB
Ts	Start Up Time	From Enable to Regulation; C_{OUT2} = 4.7μF, C_{NOISE} = On		65		μs
LDO4, LDO5 (3.3V)						
V_{OUTx}	Output Voltage Accuracy	AV_{IN} = 3.7V to 4.2V, I_{OUTX} = 1mA ~ 150mA	-3		+3	%
I_{OUTx}	Output Current		150			mA
I_{LIMx}	Output Current Limit			1000		mA
V_{DOx}	Dropout Voltage	I_{OUTX} = 150mA		165		mV
ΔV_{OUTx}/ ($V_{OUTx}\Delta V_{INx}$)	Line Regulation	I_{OUTX} = 100mA, 3.3V < V_{AVINx} < 5.5V		0.07		%/V
ΔV_{OUTx}	Load Regulation	I_{OUTX} = 0.5mA ~ 150mA		40		mV
PSRR	Power Supply Rejection Ratio	I_{OUTX} = 10mA, C_{OUTx} = 4.7μF, 10 ~ 10KHz		60		dB
e_N	Output Noise Voltage	I_{OUTX} = 10mA, Power BW: 10kHz ~ 100KHz		40		μVrms
Ts	Start Up Time	From Enable to Regulation; C_{OUTX} = 4.7μF, C_{NOISE} = On		65		μs
Logic Control						
V_{IH}	Enable Pin Logic High Level	For EN2, EN3, EN4 and EN5	1.4			V
V_{IL}	Enable Pin Logic Low Level				0.4	V
Thermal						
T_{SD}	Over Temperature Shutdown Threshold			140		°C
T_{HYS}	Over Temperature Shutdown Hysteresis			15		°C
SCL, SDA (I^2C Interface)						
F_{SCL}	Clock Frequency		0		400	KHz
T_{LOW}	Clock Low Period		1.3			μs
T_{HIGH}	Clock High Period		0.6			μs
T_{HD_STA}	Hold Time START Condition		0.6			μs
T_{SU_STA}	Setup Time for Repeat START		0.6			μs
T_{SU_DTA}	Data Setup Time		100			ns
T_{SU_STO}	Setup Time for STOP Condition		0.6			μs
T_{BUF}	Bus Free Time Between STOP and START Condition		1.3			μs
V_{IL}	Input Threshold Low	2.7V ≤ V_{IN} ≤ 5.5V			0.4	V
V_{IH}	Input Threshold High	2.7V ≤ V_{IN} ≤ 5.5V	1.4		-	V
I_I	Input Current		-1.0		1.0	μA
V_{OL}	Output Logic Low (SDA)	I_{PULLUP} = 3mA			0.4	V

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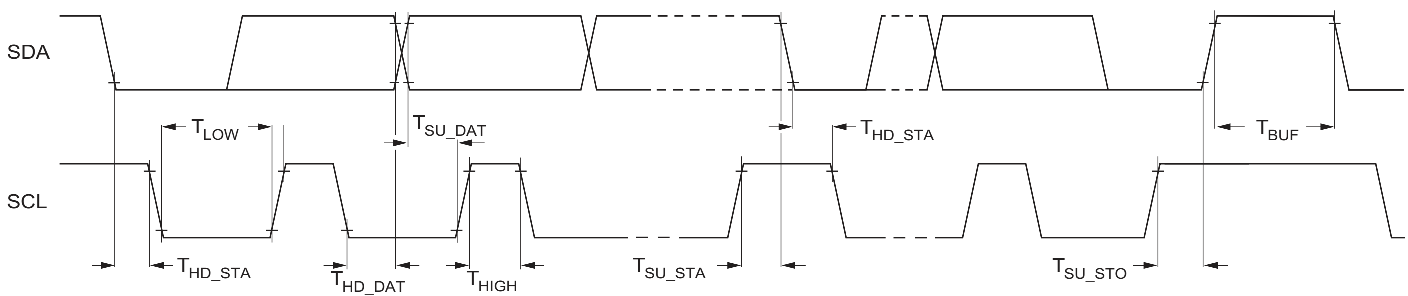
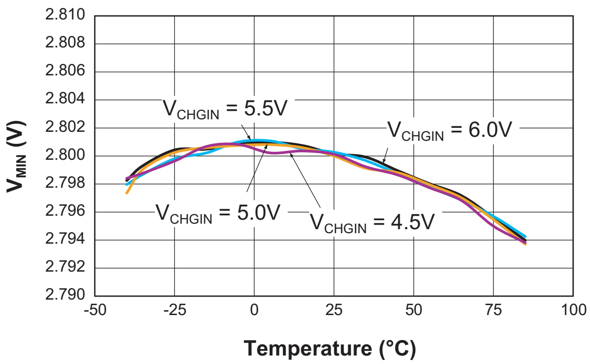
Basic I²C Timing Diagram

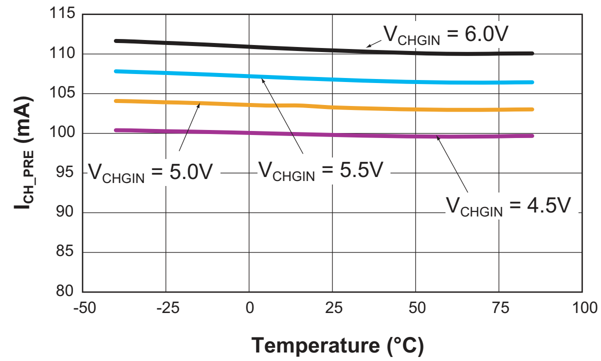


Typical Characteristics—Charger

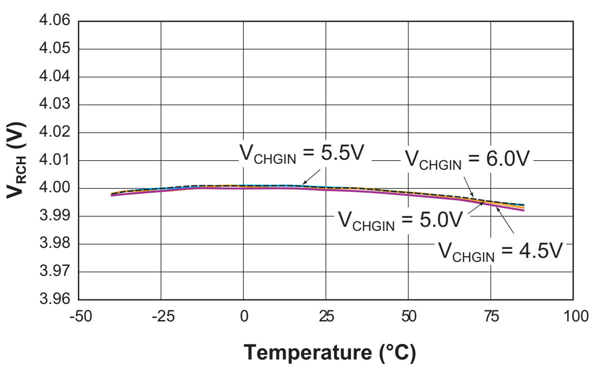
Preconditioning Threshold Voltage vs. Temperature



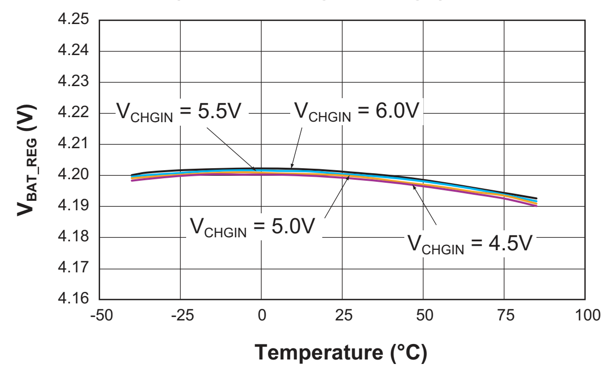
Preconditioning Charge Current vs. Temperature
(V_{BAT} = 2.5V, R_{ISET} = 1.24kΩ)



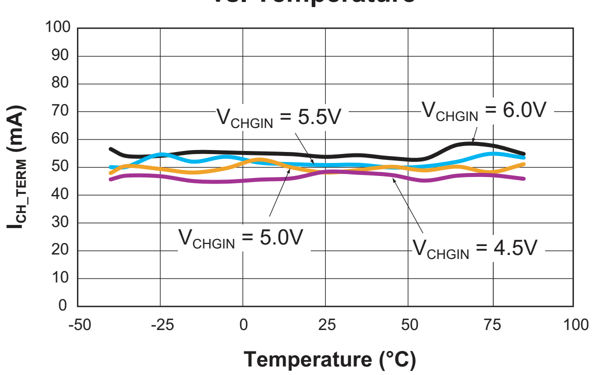
Recharge Voltage Threshold vs. Temperature
(V_{RCH} set to 4.0V)



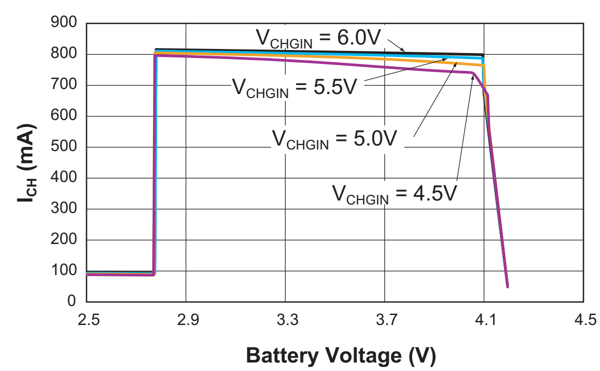
Output Charge Voltage Regulation vs. Temperature (End of Charge Voltage)



Charge Termination Threshold Current vs. Temperature

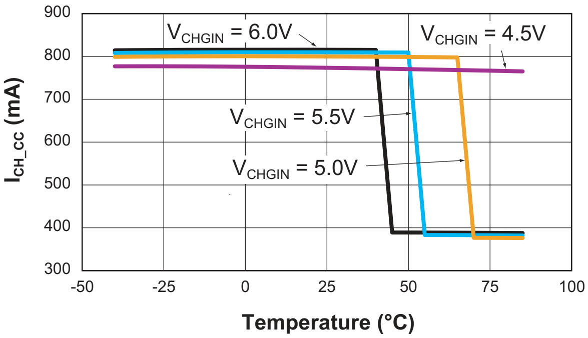


Charging Current vs. Battery Voltage
(R_{ISET} = 1.24kΩ)

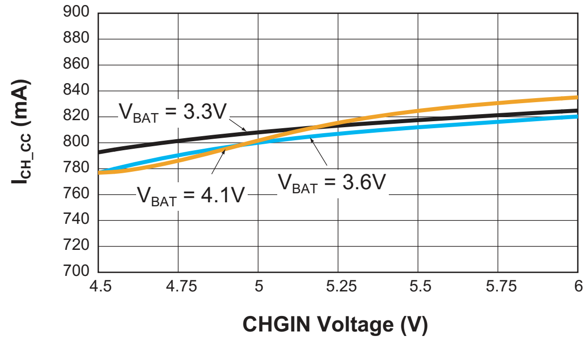


Typical Characteristics—Charger (continued)

Constant Current Mode Charge Current vs. Temperature
(V_{BAT} = 3.6V; R_{ISET} = 1.24kΩ)

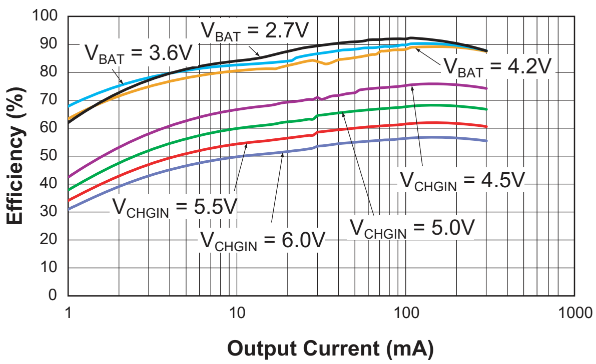


Constant Current Mode Charge Current vs. Input Voltage
(R_{ISET} = 1.24kΩ)

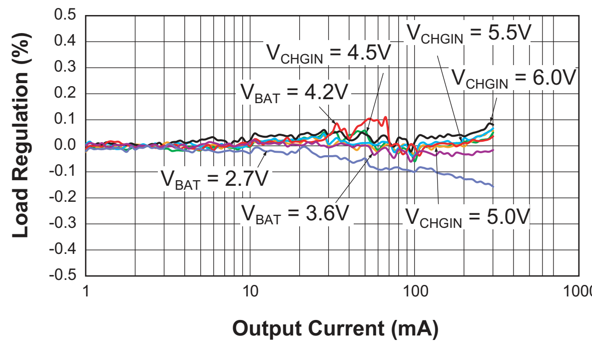


Typical Characteristics—Step-Down Buck Converter

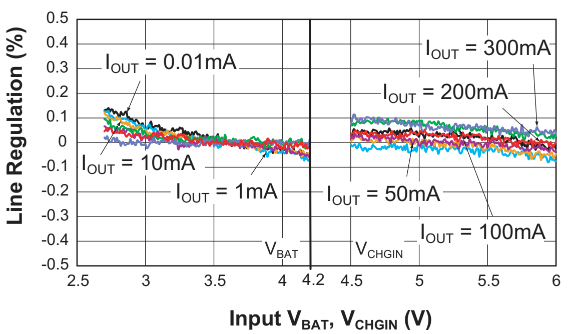
Step-Down Buck Efficiency vs. Output Current
(V_{OUT} = 1.8V; L = 3.3µH)



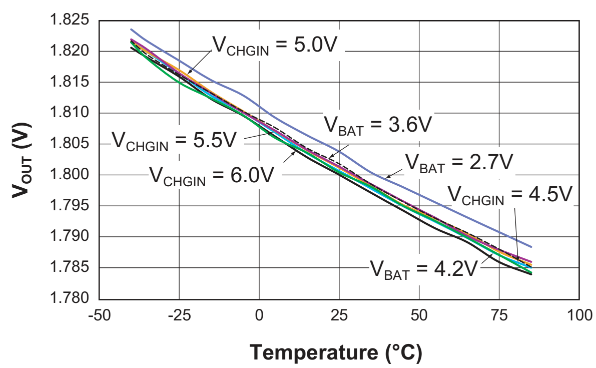
Step-Down Buck Load Regulation vs. Output Current
(V_{OUT} = 1.8V; L = 3.3µH)



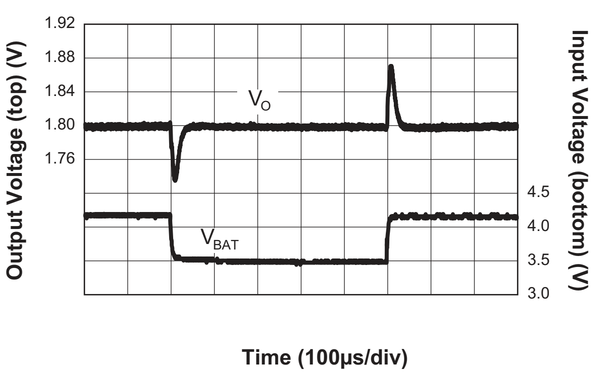
Step-Down Buck Line Regulation vs. CHGIN and Battery Input Voltage
(V_{OUT} = 1.8V; L = 3.3µH)



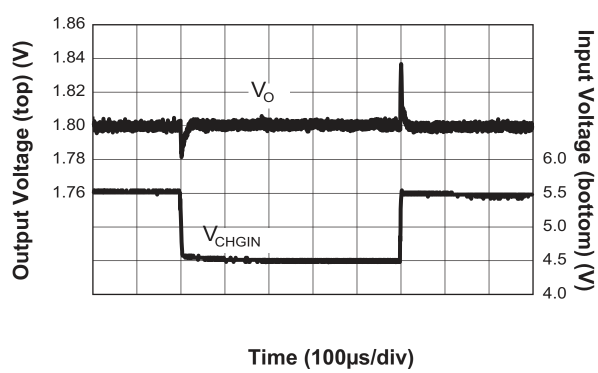
Step-Down Buck Output Voltage vs. Temperature
(I_{OUT} = 10mA)



V_{BAT} Line Transient Response Step-Down Buck
(V_{BAT} = 3.5V to 4.2V; I_{OUT} = 300mA; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)

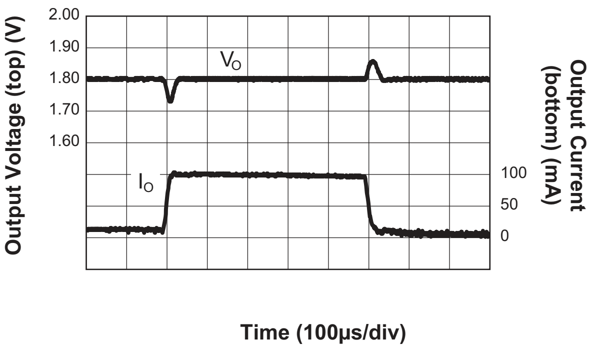


V_{CHGIN} Line Transient Response Step-Down Buck
(V_{CHGIN} = 4.5V to 5.5V; I_{OUT} = 300mA; V_{OUT} = 1.8V; C_{OUT} = 4.7µF)

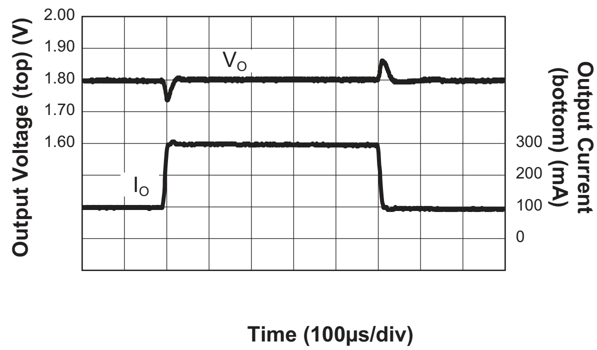


Typical Characteristics—Step-Down Buck Converter (continued)

Load Transient Response Step-Down Buck
($I_{OUTBUCK}$ = 10mA to 100mA; V_{BAT} = 3.6V; $V_{OUTBUCK}$ = 1.8V; C_{OUT} = 4.7µF)

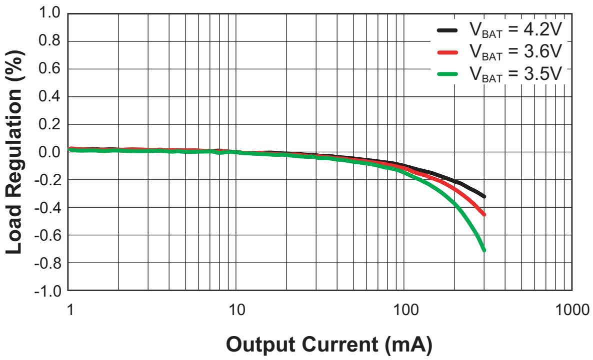


Load Transient Response Step-Down Buck
($I_{OUTBUCK}$ = 100mA to 300mA; V_{BAT} = 3.6V; $V_{OUTBUCK}$ = 1.8V; C_{OUT} = 4.7µF)

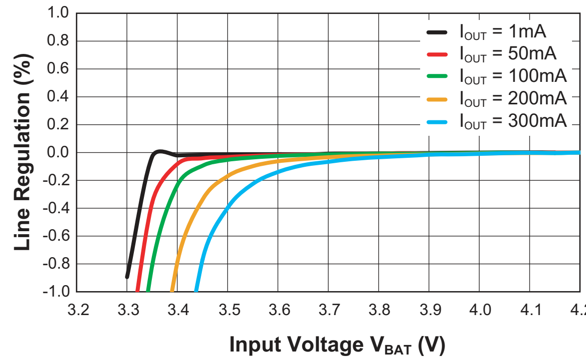


Typical Characteristics—LDO1

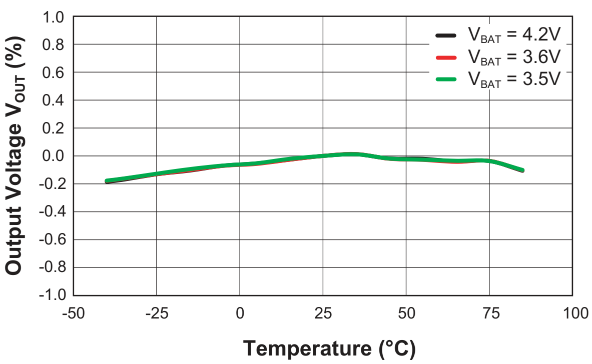
LDO1 Load Regulation vs. Output Current
(V_{OUT} = 3.3V)



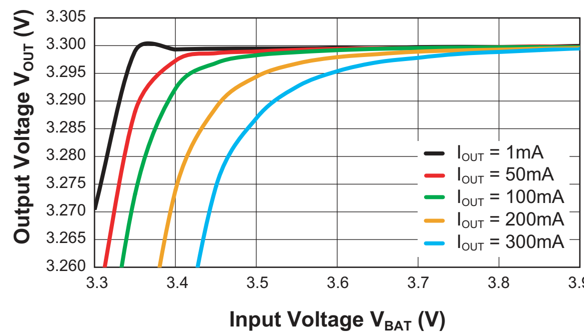
LDO1 Line Regulation vs. Battery Input Voltage
(V_{OUT} = 3.3V)



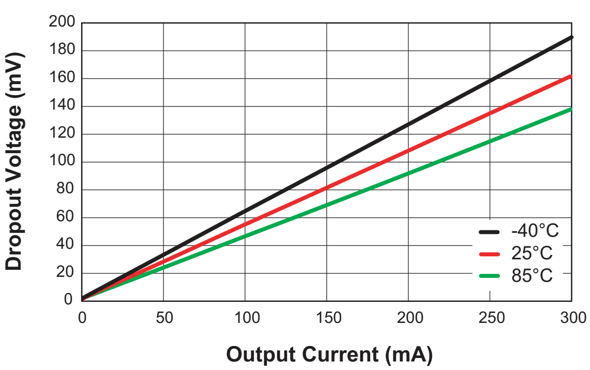
LDO1 Output Voltage vs. Temperature
(I_{OUT} = 10mA)



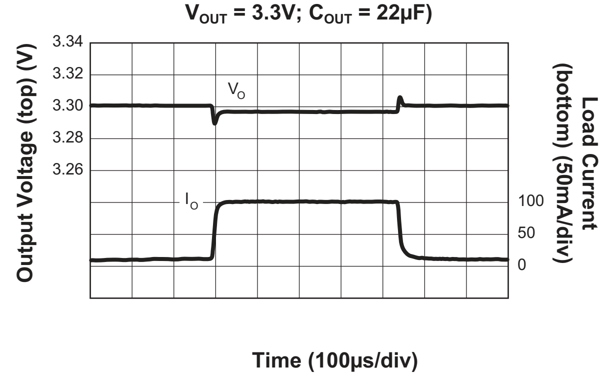
LDO1 Dropout Characteristics vs. Battery Input Voltage
(V_{OUT} = 3.3V)



LDO1 Dropout Voltage vs. Output Current
(V_{OUT} = 3.3V)



Load Transient Response
(10mA to 100mA; V_{BAT} = 3.6V; V_{OUT} = 3.3V; C_{OUT} = 22µF)



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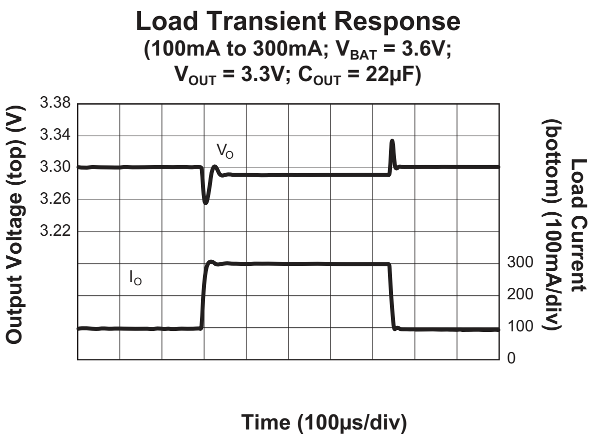
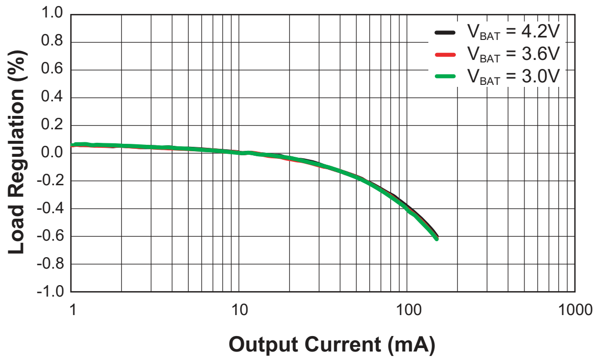
Typical Characteristics—LDO1 (continued)

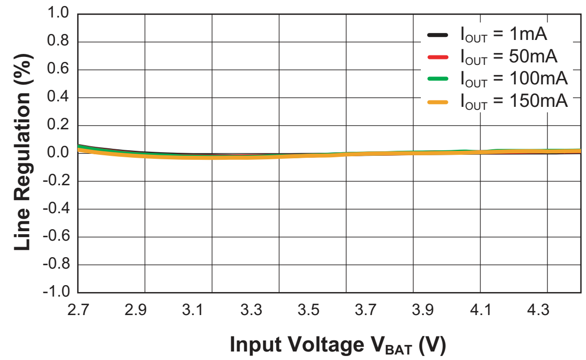


Typical Characteristics—LDO2

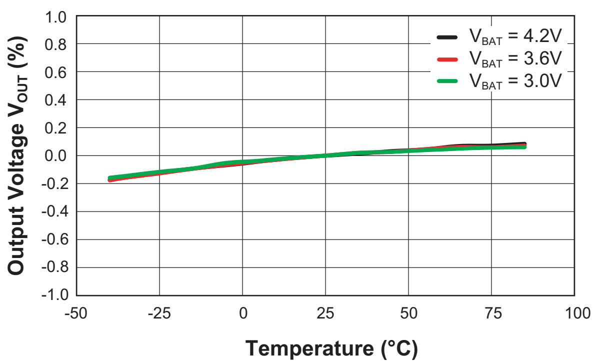
LDO2 Load Regulation vs. Output Current
(V_{OUT} = 1.2V)



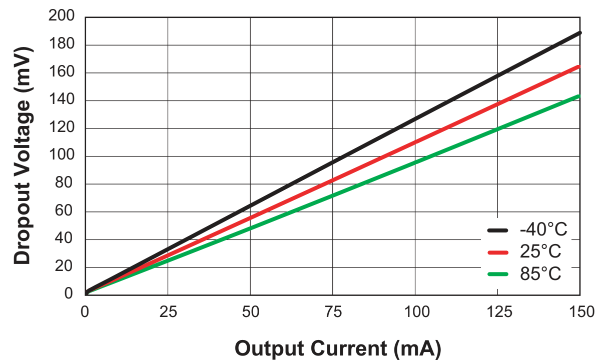
LDO2 Line Regulation vs. Battery Input Voltage
(V_{OUT} = 1.2V)



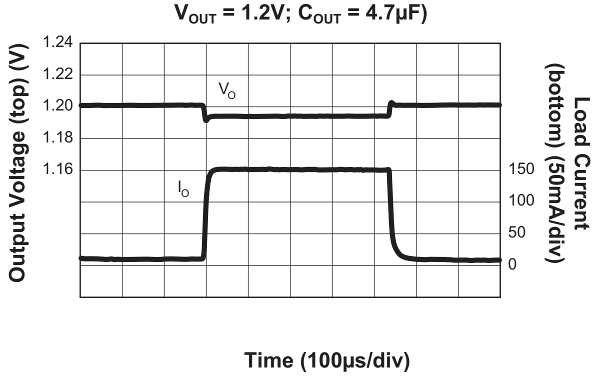
LDO2 Output Voltage vs. Temperature
(I_{OUT} = 10mA)



LDO2 Dropout Voltage vs. Output Current
(V_{OUT} = 1.2V)

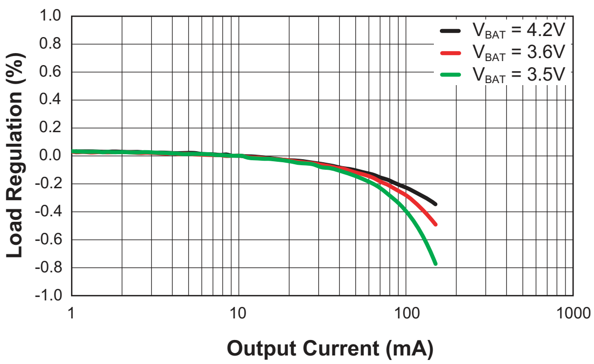


Load Transient Response
(10mA to 150mA; V_{BAT} = 3.6V;
V_{OUT} = 1.2V; C_{OUT} = 4.7µF)

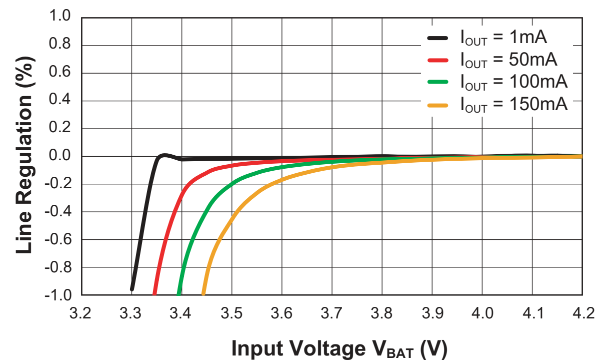


Typical Characteristics—LDO5

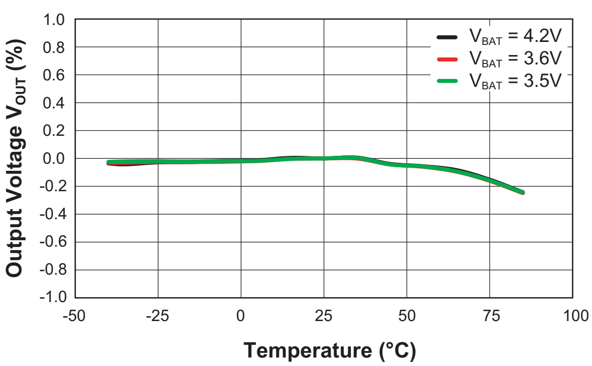
LDO5 Load Regulation vs. Output Current
(V_{OUT} = 3.3V)



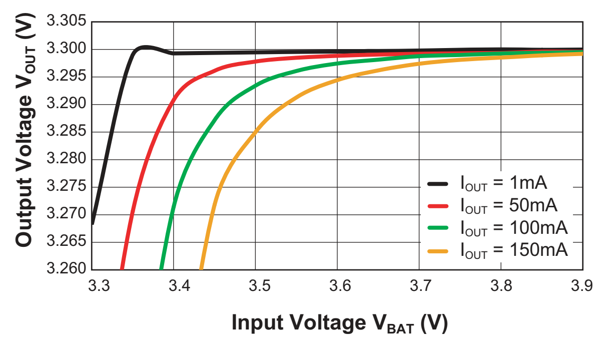
LDO5 Line Regulation vs. Battery Input Voltage
(V_{OUT} = 3.3V)



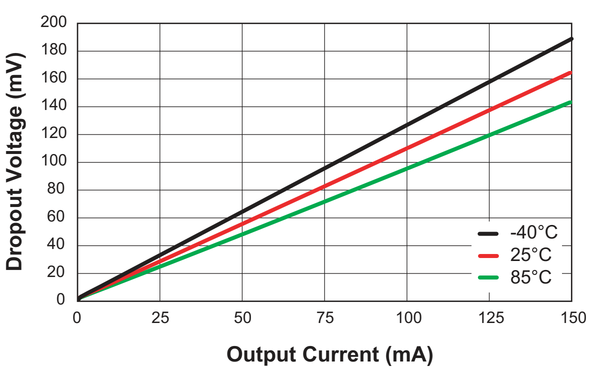
LDO5 Output Voltage vs. Temperature
(I_{OUT} = 10mA)



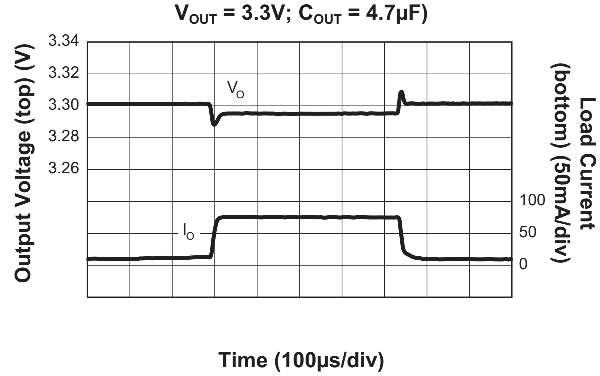
LDO5 Dropout Characteristics vs. Battery Input Voltage
(V_{OUT} = 3.3V)



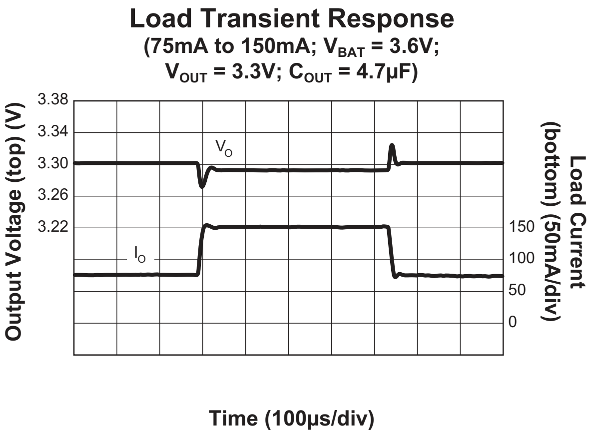
LDO5 Dropout Voltage vs. Output Current
(V_{OUT} = 3.3V)



Load Transient Response
(10mA to 75mA; V_{BAT} = 3.6V; V_{OUT} = 3.3V; C_{OUT} = 4.7µF)

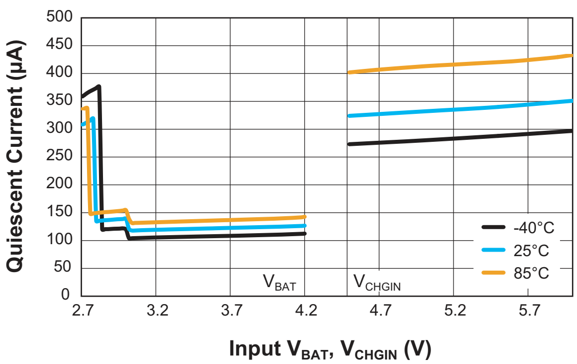


Typical Characteristics—LDO5 (continued)

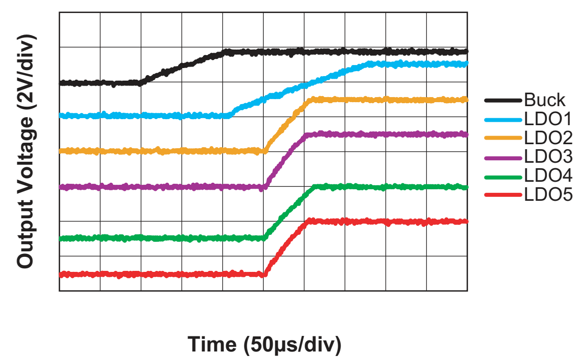


Typical Characteristics—General

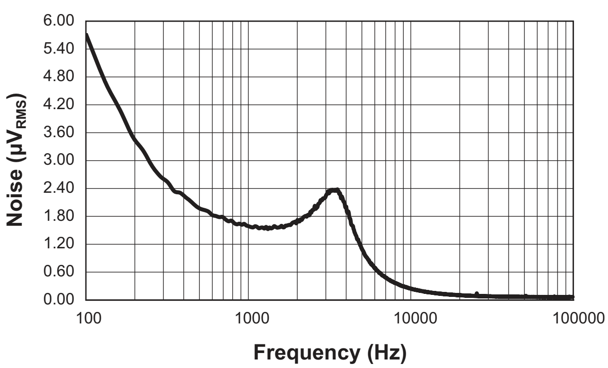
Quiescent Current vs. Input Voltage
(V_{OUT} = 1.8V; L = 3.3μH)



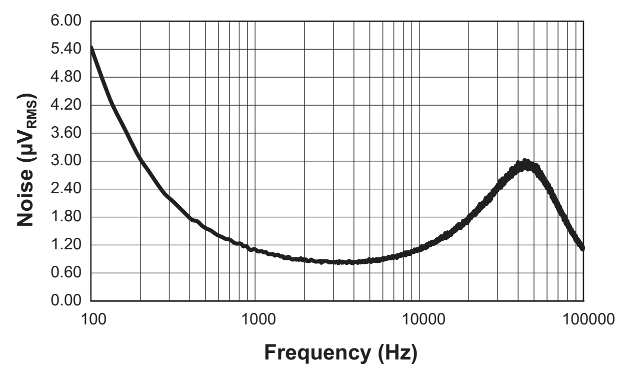
Start-up Sequence
(V_{CHGIN} = 5.0V)



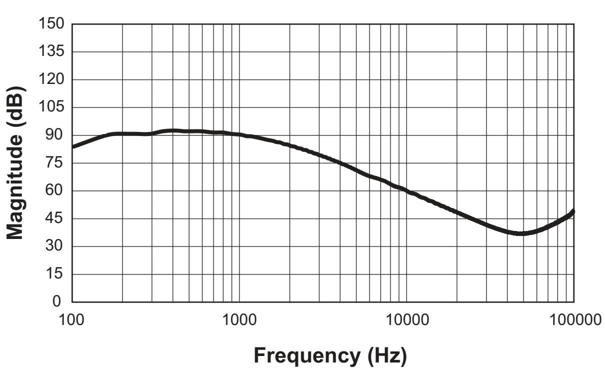
LDO Output Voltage Noise
(No Load; Power BW: 100~100KHz)



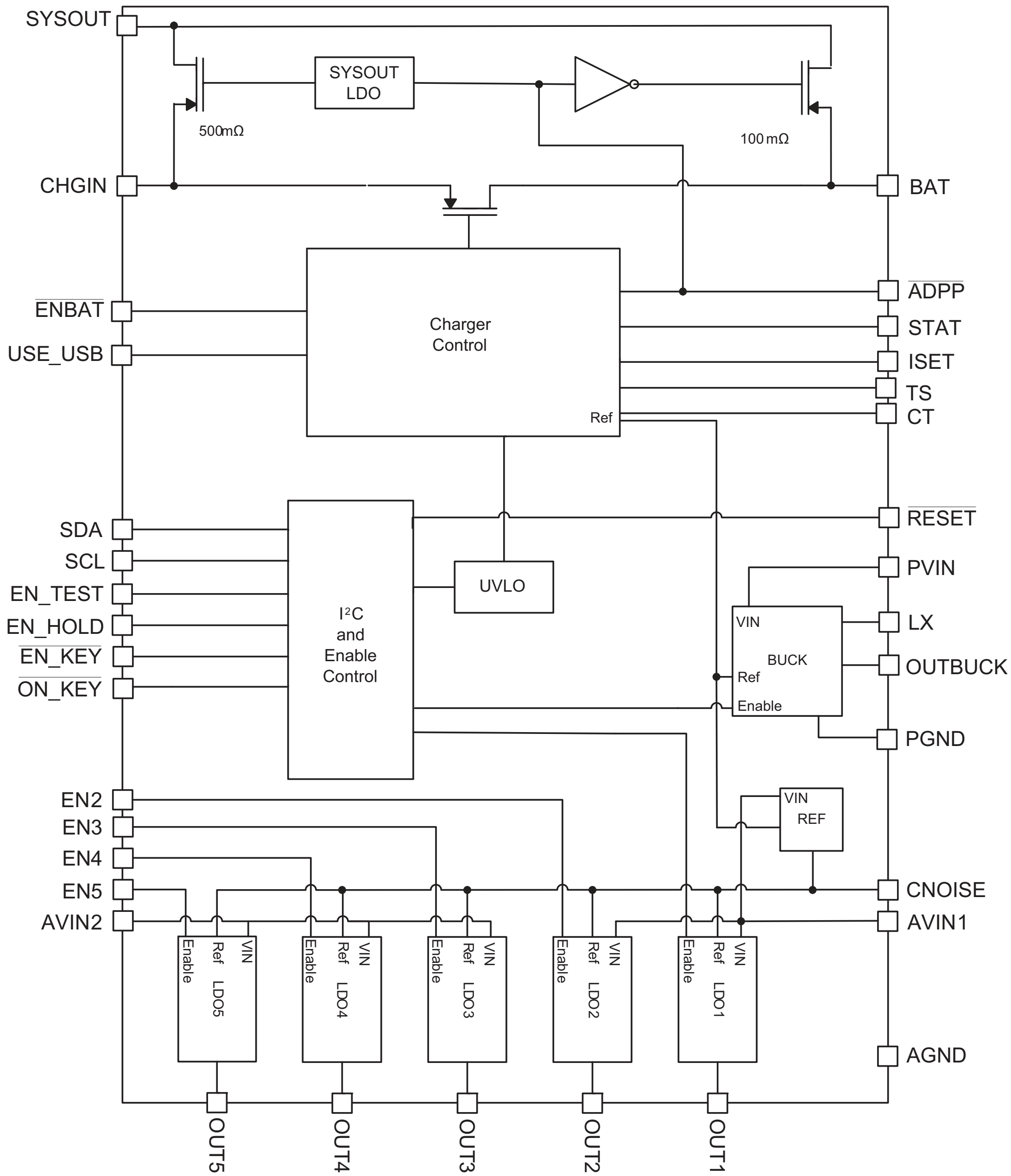
LDO Output Voltage Noise
(I_{OUT3} = 10mA, Power BW = 100~100KHz)



LDO Power Supply Rejection Ratio, PSRR
(I_{OUT3} = 10mA, BW = 100~100KHz)



Functional Block Diagram



Functional Description

The AAT2601B is a complete power management solution. It seamlessly integrates an intelligent, stand-alone CC/CV (Constant Current/Constant Voltage), linear-mode single-cell battery charger with one step-down Buck converter and five low-dropout (LDO) regulators to provide power from either a wall adapter or a single-cell Lithium Ion/Polymer battery. Internal load switches allow the LDO regulators and DC-DC converter to operate from the best available power source of either an AC wall adapter, USB port supply or battery.

If only the battery is available, then the voltage regulators and converter are powered directly from the battery through a 100mΩ load switch. (The charger is put into sleep mode and draws less than 1μA quiescent current.)

If the system is connected to a wall adapter, then the voltage converters are powered directly from the adapter through a 500mΩ load switch and the battery is disconnected from the voltage converter inputs. This allows the system to operate regardless of the charging state of the battery or with no battery.

System Output (SYSOUT)

Intelligent control of the integrated load switches is managed by the switch control circuitry to allow the step-down converter and the LDOs to have the best available power source. When the CHGIN pin voltage is above 4.5V, the system automatically turns on and the power to the SYSOUT pin will be provided by either the CHGIN pin or the BAT pin. When the USE_USB pin is low, CHGIN provides power to SYSOUT through an internal LDO regulated to 3.9V. When the USE_USB pin is high or if forced through use of an I^{2}C command, the BAT pin is shorted to SYSOUT through a 100mΩ switch. If a CHGIN voltage is not present and the system is enabled, SYSOUT will be shorted to BAT.

This system allows the step-down converter and LDOs to always have the best available source of power. This also allows the voltage converters to operate with no battery, or with a battery voltage that falls below the precondition trickle charge threshold.

Typical Power Up Sequence

The AAT2601B supports a variety of push-button or enable/disable schemes. A typical startup and shutdown process proceeds as illustrated in Figures 1 and 2. System startup is initiated whenever one of the following conditions occurs:

1) A push-button is used to assert $\overline{\text{EN\_KEY}}$ low.
2) A valid supply (>CHGIN UVLO) is connected to the charger input CHGIN.
3) A hands free device or headset is connected, asserting EN_TEST high.

The startup sequence for the AAT2601B Buck and LDO1 is typically initiated by pulling the $\overline{\text{EN\_KEY}}$ pin low with a pushbutton switch, as shown in Figure 1. The Buck is the first block to be turned on. When the output of the Buck reaches 90% of its final value, then LDO1 is enabled. When LDO1 reaches 90% of its final value, the 65ms RESET timer is initiated holding the microprocessor in reset. When the $\overline{\text{RESET}}$ pin goes High, the µP can begin a power up sequence. After the startup sequence has commenced, LDO2, LDO3, LDO4, and LDO5 can be enabled and disabled as desired using their independent enable pins, even while the Buck and LDO1 are still starting up. However, if they are shut down, then LDO2, LDO3, LDO4, and LDO5 cannot be enabled. The µP must pull the EN_HOLD signal high before the $\overline{\text{EN\_KEY}}$ signal can be released by the push-button. This procedure requires that the push-button be held until the µP assumes control of EN_HOLD, providing protection against inadvertent momentary assertions of the push-button. Once EN_HOLD is high the startup sequence is complete. If the µP is unable to complete its power-up routine successfully before the user lets go of the push-button, the AAT2601B will automatically shut down. ($\overline{\text{EN\_KEY}}$ and EN_HOLD are OR'd internally to enable the two core converters.)

Alternately, the startup sequence is automatically started without the pushbutton switch when the CHGIN pin rises above its UVLO threshold. The system cannot be disabled until the voltage at the CHGIN pin drops below the falling UVLO threshold. Thirdly, the EN_TEST pin can be used to start up the device for test purposes or for hands-free operation such as when connecting a headset to the system.

Typical Power Down Sequence

If only the battery is connected and the voltage level is above the BAT UVLO , then the $\overline{\text{EN\_KEY}}$ pin can be held low in order to power down AAT2601B. The user can initiate a shutdown process by pressing the push-button a second time. Upon detecting a second assertion of $\overline{\text{EN\_KEY}}$ (by depressing the push-button), the AAT2601B asserts $\overline{\text{ON\_KEY}}$ to interrupt the microprocessor which initiates an interrupt service routine that the user pressed the push-button. If EN_TEST and CHGIN are both low, the microprocessor then initiates a power-down routine, the final step of which will be to de-assert EN_HOLD, disabling LDO2, LDO3, LDO4, and LDO5.

When the voltage at the CHGIN pin is above the CHGIN UVLO, the device cannot be powered down. If the voltage at the CHGIN pin is below the CHGIN UVLO, both the $\overline{\text{EN\_KEY}}$ and EN_HOLD pins must be held low in order to power down the AAT2601B. If LDO2, LDO3, LDO4, and LDO5 have not been disabled individually prior to global power down, then they will be turned off simultaneously with the Buck. The outputs of LDO4 and LDO5 are internally pulled to ground with 10k during shutdown to discharge the output capacitors and ensure a fast turn-off response time.

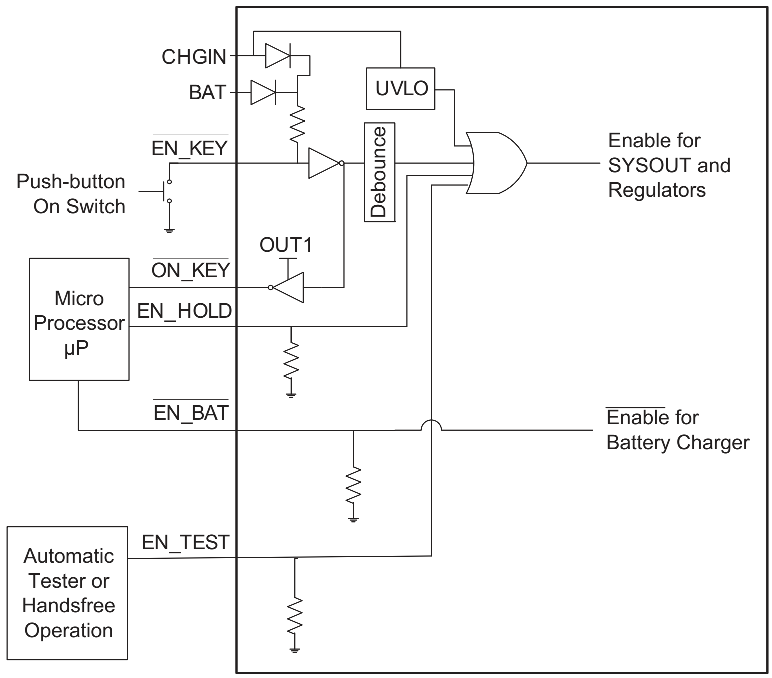


Figure 1: Enable Function Detailed Schematic.

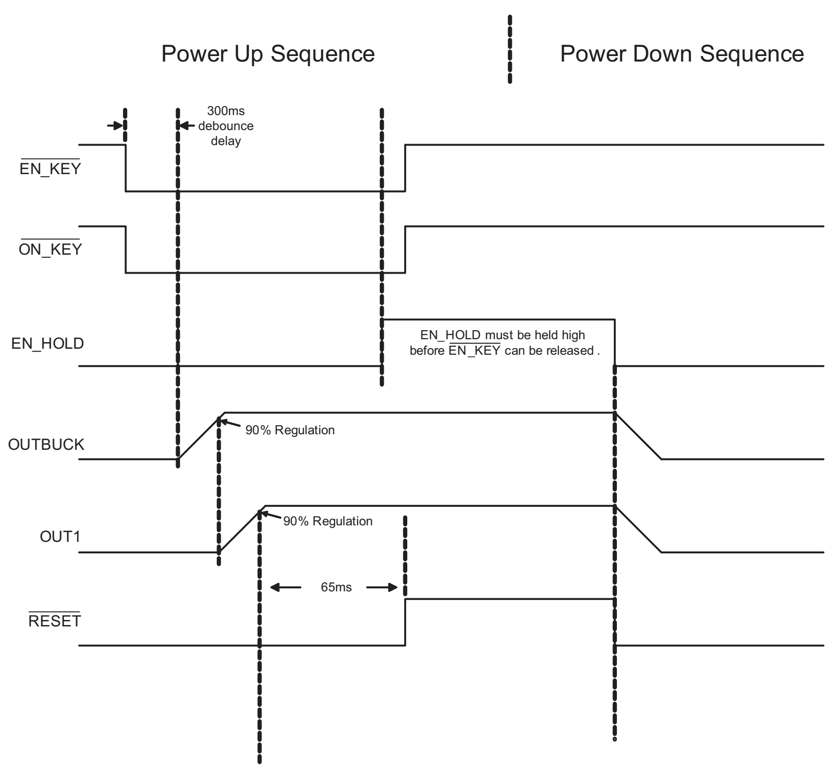


Figure 2: Typical Power Up/Down Sequence.

Battery Charger

Figure 3 illustrates the entire battery charging profile which consists of three phases.

1. Preconditioning Current Mode (Trickle) Charge
2. Constant Current Mode Charge
3. Constant Voltage Mode Charge

Preconditioning Trickle Charge

Battery charging commences only after the AAT2601B battery charger checks several conditions in order to maintain a safe charging environment. The system operation flow chart for the battery charger operation is shown in Figure 4. The input supply must be above the minimum operating voltage (UVLO) and the enable pin ($\overline{\text{ENBAT}}$) must be low (it is internally pulled down). When the battery is connected to the BAT pin, the battery charger checks the condition of the battery and determines which charging mode to apply.

Preconditioning Current Mode Charge Current

If the battery voltage is below the preconditioning voltage threshold V_{MIN}, then the battery charger initiates precondition trickle charge mode and charges the battery at 12% of the programmed constant-current magnitude. For example, if the programmed current is 500mA, then the trickle charge current will be 60mA. Trickle charge is a safety precaution for a deeply discharged cell. It also reduces power dissipation in the internal series pass MOSFET when the input-output voltage differential is at its highest.

Constant Current Mode Charge Current

Trickle charge continues until the battery voltage reaches V_{MIN}. At this point the battery charger begins constant-current charging. The current level default for this mode is programmed using a resistor from the ISET pin to ground. Once that resistor has been selected for the default charge current, then the current can be adjusted through I^2C from a range of 40% to 180% of the programmed default charge current. Programmed current can be set at a minimum of 100mA and up to a maximum of 1A. When the $\overline{\text{ADPP}}$ signal goes high, the default I^2C setting of 100% is reset. If the USE_USB signal is high when this happens, the charge current is reset to an internally set 100mA current until the microcontroller sends another I^2C signal to change the charge current. (see I^2C Programming section).

Constant Voltage Mode Charge

Constant current charging will continue until the battery voltage reaches the Output Charge Voltage Regulation point V_{BAT_REG}. When the battery voltage reaches the regulation voltage (V_{BAT_REG}), the battery charger will transition to constant-voltage mode. V_{BAT_REG} is factory programmed to 4.2V (nominal). Charging in constant-voltage mode will continue until the charge current has reduced to the end of charge termination current programmed using the I^2C interface (5%, 10%, 15%, or 20%).

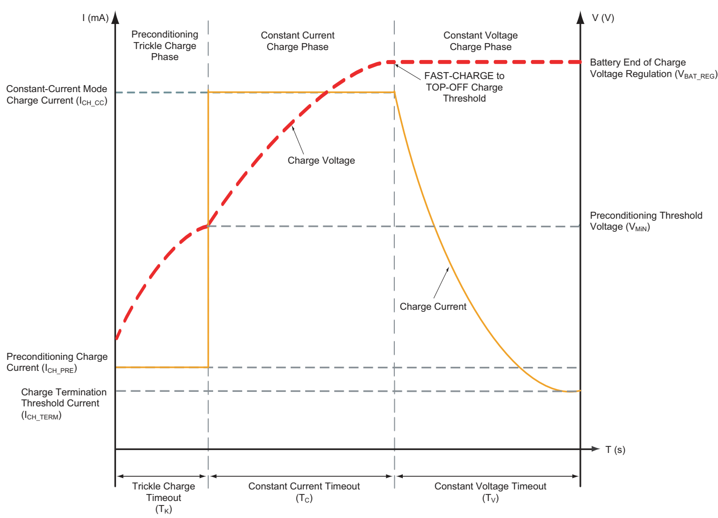


Figure 3: Current vs. Voltage and Charger Time Profile.

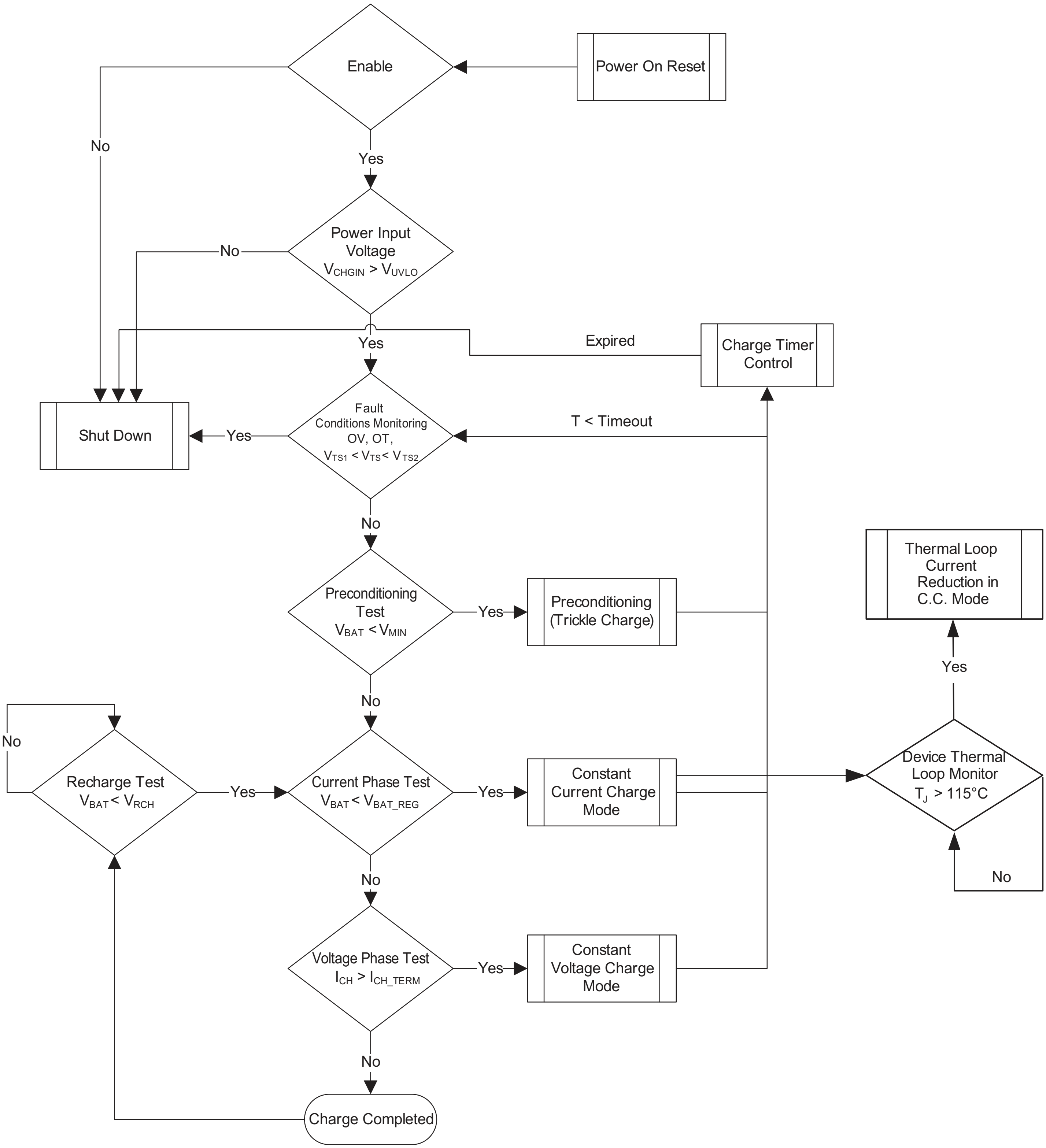


Figure 4: System Operation Flow Chart for the Battery Charger.

Power Saving Mode

After the charge cycle is complete, the battery charger turns off the series pass device and automatically goes into a power saving sleep mode. During this time, the series pass device will block current in both directions to prevent the battery from discharging through the battery charger.

The battery charger will remain in sleep mode even if the charger source is disconnected. It will come out of sleep mode if either the battery terminal voltage drops below the V_{RCH} threshold, the charger EN pin is recycled, or the charging source is reconnected. In all cases, the battery charger will monitor all parameters and resume charging in the most appropriate mode.

Temperature Sense (TS)

The TS pin is available to monitor the battery temperature. Connect a 10k NTC resistor from the TS pin to ground. The TS pin outputs a 75µA constant current into the resistor and monitors the voltage to ensure that the battery temperature does not fall outside the limits depending on the temperature coefficient of the resistor used. When the voltage goes above 2.39V or goes below 0.331V, the charging current will be suspended.

Charge Safety Timer (CT)

While monitoring the charge cycle, the AAT2601B utilizes a charge safety timer to help identify damaged cells and to ensure that the cell is charged safely. Operation is as follows: upon initiating a charging cycle, the AAT2601B charges the cell at 12% of the programmed maximum charge until V_{BAT} >2.8V. If the cell voltage fails to reach the preconditioning threshold of 2.8V (typ) before the safety timer expires, the cell is assumed to be damaged and the charge cycle terminates. If the cell voltage exceeds 2.8V prior to the expiration of the timer, the charge cycle proceeds into fast charge. There are three timeout periods: 1 hour for Trickle Charge mode, 3 hours for Constant Current mode, and 3 hours for Constant Voltage mode.

The CT pin is driven by a constant current source and will provide a linear response to increases in the timing capacitor value. Thus, if the timing capacitor were to be doubled from the nominal 0.1µF value, the time-out periods would be doubled. If the programmable watchdog timer function is not needed, it can be disabled by terminating the CT pin to ground. The CT pin should not be left floating or unterminated, as this will cause errors in the internal timing control circuit. The constant current provided to charge the timing capacitor is very small, and this pin is susceptible to noise and changes in capacitance value. Therefore, the timing capacitor should be physically located on the printed circuit board layout as close as possible to the CT pin. Since the accuracy of the internal timer is dominated by the capacitance value, a 10% tolerance or better ceramic capacitor is recommended. Ceramic capacitor materials, such as X7R and X5R types, are a good choice for this application.

Programming Charge Current (ISET)

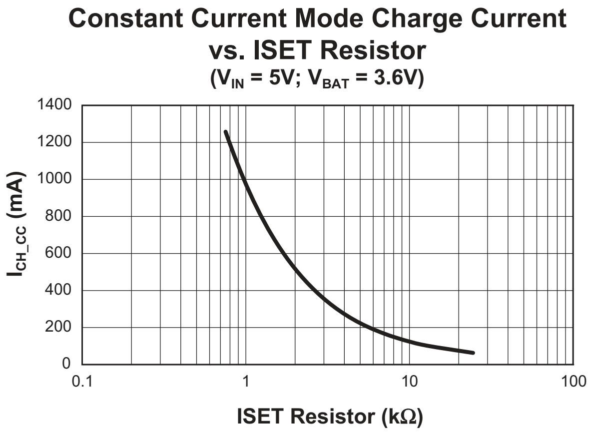
The default constant current mode charge level is user programmed with a set resistor placed between the ISET pin and ground. The accuracy of the constant charge current, as well as the preconditioning trickle charge current, is dominated by the tolerance of the set resistor. For this reason, a 1% tolerance metal film resistor is recommended for the set resistor function. The constant charge current levels from 100mA to 1A may be set by selecting the appropriate resistor value from Table 1 and Figure 5. The ISET pin current to charging current ratio is 1 to 800. It is regulated to 1.25V during constant current mode unless changed using I²C commands. It can be used as a charging current monitor, based on the equation:

$$I_{CH} = 800 \cdot \left(\frac{V_{ISET}}{R_{ISET}}\right)$$

During preconditioning charge, the ISET pin is regulated to 12% of the fast charge current I_{SET} voltage level (Figure 5), but the equation stays the same. During constant voltage charge mode, the ISET pin voltage will slew down and be directly proportional to the battery current at all times.

Constant Charging Current I_{CH_CC} (mA)	Set Resistor Value (kΩ)
100	10
200	4.99
300	3.32
400	2.49
500	2
600	1.65
700	1.43
800	1.24
900	1.1
1000	1

Table 1: Constant Current Charge vs. I_{SET} Resistor Value.



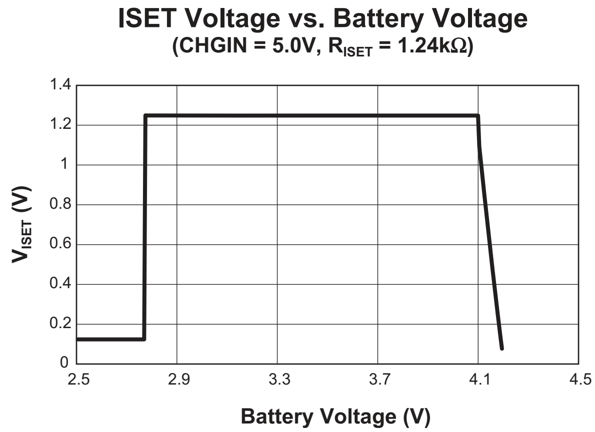


Figure 5: Constant Current Mode Charge I_{CH_CC} Setting vs. I_{SET} Resistor and I_{SET} Voltage vs. Battery Voltage.

Reverse Battery Leakage

The AAT2601B includes internal circuitry that eliminates the need for series blocking diodes, reducing solution size and cost as well as dropout voltage relative to conventional battery chargers. When the input supply is removed or when CHGIN goes below the AAT2601B's under voltage-lockout (UVLO) voltage, or when CHGIN drops below V_{BAT}, the AAT2601B automatically reconfigures its power switches to minimize current drain from the battery.

Adapter Power Indicator ($\overline{ADPP}$)

This is an open drain output which will pull low when V_{CHGIN} > 4.5V. When this happens, depending on the status of the USE_USB pin, the charge current will be reset to the default ISET values or I²C programmed values.

Charge Status Output (STAT)

The AAT2601B provides battery charging status via a status pin. This pin is a buffered output with a supply level up to the LDO1 output. The status pin can indicate the following conditions:

Event Description	STAT
No battery charging activity	Low (to GND)
Battery charging	High (to V_{OUT1})
Charging completed	Low (to GND)

Table 2: Charge Status Output (STAT).

CHGIN Bypass Capacitor Selection

CHGIN is the power input for the AAT2601B battery charger. The battery charger is automatically enabled whenever a valid voltage is present on CHGIN. In most applications, CHGIN is connected to either a wall adapter or USB port. Under normal operation, the input of the charger will often be "hot-plugged" directly to a powered USB or wall adapter cable, and supply voltage ringing and overshoot may appear at the CHGIN pin. A high quality capacitor connected from CHGIN to GND, placed as close as possible to the IC, is sufficient to absorb the energy. Wall-adapter powered applications provide flexibility in input capacitor selection, but the USB specification presents limitations to input capacitance selection. In order to meet both the USB 2.0 and USB OTG (On The Go) specifications while avoiding USB supply under-voltage conditions resulting from the current limit slew rate (100mA/μs) limitations of the USB bus, the CHGIN bypass capacitance value must be between 1μF and 4.7μF. Ceramic capacitors are often preferred for bypassing due to their small size and good surge current ratings, but care must be taken in applications that can encounter hot plug conditions as their very low ESR, in combination with the inductance of the cable, can create a high-Q filter that induces excessive ringing at the CHGIN pin. This ringing can couple to the output and be mistaken as loop instability, or the ringing may be large enough to damage the input itself. Although the CHGIN pin is designed for maximum robustness and an absolute maximum voltage rating of +6.5V for transients, attention must be given to bypass techniques to ensure safe operation. As a result, design of the CHGIN bypass must take care to “de-Q” the filter. This can be accomplished by connecting a 1Ω resistor in series with a ceramic capacitor (as shown in Figure 6A), or by bypassing with a tantalum or electrolytic capacitor to utilize its higher ESR to dampen the ringing (as shown in Figure 6B). For additional protection, Zener diodes with 6V clamp voltages may also be used. In any case, it is always critical to evaluate voltage transients at the CHGIN pin with an oscilloscope to ensure safe operation.

Thermal Considerations

The actual maximum charging current is a function of charge adapter input voltage, the state of charge of the battery at the moment of charge, the system supply current from SYSOUT, and the ambient temperature and the thermal impedance of the package and printed circuit board. The maximum programmable current may not be achievable under all operating parameters. One issue to consider is the amount of current being sourced to the SYSOUT pin from the CHGIN LDO while the battery is being charged.

The AAT2601B is offered in a TQFN55-36 package which can provide up to 4W of power dissipation when it is properly bonded to a printed circuit board and has a maximum thermal resistance of 25°C/W. Many considerations should be taken into account when designing the printed circuit board layout, as well as the placement of the charger IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the charger IC will also have an effect on the thermal limits of a battery charging application. The maximum limits that can be expected for a given ambient condition can be estimated by the following discussion. First, the maximum power dissipation for a given situation should be calculated:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)
θ_{JA} = Package Thermal Resistance (°C/W)
$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C) [150°C]
T_A = Ambient Temperature (°C)

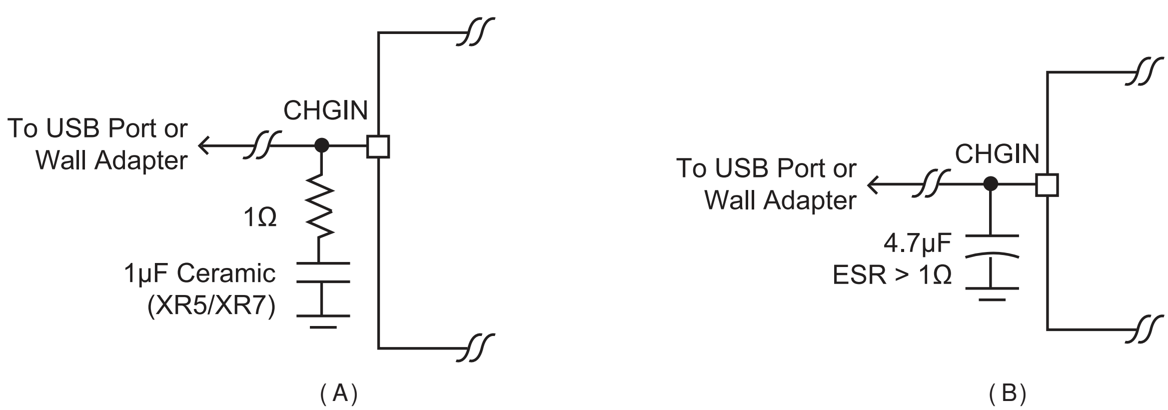


Figure 6: Hot Plug Requirements.

Next, the power dissipation for the charger can be calculated by the following equation:

$$P_D = (V_{CHGIN} - V_{BAT}) \cdot I_{CH\_CC} + (V_{CHGIN} \cdot I_{OP}) + (V_{CHGIN} - V_{SYSOUT}) \cdot I_{SYSOUT}$$
$$+ (V_{SYSOUT} - V_{OUT1}) \cdot I_{OUT1} + (V_{SYSOUT} - V_{OUT2}) \cdot I_{OUT2}$$
$$+ (V_{SYSOUT} - V_{OUT3}) \cdot I_{OUT3} + (V_{SYSOUT} - V_{OUT4}) \cdot I_{OUT4}$$
$$+ (V_{SYSOUT} - V_{OUT5}) \cdot I_{OUT5}$$
$$+ I_{OUTBUCK}^2 \cdot \left(R_{DS(ON)L} \cdot \frac{V_{OUTBUCK}}{V_{SYSOUT}} + \frac{R_{DS(ON)H} \cdot [V_{SYSOUT} - V_{OUTBUCK}]}{V_{SYSOUT}}\right)$$

Where:

P_D = Total Power Dissipation by the Device
V_{CHGIN} = CHGIN Input Voltage
V_{BAT} = Battery Voltage at the BAT Pin
I_{CH_CC} = Constant Charge Current Programmed for the Application
I_{OP} = Quiescent Current Consumed by the IC for Normal Operation [0.5mA]
V_{SYSOUT} and I_{SYSOUT} = Output voltage and load current from the SYSOUT pin for the system LDOs and step-down converter [3.9V out for SYSOUT]
$R_{DS(ON)H}$ and $R_{DS(ON)L}$ = On-resistance of step-down high and low side MOSFETs [0.8Ω each]
V_{OUTX} and I_{OUTX} = Output voltage and load currents for the LDOs and step-down converter [3V out for each LDO]

By substitution, we can derive the maximum charge current before reaching the thermal limit condition (T_{REG} = 100°C, Thermal Loop Regulation). The maximum charge current is the key factor when designing battery charger applications.

$$I_{CH\_CC(MAX)} = \frac{\left(\frac{(T_{REG} - T_A)}{\theta_{JA}} - (V_{CHGIN} \cdot I_{OP})\right) - (V_{CHGIN} - V_{SYSOUT}) \cdot I_{SYSOUT} - [(V_{SYSOUT} - V_{OUT1}) \cdot I_{OUT1}] - (V_{SYSOUT} - V_{OUT2}) \cdot I_{OUT2} - [(V_{SYSOUT} - V_{OUT3}) \cdot I_{OUT3}] - (V_{SYSOUT} - V_{OUT4}) \cdot I_{OUT4} - (V_{SYSOUT} - V_{OUT5}) \cdot I_{OUT5} - I_{OUTBUCK}^2 \cdot \left(R_{DS(ON)L} \cdot \frac{V_{OUTBUCK}}{V_{SYSOUT}} + \frac{R_{DS(ON)H} \cdot (V_{SYSOUT} - V_{OUTBUCK})}{V_{SYSOUT}}\right)}{V_{CHGIN} - V_{BAT}}$$

In general, the worst condition is when there is the greatest voltage drop across the charger, when battery voltage is charged up to just past the preconditioning voltage threshold and the LDOs and step-down converter are sourcing full output current.

Thermal Overload Protection

The AAT2601B integrates thermal overload protection circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions, for example. This circuitry disables all regulators if the AAT2601B die temperature exceeds 140°C, and prevents the regulators from being enable until the die temperature drops by 15°C (typ).

Synchronous Step-Down Converter (Buck)

The AAT2601B contains a high performance 300mA, 1.5MHz synchronous step-down converter. The step-down converter operates to ensure high efficiency performance over all load conditions. It requires only three external power components (C_{IN}, C_{OUT}, and L). A high DC gain error amplifier with internal compensation controls the output. It provides excellent transient response and load/line regulation. Transient response time is typically less than 20μs. The converter has soft start control to limit inrush current and transitions to 100% duty cycle at drop out.

The step-down converter input pin PVIN should be connected to the SYSOUT LDO output pin. The output voltage is internally fixed at 1.8V. Power devices are sized for 300mA current capability while maintaining over 90% efficiency at full load.

Input/Output Capacitor and Inductor

Apart from the input capacitor that is shared with the LDO inputs, only a small L-C filter is required at the output side for the step-down converter to operate properly. Typically, a 3.3μH inductor such as the Sumida CDRH2D11NP-3R3NC and a 4.7μF ceramic output capacitor are recommended for low output voltage ripple and small component size. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10μF ceramic input capacitor is sufficient for most applications.

Control Loop

The converter is a peak current mode step-down converter. The inner, wide bandwidth loop controls the inductor peak current. The inductor current is sensed through the P-channel MOSFET (high side) which is also used for short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak inductor current to force a constant output voltage for all load and line conditions. The voltage feedback resistive divider is internal and the error amplifier reference voltage is 0.45V. The voltage loop has a high DC gain making for excellent DC load and line regulation. The internal voltage loop compensation is located at the output of the transconductance voltage error amplifier.

Soft Start

Soft start slowly increases the internal reference voltage when the input voltage or enable input is initially applied. It limits the current surge seen at the input and eliminates output voltage overshoot.

Current Limit and Over-Temperature Protection

For overload conditions the peak input current is limited. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

Linear LDO Regulators (OUT1-5)

The advanced circuit design of the linear regulators has been specifically optimized for very fast start-up and shutdown timing. These proprietary LDOs are tailored for superior transient response characteristics. These traits are particularly important for applications which require fast power supply timing.

The high-speed turn-on capability is enabled through the implementation of a fast start control circuit, which accelerates the power up behavior of fundamental control and feedback circuits within the LDO regulator. For LDO4 and LDO5, fast turn-off time response is achieved by an active output pull down circuit, which is enabled when the LDO regulator is placed in the shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation.

Input/Output Capacitors

The LDO regulator output has been specifically optimized to function with low cost, low ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types. The input capacitor is shared with all LDO inputs and the step-down converter. A 10μF is sufficient. A 4.7μF ceramic output capacitor is recommended for LDO2-5 and a 22μF output capacitor for LDO1.

Current Limit and Over-Temperature Protection

The regulator comes with complete short circuit and thermal protection. The combination of these two internal protection circuits gives a comprehensive safety system to guard against extreme adverse operating conditions.

I^{2}C Serial Interface and Programmability

Serial Interface

Many of the features of the AAT2601B can be controlled via the I^{2}C serial interface. The I^{2}C serial interface is a widely used interface where it requires a master to initiate all the communications with the slave devices. The I^{2}C protocol consists of 2 active wire SDA (serial data line) and SCL (serial clock line). Both wires are open drain and require an external pull up resistor to V_{CC} (SYSOUT may be used as V_{CC}). The SDA pin serves I/O function, and the SCL pin controls and references the I^{2}C bus. I^{2}C protocol is a bidirectional bus which allows both read and write actions to take place, but the AAT2601B supports the write protocol only. Since the protocol has a dedicated bit for Read or Write access (R/W), when communicating with AAT2601B, this bit must be set to "0".

The timing diagram in Figure 7 depicts the transmission protocol.

START and STOP Conditions

START and STOP conditions are always generated by the master. Prior to initiating a START condition, both the SDA and SCL pin are idle mode (idle mode is when there is no activity on the bus and SDA and SCL are pulled to V_{CC} via external resistor). As depicted in Figure 7, a START condition is defined to be when the master pulls the SDA line low and after a short period pulls the SCL line low. A START condition acts as a signal to all IC's that something is about to be transmitted on the BUS.

A STOP condition, also shown in Figure 7, is when the master releases the bus and SCL changes from low to high followed by SDA low to high transition. The master does not issue an ACKNOWLEGE and releases the SCL and SDA pins.

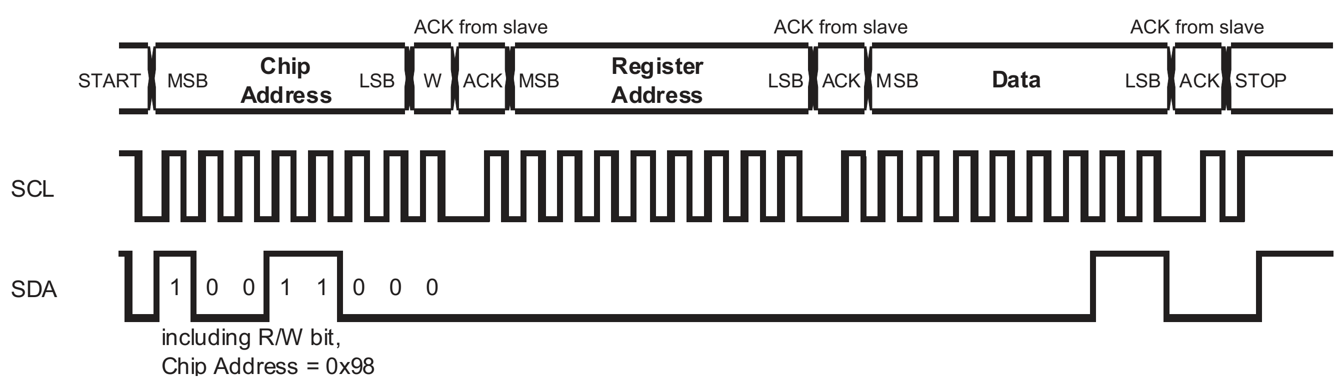


Figure 7: I^{2}C Timing Diagram.

Transferring Data

Every byte on the bus must be 8 bits long. A byte is always sent with a most significant bit first (see Figure 8).

MSB						LSB	R/W

Figure 8: Bit Order.

The address is embedded in the first seven bits of the byte. The eighth bit is reserved for the direction of the information flow for the next byte of information. For the AAT2601B, this bit must be set to "0". The full 8-bit address including the R/W bit is 0x98 (hex) or 10011000 in binary.

Acknowledge Bit

The acknowledge bit is the ninth bit of data. It is used to send back a confirmation to the master that the data has been received properly. For acknowledge to take place, the MASTER must first release the SDA line, then the SLAVE will pull the data line low as shown in Figure 7.

Serial Programming Code

After sending the chip address, the master should send an 8-bit data stream to select which register to program and then the codes that the user wishes to enter.

Register 0x00:

Timer	$RCHG_1$	$RCHG_0$	CHG_2	CHG_1	CHG_0	$Term_1$	$Term_0$

Register 0x01:

Not used	Not used	Not used	Not used	Not used	SYS	$LDO1_1$	$LDO1_0$

Register 0x02:

$LDO5_1$	$LDO5_0$	$LDO4_1$	$LDO4_0$	$LDO3_1$	$LDO3_0$	$LDO2_1$	$LDO2_0$

Figure 9: Serial Programming Register Codes.

USE_USB Pin	CHG_2	CHG_1	CHG_0	Constant Current Charge I_{CH_CC}	Constant Current Charge as % of I_{SET} Current
1	0	0	0	100mA (fixed internally)	(default)
0	0	0	0	800mA (set by I_{SET} resistor)	100% (default)
X	0	0	1	640mA	80%
X	0	1	0	480mA	60%
X	0	1	1	320mA	40%
X	1	0	0	960mA	120%
X	1	0	1	1120mA	140%
X	1	1	0	1280mA	160%
X	1	1	1	1440mA	180%

Table 3: CHG Bit Setting for the Constant Current Charge Level (assuming I_{SET} resistor is set to default 800mA charge current).

Notes concerning the operation of the CHG_2, CHG_1 and CHG_0 bits or ISET code:

- Once the part is turned on using the $\overline{EN\_KEY}$ pin (and there is a BAT and/or CHGIN supply), and data is sent through I²C, the I²C codes in the registers will always be preserved until the part is shut down using the EN_HOLD (going low) or if the BAT and CHGIN supply are removed.
- If the part is turned on by connecting supply CHGIN (and not through $\overline{EN\_KEY}$), then when the CHGIN is removed, the part will shut down and all I²C registers will be cleared.

If USE_USB = L:
- The charge current is set by the ISET code in Register 0x00, bits 2,3,4. (code 000 will equal 100%)
- If the part has been turned on by $\overline{EN\_KEY}$ and CHGIN is disconnected then reconnected, it will still contain the code it had before (if it was 60% then it will remain 60%).
- If the part has NOT been turned on by $\overline{EN\_KEY}$ and CHGIN is disconnected then reconnected, it will be reset to 100% (since the whole part was shutdown).

If USE_USB = H:
- ISET Code 000 in Register 0x00, bits 2,3,4 = 100mA. The other codes stay the same as if USE_USB=H.
- If the part has been turned on by $\overline{EN\_KEY}$ and CHGIN is disconnected then reconnected, the ISET code will be forced to 000 and the current will be set to 100mA.
- The next time any I²C register is programmed (even if it is not for the ISET code), the ISET code will revert back to what it was before. For example, if the ISET code is set to 010 and USE_USB=H and the part was turned on with $\overline{EN\_KEY}$, then when CHGIN is disconnected then reconnected, the charger will be set to 100mA. Then if any other command is sent, the ISET code will remain 010.

$Term_1$	$Term_0$	Termination Current (as % of Constant Current Charge)
0	0	5% (default)
0	1	10%
1	0	15%
1	1	20%

Table 4: Term Bit Setting for the Termination Current Level.

$RCHG_1$	$RCHG_0$	Recharge Threshold
0	0	4.00V (default)
0	1	4.05V
1	0	4.10V
1	1	4.15V

Table 5: RCHG Bit Setting for the Battery Charger Recharge Voltage Level.

Timer	Charger Watchdog Timer
0	ON (default)
1	OFF (and reset to zero)

Table 6: Timer Bit Setting for the Charger Watchdog Timer.

$LDO1_1$	$LDO1_0$	LDO1 Output Voltage
0	0	3.30V (default)
0	1	2.90V
1	0	2.85V
1	1	2.80V
$LDO4_1$	$LDO4_0$	LDO4 Output Voltage
0	0	3.30V (default)
0	1	2.90V
1	0	2.85V
1	1	2.80V
$LDO5_1$	$LDO5_0$	LDO5 Output Voltage
0	0	3.30V (default)
0	1	2.90V
1	0	2.85V
1	1	2.80V

Table 7: LDO Bit Setting for LDO Output Voltage Level.

SYS Bit	SYSOUT Power Source
0	If USE_USB = H, SYSOUT powered from BAT If USE_USB = L, SYSOUT powered from CHGIN
1	SYSOUT always powered from BAT

Table 8: SYS Bit Setting for SYSOUT Power Path.

Layout Guidance

Figure 10 is the schematic for the evaluation board. The evaluation board has extra components for easy evaluation; the actual BOM need for a system is shown in Table 9. When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the AAT2601B:

1. The exposed pad EP must be reliably soldered to PGND/AGND and multilayer GND. The exposed thermal pad should be connected to board ground plane and pins 2 and 16. The ground plane should include a large exposed copper pad under the package with VIAs to all board layers for thermal dissipation.
2. The power traces, including GND traces, the LX traces and the VIN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several via pads when routing between layers.
3. The input capacitors (C1 and C2) should be connected as close as possible to CHGIN (Pin 28) and PGND (Pin 2) to get good power filtering.
4. Keep the switching node LX away from the sensitive OUTBUCK feedback node.
5. The feedback trace for the OUTBUCK pin should be separate from any power trace and connected as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation.
6. The output capacitor C4 and L1 should be connected as close as possible and there should not be any signal lines under the inductor.
7. The resistance of the trace from the load return to the PGND (Pin 2) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Quantity	Value	Designator	Footprint	Description
5	10µF	C1, C2, C3, C14, C15	0603	Capacitor, Ceramic, X5R, 6.3V, ±20%
2	22µF	C9	0805	Capacitor, Ceramic, 20%, 6.3V, X5R
4	4.7µF	C4, C5, C6, C7, C8	0603	Capacitor, Ceramic, 20%, 6.3V, X5R
3	0.1µF	C10, C11, C12	0402	Capacitor, Ceramic, 16V, 10%, X5R
1	0.01µF	C13	0402	Capacitor, Ceramic, 16V, 10%, X7R
1	3.3µH	L1	CDRH2D	Inductor, Sumida CDRH2D11NP-3R3NC
9	100K	R5, R8, R20, R21, R22, R23, R25, R26, R27	0402	Resistor, 5%
8	10K	R17, R19, R24, R29, R31, R32, R33, R37	0402	Resistor, 5%
1	1.24K	R18	0402	Resistor, 1%

Table 9: Minimum AAT2601B Bill of Materials.

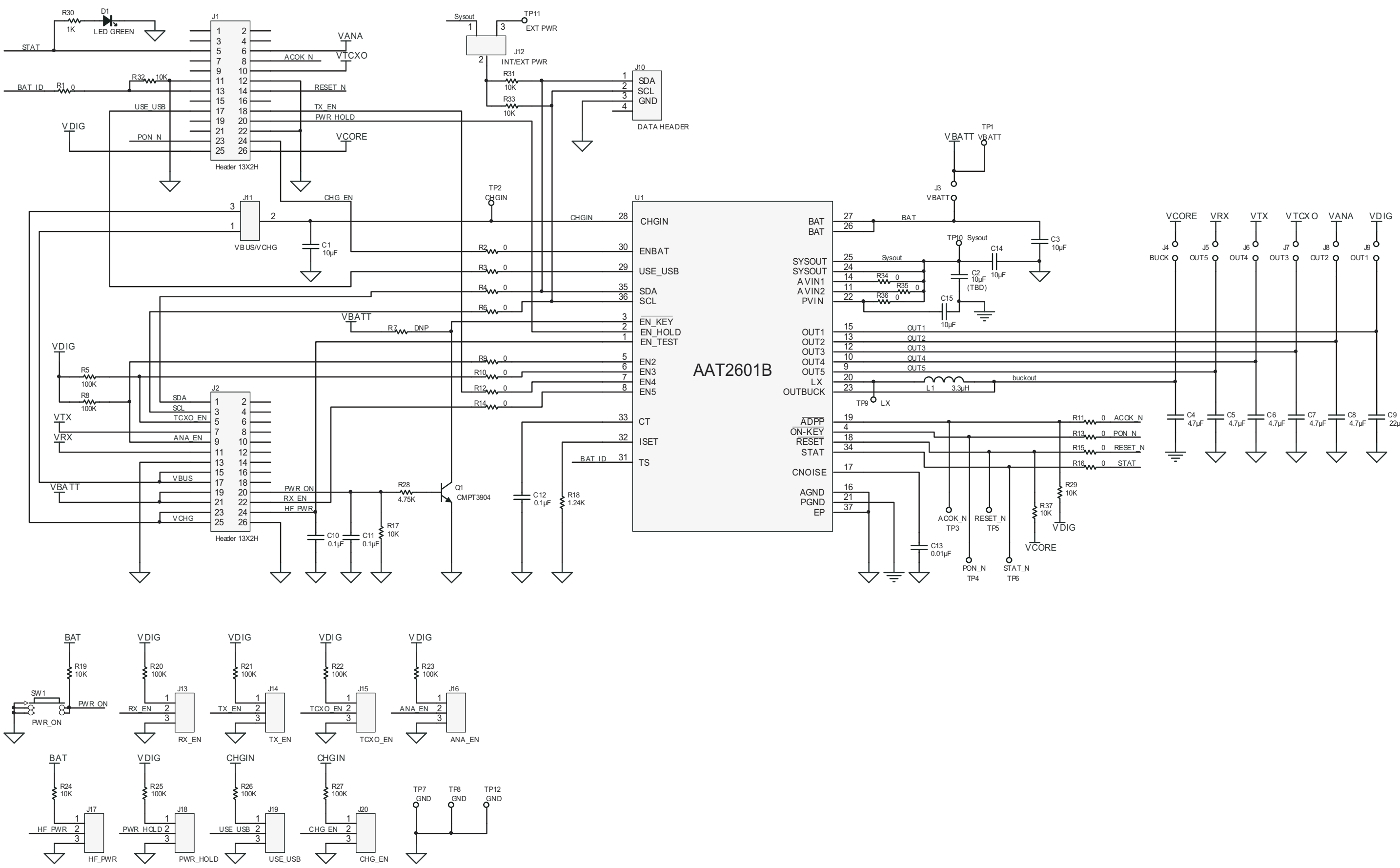


Figure 10: AAT2601B Evaluation Kit Schematic.

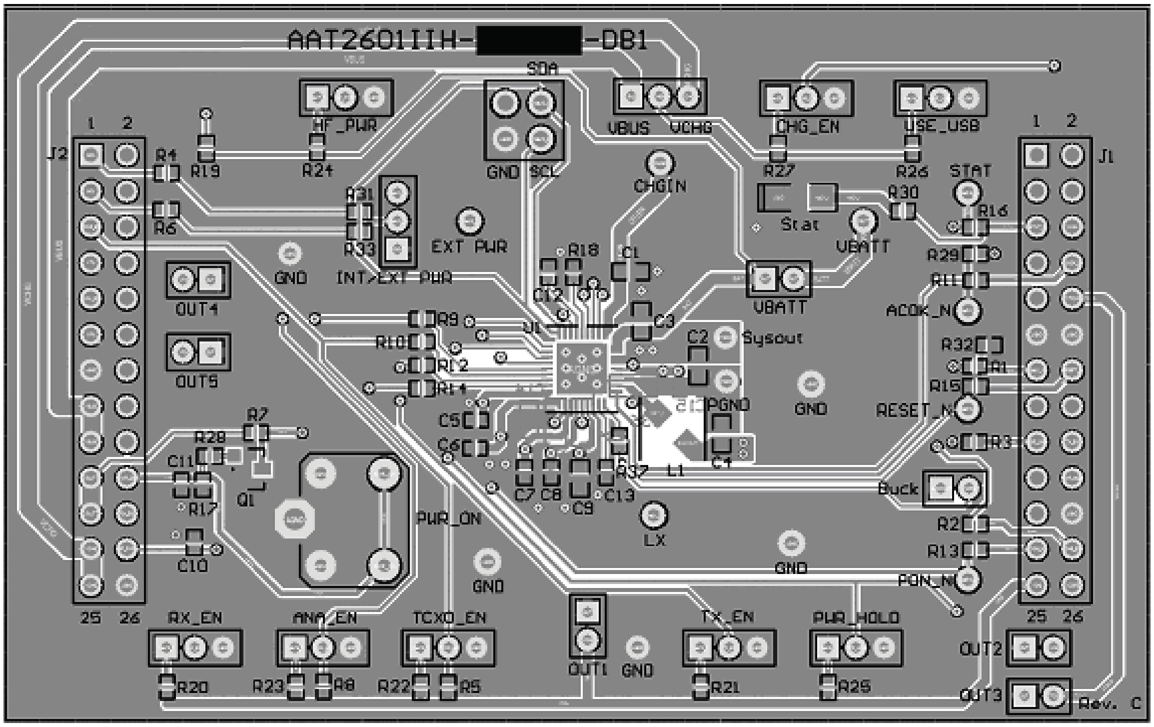


Figure 11: AAT2601B Evaluation Kit Top Layer.

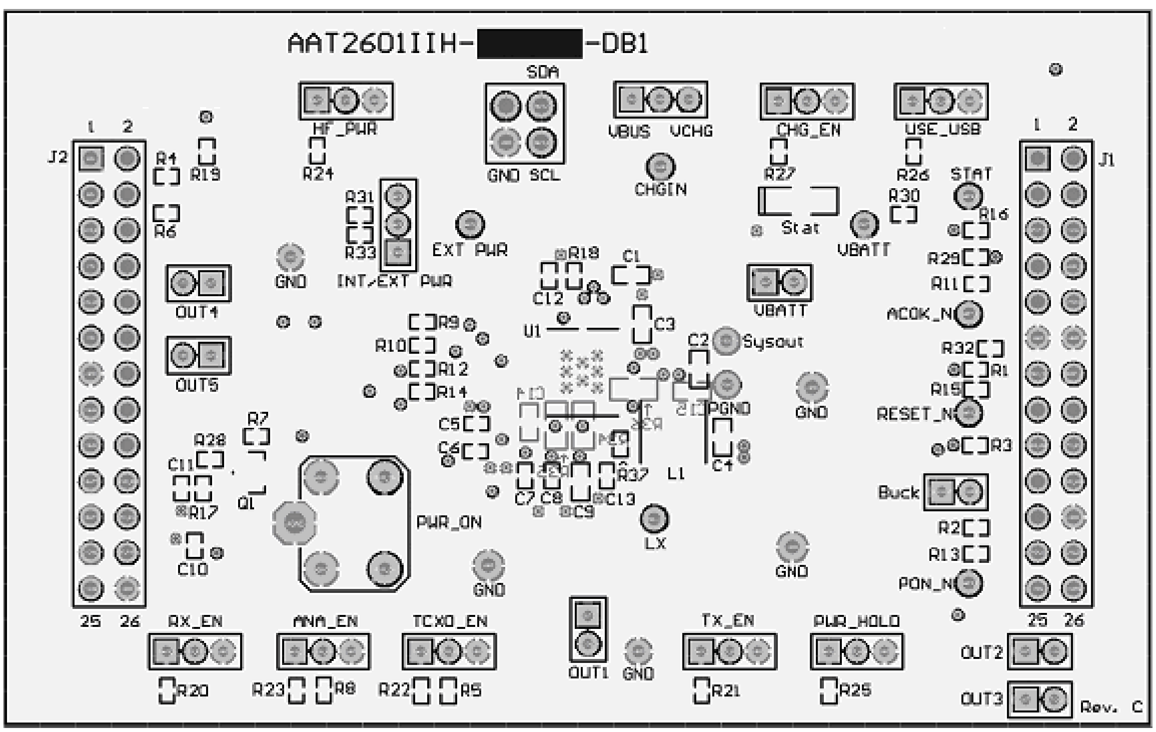


Figure 12: AAT2601B Evaluation Kit Mid1 Layer.

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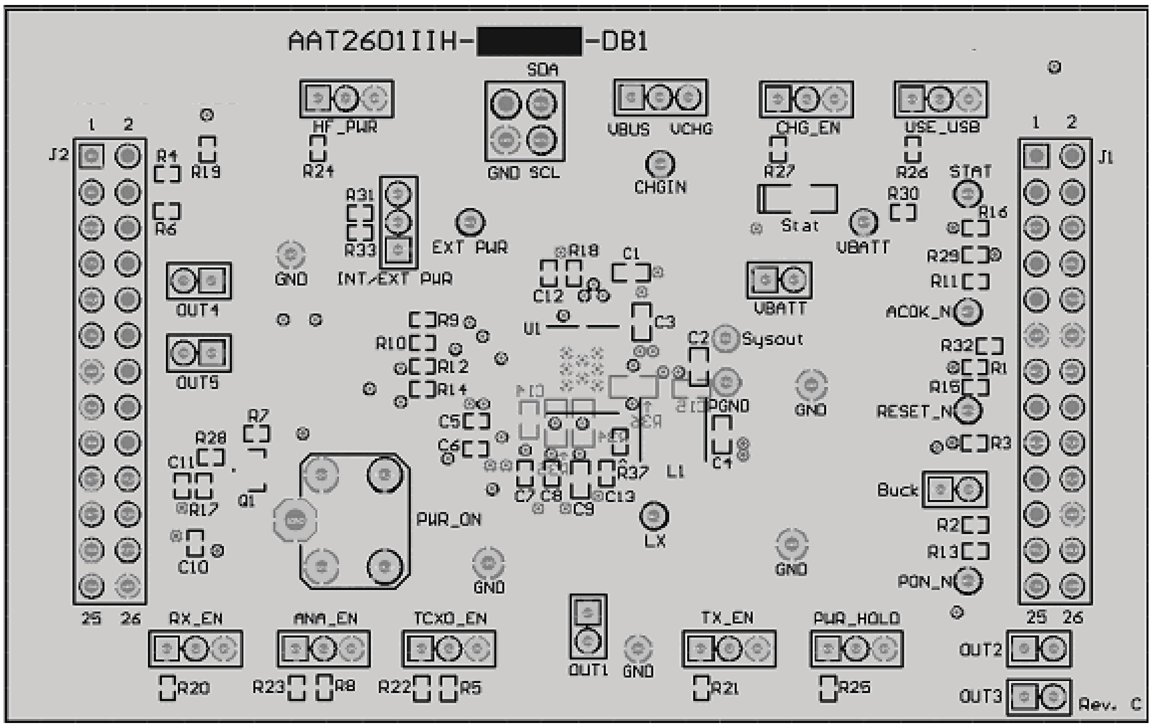


Figure 13: AAT2601B Evaluation Kit Mid2 Layer.

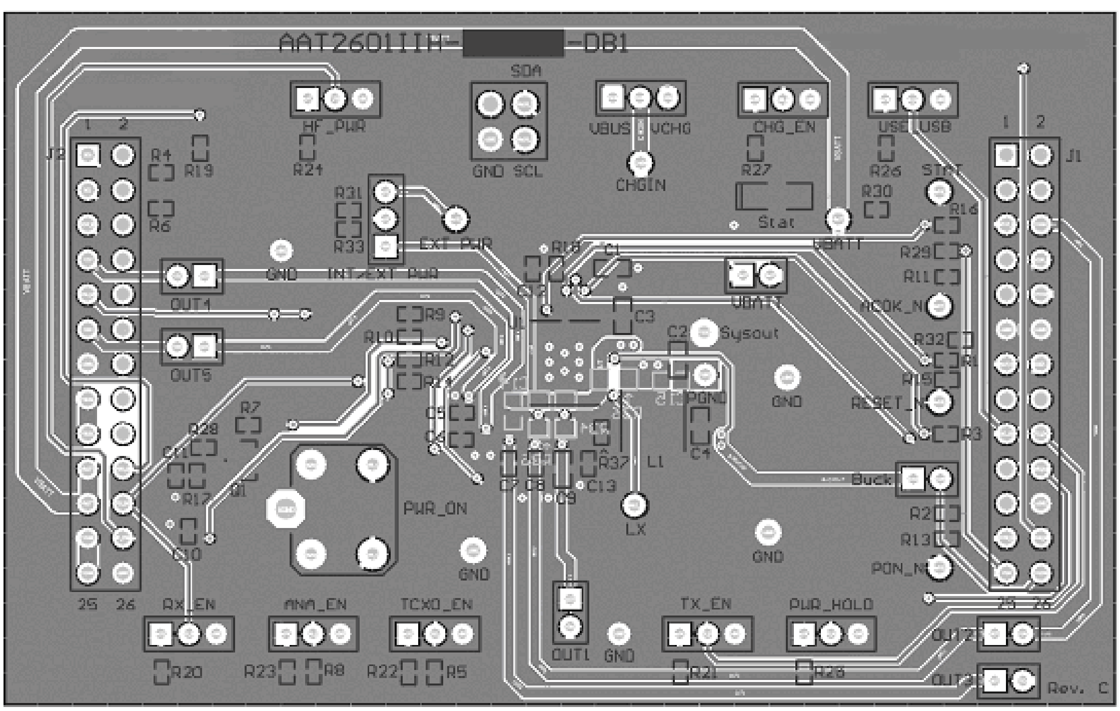


Figure 14: AAT2601B Evaluation Kit Bottom Layer.

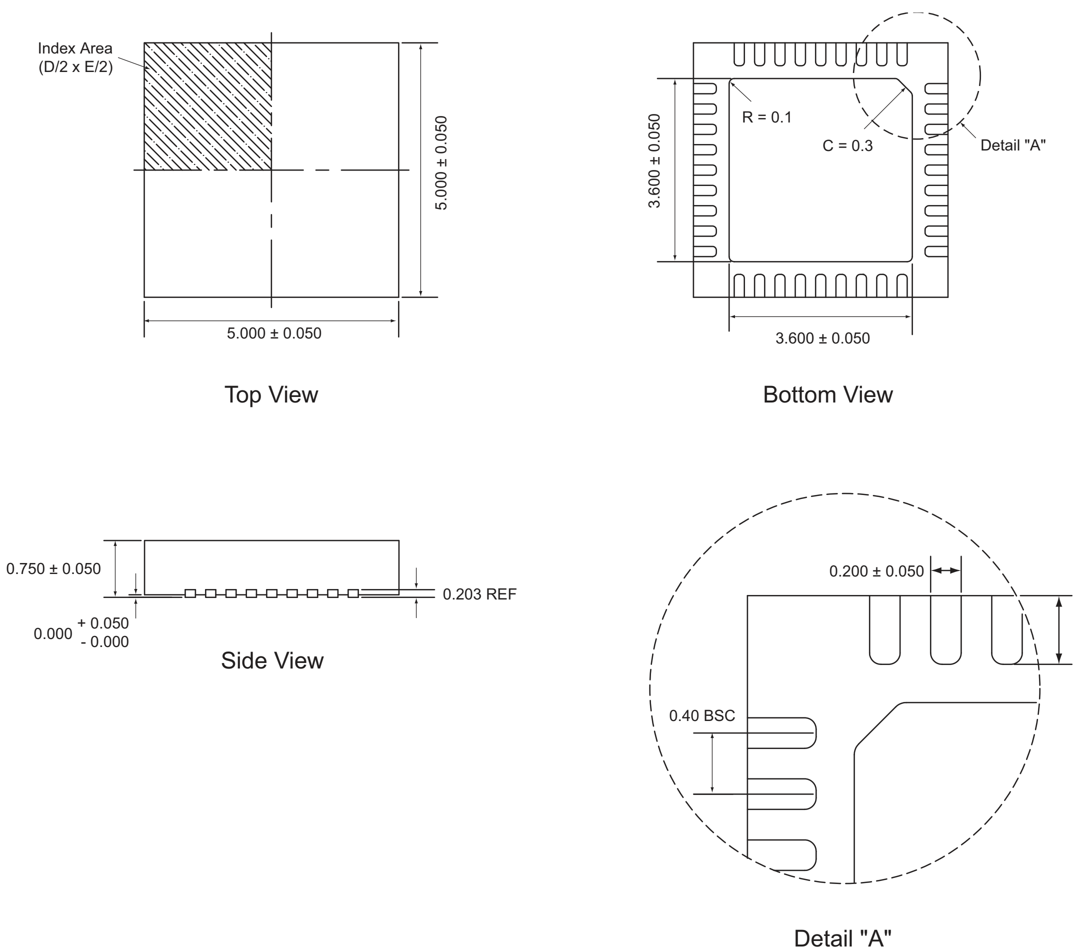
Ordering Information

Package	Part Marking[1]	Part Number (Tape and Reel)[2]
TQFN55-36	9CXYY	AAT2601BIIH-T1

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Packaging Information

TQFN55-36[3]



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in BOLD.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.