

CDCE937 Flexible Low Power LVCMOS Clock Generator With SSC Support For EMI Reduction

1 Features

- Member of Programmable Clock Generator Family
 - CDCE913: 1-PLL, 3 Outputs
 - CDCE925: 2-PLL, 5 Outputs
 - *CDCE937: 3-PLL, 7 Outputs*
 - CDCE949: 4-PLL, 9 Outputs
- In-System Programmability and EEPROM
 - Serial Programmable Volatile Register
 - Nonvolatile EEPROM to Store Customer Setting
- Flexible Input Clocking Concept
 - External Crystal: 8 MHz to 32 MHz
 - On-Chip VCXO: Pull Range ± 150 ppm
 - Single-Ended LVCMOS up to 160 MHz
- Free Selectable Output Frequency up to 230 MHz
- Low-Noise PLL Core
 - PLL Loop Filter Components Integrated
 - Low Period Jitter (Typical 60 ps)
- Separate Output Supply Pins
 - CDCE937: 3.3 V and 2.5 V
 - CDCEL937: 1.8 V
- Flexible Clock Driver
 - Three User-Definable Control Inputs [S0/S1/S2], for Example, SSC Selection, Frequency Switching, Output Enable or Power Down
 - Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Bluetooth™, WLAN, Ethernet™, and GPS
 - Generates Common Clock Frequencies Used With TI-DaVinci™, OMAP™, DSPs
 - Programmable SSC Modulation
 - Enables 0-PPM Clock Generation
- 1.8-V Device Power Supply
- Wide Temperature Range -40°C to 85°C
- Packaged in TSSOP
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)

2 Applications

D-TVs, STBs, IP-STBs, DVD Players, DVD Recorders, and Printers

3 Description

The CDCE937 and CDCEL937 devices are modular PLL-based low cost, high-performance, programmable clock synthesizers, multipliers and dividers. They generate up to 7 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to three independent configurable PLLs.

The CDCE937 has separate output supply pins, VDDOUT, which is 1.8 V for CDCEL937 and to 2.5 V to 3.3 V for CDCE937.

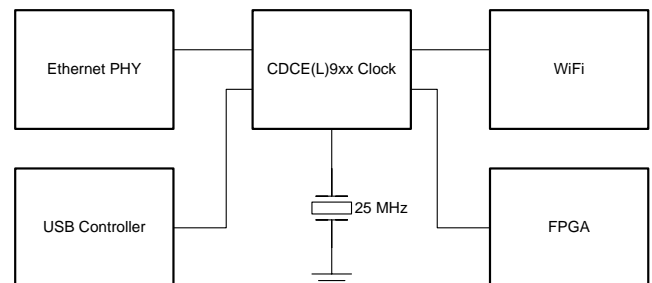
The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal, that is, PWM signal.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------------|------------|-------------------|
| CDCE937, CDCEL937 | TSSOP (20) | 6.50 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (March 2010) to Revision G | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Changed <i>Applications</i> | 1 |
| • Changed Thermal Resistance Junction to Ambient, $R_{\theta JA}$, values in <i>Thermal Information</i> From: 89 (0 lfm), 75 (150 lfm), 74 (200 lfm), 74 (250 lfm), and 69 (500 lfm) To: 89.04 | 6 |
| • Deleted <i>Input Capacitance</i> figure | 19 |

| Changes from Revision E (October 2009) to Revision F | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Added PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$ foot to PLL1, PLL2, and PLL3 Configure Register Table | 20 |
| • Changed $100 \text{ MHz} < f_{VCO} > 200 \text{ MHz}$; TO $80 \text{ MHz} \leq f_{VCO} \leq 230 \text{ MHz}$; and changed $0 \leq p \leq 7$ TO $0 \leq p \leq 4$ | 26 |
| • Changed under Example, fifth row, N", 2 places TO N' | 26 |

| Changes from Revision D (September 2009) to Revision E | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Deleted sentence - A different default setting can be programmed on customer request. Contact Texas Instruments sales or marketing representative for more information. | 14 |

| Changes from Revision C (January 2009) to Revision D | Page |
|---------------------------------------------------------------------------------------------------------------------|-------------|
| • Added Note 3: SDA and SCL can go up to 3.6 V as stated in the <i>Recommended Operating Conditions</i> table | 5 |

Changes from Revision B (December 2007) to Revision C **Page**

- Changed *Generic Configuration Register* table SLAVE_ADR default value From: 00b To: 01b [18](#)
-

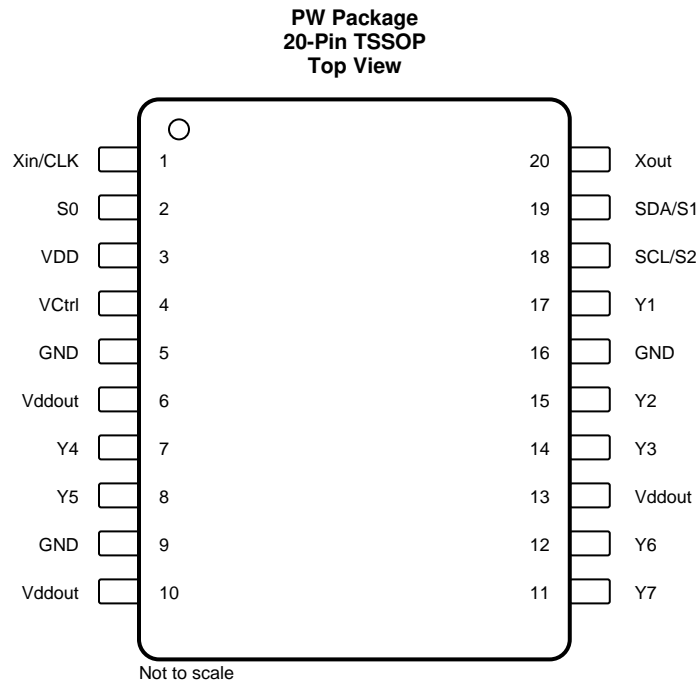
Changes from Revision A (September 2007) to Revision B **Page**

- Changed Terminal Functions Table - the pin numbers to correspond with pin outs on the package [4](#)
 - Changed *Generic Configuration Register* table RID default From: 0h To: Xb [18](#)
 - Added note to PWDN description to *Generic Configuration Register* table [18](#)
-

Changes from Original (August 2007) to Revision A **Page**

- Changed the data sheet status From: Product Preview To: Production data [1](#)
-

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------------|-----------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NO. | | |
| GND | 5, 9, 16 | G | Ground |
| SCL/S2 | 18 | I | SCL: Serial clock input (default configuration), LVCMOS; Internal pullup 500k; S2: User programmable control input; LVCMOS inputs; Internal pullup 500k |
| SDA/S1 | 19 | I/O | SDA: Bi-directional serial data input/output (default configuration). LVCMOS; Internal pullup 500k; S1: User programmable control input; LVCMOS inputs; Internal pullup 500k |
| S0 | 2 | I | User programmable control input S0; LVCMOS inputs; Internal pullup 500k |
| V _{Ctrl} | 4 | I | VCXO control voltage, leave open or pullup (approximately 500k) when not used |
| V _{DD} | 3 | P | 1.8-V power supply for the device |
| Vddout | 6, 10, 13 | P | CDCEL937: 1.8-V supply for all outputs CDCE937: 3.3-V or 2.5-V supply for all outputs |
| Xin/CLK | 1 | I | Crystal oscillator input or LVCMOS clock input (selectable through SDA/SCL bus) |
| Xout | 20 | O | Crystal oscillator output, leave open or pullup (~500k) when not used |
| Y1 | 17 | O | LVCMOS outputs |
| Y2 | 15 | O | LVCMOS outputs |
| Y3 | 14 | O | LVCMOS outputs |
| Y4 | 7 | O | LVCMOS outputs |
| Y5 | 8 | O | LVCMOS outputs |
| Y6 | 12 | O | LVCMOS outputs |
| Y7 | 11 | O | LVCMOS outputs |

(1) G= Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|-----------------------------------------------------|------|-------------------|------|
| Supply voltage, V_{DD} | -0.5 | 2.5 | V |
| Input voltage, V_I ⁽²⁾⁽³⁾ | -0.5 | $V_{DD} + 0.5$ | V |
| Output voltage, V_O ⁽²⁾ | -0.5 | $V_{DDout} + 0.5$ | V |
| Input current, I_I ($V_I < 0$, $V_I > V_{DD}$) | | 20 | mA |
| Continuous output current, I_O | | 50 | mA |
| Junction temperature, T_J | | 125 | °C |
| Storage temperature, T_{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) SDA and SCL can go up to 3.6 V as stated in [Recommended Operating Conditions](#).

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------------------------|---------------------------------------------------------------------------|---------------------------------------------------|---------------------|---------------------|------|
| V_{DD} | Device supply voltage | 1.7 | 1.8 | 1.9 | V |
| V_O | Output Yx supply voltage, V_{DDout} | CDCE937 | | 3.6 | V |
| | | CDCEL937 | 1.7 | 1.9 | |
| V_{IL} | Low-level input voltage LVCMOS | | | $0.3 \times V_{DD}$ | V |
| V_{IH} | High-level input voltage LVCMOS | $0.7 \times V_{DD}$ | | | V |
| $V_{I(thresh)}$ | Input voltage threshold LVCMOS | | $0.5 \times V_{DD}$ | | V |
| V_{IS} | Input voltage | S0 | 0 | 1.9 | V |
| | | S1, S2, SDA, SCL, $V_{I(thresh)} = 0.5 V_{DD}$ | 0 | 3.6 | |
| $V_{I(CLK)}$ | Input voltage, CLK | 0 | | 1.9 | V |
| I_{OH} / I_{OL} | Output current | $V_{DDout} = 3.3$ V | | ±12 | mA |
| | | $V_{DDout} = 2.5$ V | | ±10 | |
| | | $V_{DDout} = 1.8$ V | | ±8 | |
| C_L | Output load LVCMOS | | | 10 | pF |
| T_A | Operating free-air temperature | -40 | | 85 | °C |
| CRYSTAL AND VCXO⁽¹⁾ | | | | | |
| f_{Xtal} | Crystal input frequency (fundamental mode) | 8 | 27 | 32 | MHz |
| ESR | Effective series resistance | | | 100 | Ω |
| f_{PR} | Pulling ($0 \text{ V} \leq V_{ctrl} \leq 1.8 \text{ V}$) ⁽²⁾ | ±120 | ±150 | | ppm |
| | Frequency control voltage, V_{ctrl} | 0 | | V_{DD} | V |
| C_0/C_1 | Pullability ratio | | | 220 | |

- (1) For more information about VCXO configuration, and crystal recommendation, see [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).
- (2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).

Recommended Operating Conditions (continued)

| | | MIN | NOM | MAX | UNIT |
|-------|------------------------------------------|-----|-----|-----|------|
| C_L | On-chip load capacitance at Xin and Xout | 0 | | 20 | pF |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | CDCE937, CDCEL937 | UNIT |
|-------------------------------|----------------------------------------------|----------------------|------|
| | | PW (TSSOP) | |
| | | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 89.04 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 31.33 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.6 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 0.8 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 48.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------|--------------------|------|------|
| I_{DD} | Supply current (see Figure 1) | All outputs off, $f_{(CLK)} = 27$ MHz, $f_{(VCO)} = 135$ MHz | All PLLS on | | 29 | mA |
| | | | Per PLL | | 9 | |
| I_{DDOUT} | Output supply current (see Figure 2 and Figure 3) | No load, all outputs on, $f_{OUT} = 27$ MHz | CDCE937, $V_{DDOUT} = 3.3$ V | | 3.1 | mA |
| | | | CDCEL937, $V_{DDOUT} = 1.8$ V | | 1.5 | |
| $I_{DD(PD)}$ | Power-down current | Every circuit powered down except SDA/SCL, $f_{IN} = 0$ MHz, $V_{DD} = 1.9$ V | | | 50 | μA |
| $V_{(PUC)}$ | Supply voltage Vdd threshold for power-up control circuit | | 0.85 | | 1.45 | V |
| $f_{(VCO)}$ | VCO frequency range of PLL | | 80 | | 230 | MHz |
| f_{OUT} | LVCMOS output frequency | $V_{ddout} = 3.3$ V | | | 230 | MHz |
| | | $V_{ddout} = 1.8$ V | | | 230 | |
| LVCMOS PARAMETER | | | | | | |
| V_{IK} | LVCMOS input voltage | $V_{DD} = 1.7$ V, $I_I = -18$ mA | | | -1.2 | V |
| I_I | LVCMOS Input current | $V_I = 0$ V or V_{DD} , $V_{DD} = 1.9$ V | | | ±5 | μA |
| I_{IH} | LVCMOS Input current for S0/S1/S2 | $V_I = V_{DD}$, $V_{DD} = 1.9$ V | | | 5 | μA |
| I_{IL} | LVCMOS Input current for S0/S1/S2 | $V_I = 0$ V, $V_{DD} = 1.9$ V | | | -4 | μA |
| C_I | Input capacitance at Xin/Clk | $V_{I(CLK)} = 0$ V or V_{DD} | | | 6 | pF |
| | Input capacitance at Xout | $V_{I(Xout)} = 0$ V or V_{DD} | | | 2 | |
| | Input capacitance at S0/S1/S2 | $V_{IS} = 0$ V or V_{DD} | | | 3 | |
| CDCE937 – LVCMOS FOR Vddout = 3.3 V | | | | | | |
| V_{OH} | LVCMOS high-level output voltage | $V_{ddout} = 3$ V, $I_{OH} = -0.1$ mA | | | 2.9 | V |
| | | $V_{ddout} = 3$ V, $I_{OH} = -8$ mA | | | 2.4 | |
| | | $V_{ddout} = 3$ V, $I_{OH} = -12$ mA | | | 2.2 | |
| V_{OL} | LVCMOS low-level output voltage | $V_{ddout} = 3$ V, $I_{OL} = 0.1$ mA | | | 0.1 | V |
| | | $V_{ddout} = 3$ V, $I_{OL} = 8$ mA | | | 0.5 | |
| | | $V_{ddout} = 3$ V, $I_{OL} = 12$ mA | | | 0.8 | |
| t_{PLH}, t_{PHL} | Propagation delay | All PLL bypass | | | 3.2 | ns |
| t_r/t_f | Rise and fall time | $V_{ddout} = 3.3$ V (20%–80%) | | | 0.6 | ns |

(1) All typical values are at respective nominal V_{DD} .

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------------------------------------|---------------------------------------------|------------------------------------------------------------|-----------------------|--------------------|-----------------------|------|
| t _{jitter(cc)} | Cycle-to-cycle jitter ⁽²⁾⁽³⁾ | 1 PLL switching, Y2-to-Y3 | | 60 | 90 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 100 | 150 | |
| t _{jitter(per)} | Peak-to-peak period jitter ⁽³⁾ | 1 PLL switching, Y2-to-Y3 | | 70 | 100 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 120 | 180 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ (see Table 2) | f _{OUT} = 50 MHz, Y1-to-Y3 | | | 60 | ps |
| | | f _{OUT} = 50 MHz, Y2-to-Y5 | | | 160 | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz, Pdiv = 1 | 45% | | 55% | |
| CDCE937 – LVCMOS FOR V_{ddout} = 2.5 V | | | | | | |
| V _{OH} | LVCMOS high-level output voltage | V _{ddout} = 2.3 V, I _{OH} = -0.1 mA | 2.2 | | | V |
| | | V _{ddout} = 2.3 V, I _{OH} = -6 mA | 1.7 | | | |
| | | V _{ddout} = 2.3 V, I _{OH} = -10 mA | 1.6 | | | |
| V _{OL} | LVCMOS low-level output voltage | V _{ddout} = 2.3 V, I _{OL} = 0.1 mA | | | 0.1 | V |
| | | V _{ddout} = 2.3 V, I _{OL} = 6 mA | | | 0.5 | |
| | | V _{ddout} = 2.3 V, I _{OL} = 10 mA | | | 0.7 | |
| t _{PLH} , t _{PHL} | Propagation delay | All PLL bypass | | 3.4 | | ns |
| t _r /t _f | Rise and fall time | V _{ddout} = 2.5 V (20%–80%) | | 0.8 | | ns |
| t _{jitter(cc)} | Cycle-to-cycle jitter ⁽²⁾⁽³⁾ | 1 PLL switching, Y2-to-Y3 | | 60 | 90 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 100 | 150 | |
| t _{jitter(per)} | Peak-to-peak period jitter ⁽⁴⁾ | 1 PLL switching, Y2-to-Y3 | | 70 | 100 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 120 | 180 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ (see Table 2) | f _{OUT} = 50 MHz, Y1-to-Y3 | | | 60 | ps |
| | | f _{OUT} = 50 MHz, Y2-to-Y5 | | | 160 | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz, Pdiv = 1 | 45% | | 55% | |
| CDCEL937 – LVCMOS FOR V_{ddout} = 1.8 V | | | | | | |
| V _{OH} | LVCMOS high-level output voltage | V _{ddout} = 1.7 V, I _{OH} = -0.1 mA | 1.6 | | | V |
| | | V _{ddout} = 1.7 V, I _{OH} = -4 mA | 1.4 | | | |
| | | V _{ddout} = 1.7 V, I _{OH} = -8 mA | 1.1 | | | |
| V _{OL} | LVCMOS low-level output voltage | V _{ddout} = 1.7 V, I _{OL} = 0.1 mA | | | 0.1 | V |
| | | V _{ddout} = 1.7 V, I _{OL} = 4 mA | | | 0.3 | |
| | | V _{ddout} = 1.7 V, I _{OL} = 8 mA | | | 0.6 | |
| t _{PLH} , t _{PHL} | Propagation delay | All PLL bypass | | 2.6 | | ns |
| t _r /t _f | Rise and fall time | V _{ddout} = 1.8 V (20%–80%) | | 0.7 | | ns |
| t _{jitter(cc)} | Cycle-to-cycle jitter ⁽²⁾⁽³⁾ | 1 PLL switching, Y2-to-Y3 | | 70 | 120 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 100 | 150 | |
| t _{jitter(per)} | Peak-to-peak period jitter ⁽³⁾ | 1 PLL switching, Y2-to-Y3 | | 90 | 140 | ps |
| | | 3 PLL switching, Y2-to-Y7 | | 120 | 190 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ (see Table 2) | f _{OUT} = 50 MHz, Y1-to-Y3 | | | 60 | ps |
| | | f _{OUT} = 50 MHz, Y2-to-Y5 | | | 160 | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz, Pdiv = 1 | 45% | | 55% | |
| SDA AND SCL | | | | | | |
| V _{IK} | SCL and SDA input clamp voltage | V _{DD} = 1.7 V; I _I = -18 mA | | | -1.2 | V |
| I _{IH} | SCL and SDA input current | V _I = V _{DD} ; V _{DD} = 1.9 V | | | ±10 | μA |
| V _{IH} | SDA/SCL input high voltage ⁽⁶⁾ | | 0.7 × V _{DD} | | | V |
| V _{IL} | SDA/SCL input low voltage ⁽⁶⁾ | | | | 0.3 × V _{DD} | V |

(2) 10000 cycles.

 (3) Jitter depends on configuration. Data is taken under the following conditions: 1-PLL is f_{IN} = 27 MHz and Y2/3 = 27 MHz (measured at Y2); 3-PLL is f_{IN} = 27 MHz, Y2/3 = 27 MHz (measured at Y2), Y4/5 = 16.384 MHz, and Y6/7 = 74.25 MHz.

(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and outputs are generated from the same divider; data taken on rising edge (tr).

(5) odc depends on output rise and fall time (tr/tf).

(6) SDA and SCL pins are 3.3-V tolerant.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------|------------------------------|-------------------------------------------------|-----|--------------------|-----------------------|------|
| V _{OL} | SDA low-level output voltage | I _{OL} = 3 mA, V _{DD} = 1.7 V | | | 0.2 × V _{DD} | V |
| C _I | SCL/SDA Input capacitance | V _I = 0 V or V _{DD} | | 3 | 10 | pF |

6.6 Timing Requirements: CLK_IN

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---------------------------------|--------------------------------------------|-----------------|-----|-----|------|
| f _{CLK} | LVCMOS clock input frequency | PLL bypass mode | 0 | 160 | MHz |
| | | PLL mode | 8 | 160 | |
| t _r / t _f | Rise and fall time CLK signal (20% to 80%) | | | 3 | ns |
| duty _{CLK} | Duty cycle CLK at V _{DD} /2 | 40% | | 60% | |

6.7 Timing Requirements: SDA/SCL

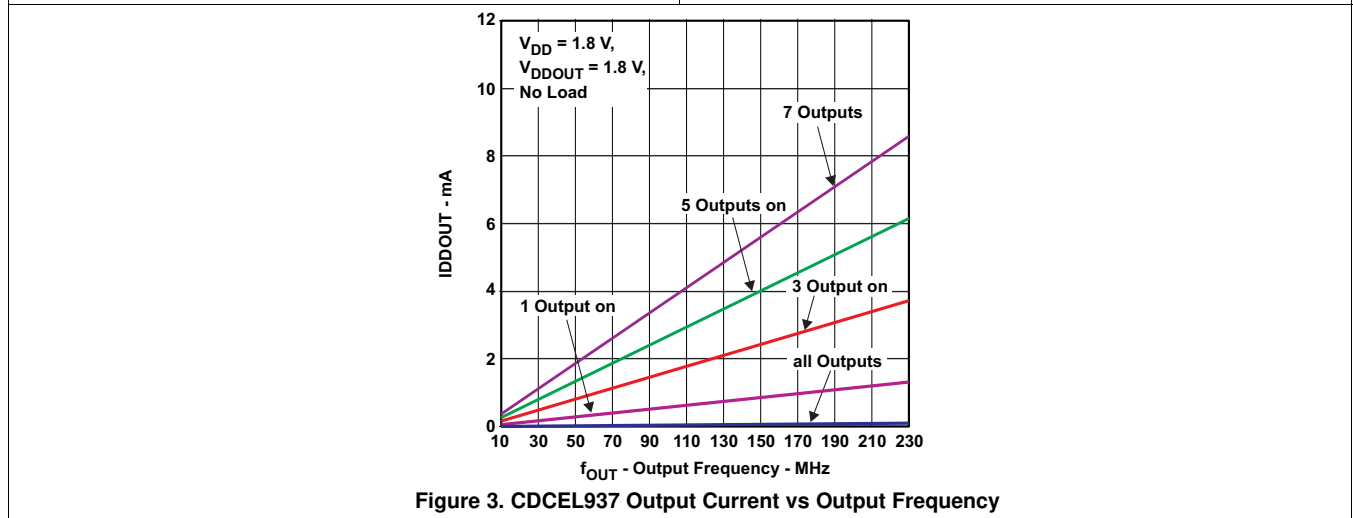
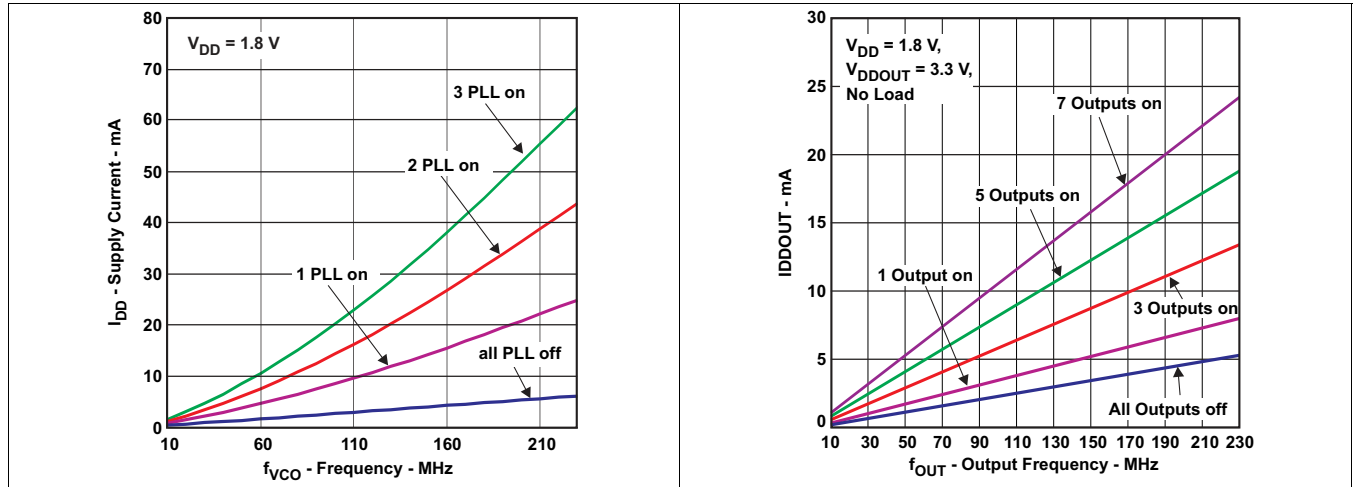
over operating free-air temperature range (unless otherwise noted; see [Figure 7](#))

| | | MIN | NOM | MAX | UNIT |
|-------------------------|--------------------------------------------------|---------------|-----|------|------|
| f _{SCL} | SCL clock frequency | Standard mode | 0 | 100 | kHz |
| | | Fast mode | 0 | 400 | |
| t _{su} (START) | START setup time (SCL high before SDA low) | Standard mode | 4.7 | | μs |
| | | Fast mode | 0.6 | | |
| t _h (START) | START hold time (SCL low after SDA low) | Standard mode | 4 | | μs |
| | | Fast mode | 0.6 | | |
| t _w (SCLL) | SCL low-pulse duration | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | |
| t _w (SCLH) | SCL high-pulse duration | Standard mode | 4 | | μs |
| | | Fast mode | 0.6 | | |
| t _h (SDA) | SDA hold time (SDA valid after SCL low) | Standard mode | 0 | 3.45 | μs |
| | | Fast mode | 0 | 0.9 | |
| t _{su} (SDA) | SDA setup time | Standard mode | 250 | | ns |
| | | Fast mode | 100 | | |
| t _r | SCL/SDA input rise time | Standard mode | | 1000 | ns |
| | | Fast mode | | 300 | |
| t _f | SCL/SDA input fall time | Standard mode | | 300 | ns |
| | | Fast mode | | 300 | |
| t _{su} (STOP) | STOP setup time | Standard mode | 4 | | μs |
| | | Fast mode | 0.6 | | |
| t _{BUS} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | |

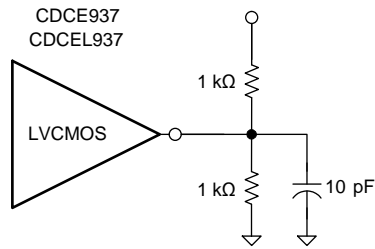
6.8 EEPROM Specification

| | | MIN | TYP | MAX | UNIT |
|-------|------------------------------|------|-----|-----|--------|
| EEcyc | Programming cycles of EEPROM | 1000 | | | cycles |
| EEret | Data retention | 10 | | | years |

6.9 Typical Characteristics

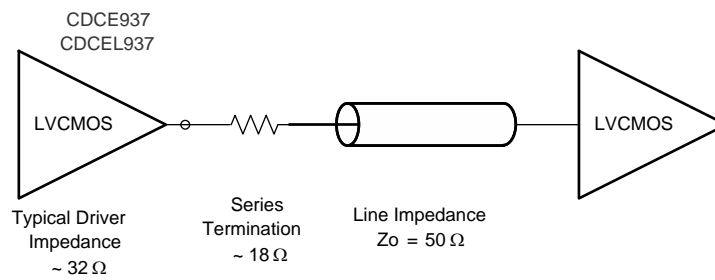


7 Parameter Measurement Information



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Figure 4. Test Load



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Figure 5. Test Load for 50-Ω Board Environment

8 Detailed Description

8.1 Overview

The CDCE937 and CDCEL937 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. They generate up to seven output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using one of the three integrated configurable PLLs. The CDCx937 has separate output supply pins, VDDOUT, which is 1.8 V for CDCEL937 and 2.5 V to 3.3 V for CDCE937.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF.

Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M/N divider ratio allows the generation of 0 ppm audio/video, networking (WLAN, BlueTooth, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency such as 27 MHz.

All PLLs supports SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking which is a common technique to reduce electro-magnetic interference (EMI).

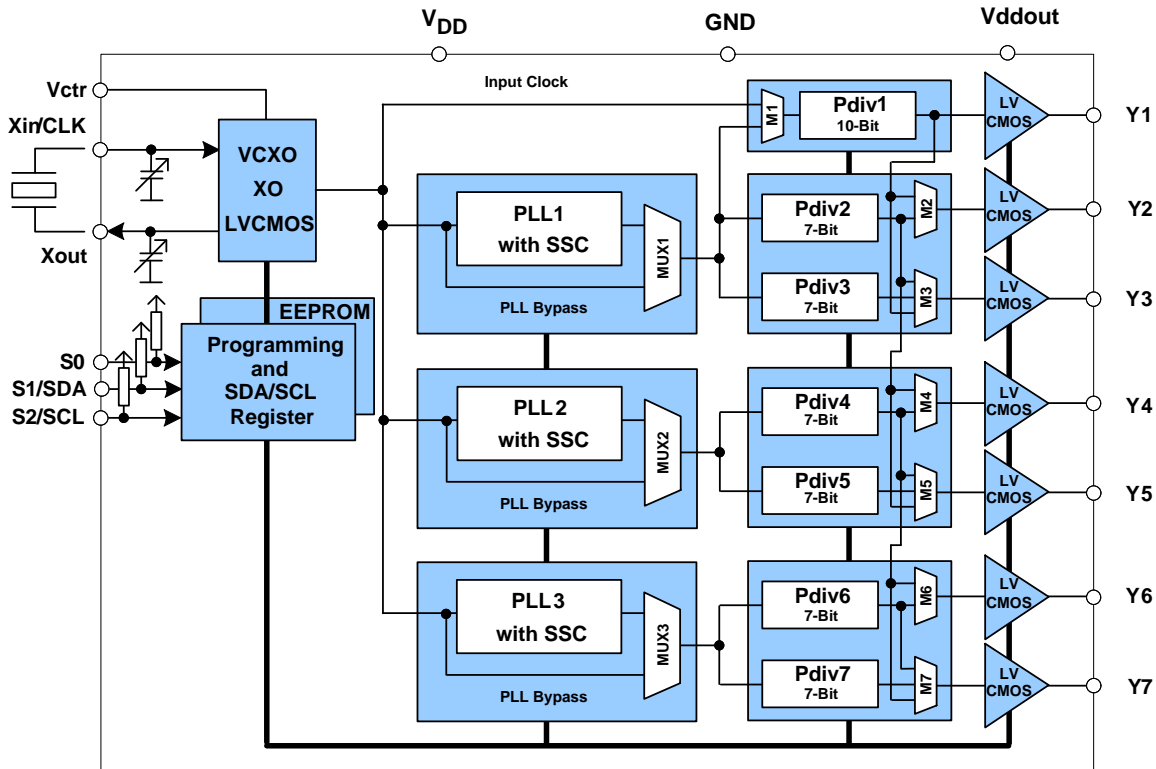
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports non-volatile EEPROM programming for ease-customized application. It is preset to a factory default configuration (see [Default Device Setting](#)). It can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through SDA/SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for output-disable function.

The CDCx937 operates in a 1.8-V environment. It is characterized for operation from -40°C to 85°C .

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Control Terminal Setting

The CDCE937 has three user-definable control terminals (S0, S1, and S2) which allow external control of device settings. They can be programmed to any of the following setting:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power down control

The user can predefine up to eight different control settings. [Table 1](#) and [Table 2](#) explain these settings.

Table 1. Control Terminal Definition

| EXTERNAL CONTROL BITS | PLL1 SETTING | | | PLL2 SETTING | | | PLL3 SETTING | | | Y1 SETTING |
|-----------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|------------------------------------|
| | PLL Frequency Selection | SSC Selection | Output Y2/Y3 Selection | PLL Frequency Selection | SSC Selection | Output Y4/Y5 Selection | PLL Frequency Selection | SSC Selection | Output Y6/Y7 Selection | Output Y1 and Power-Down Selection |
| Control Function | | | | | | | | | | |

Table 2. PLLx Setting (Can Be Selected for Each PLL Individual)

| SSC SELECTION (CENTER/DOWN) ⁽¹⁾ | | | | |
|--------------------------------------------|---|---|----------|----------|
| SSCx [3-bits] | | | CENTER | DOWN |
| 0 | 0 | 0 | 0% (off) | 0% (off) |
| 0 | 0 | 1 | ±0.25% | -0.25% |
| 0 | 1 | 0 | ±0.5% | -0.5% |

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register

Table 2. PLLx Setting (Can Be Selected for Each PLL Individual) (continued)

| SSC SELECTION (CENTER/DOWN) ⁽¹⁾ | | | | |
|---------------------------------------------|---|------------|--------|--------|
| SSCx [3-bits] | | | CENTER | DOWN |
| 0 | 1 | 1 | ±0.75% | –0.75% |
| 1 | 0 | 0 | ±1% | –1% |
| 1 | 0 | 1 | ±1.25% | –1.25% |
| 1 | 1 | 0 | ±1.5% | –1.5% |
| 1 | 1 | 1 | ±2% | –2% |
| FREQUENCY SELECTION ⁽²⁾ | | | | |
| FSx | | FUNCTION | | |
| 0 | | Frequency0 | | |
| 1 | | Frequency1 | | |
| OUTPUT SELECTION ⁽³⁾ (Y2 ... Y7) | | | | |
| YxYx | | FUNCTION | | |
| 0 | | State0 | | |
| 1 | | State1 | | |

(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range

(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 3. Y1 Setting⁽¹⁾

| Y1 SELECTION | |
|--------------|----------|
| Y1 | FUNCTION |
| 0 | State 0 |
| 1 | State 1 |

(1) State0 and State1 are user definable in Generic Configuration Register and can be power down, 3-state, low, or active.

S1/SDA and S2/SCL pins of the CDCEx937 are dual function pins. In default configuration they are defined as SDA/SCL for the serial interface. They can be programmed as control-pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes to the Control register (Bit [6] of Byte [02]) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL).

S0 is not a multi-use pin, it is a control pin only.

8.3.2 Default Device Setting

The internal EEPROM of CDCEx937 is preconfigured as shown in [Figure 6](#). (The input frequency is passed through to the output as a default.) This allows the device to operate in default mode without the extra production step of program it. The default setting appears after power is supplied or after power-down or power-up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed through the serial SDA/SCL Interface.

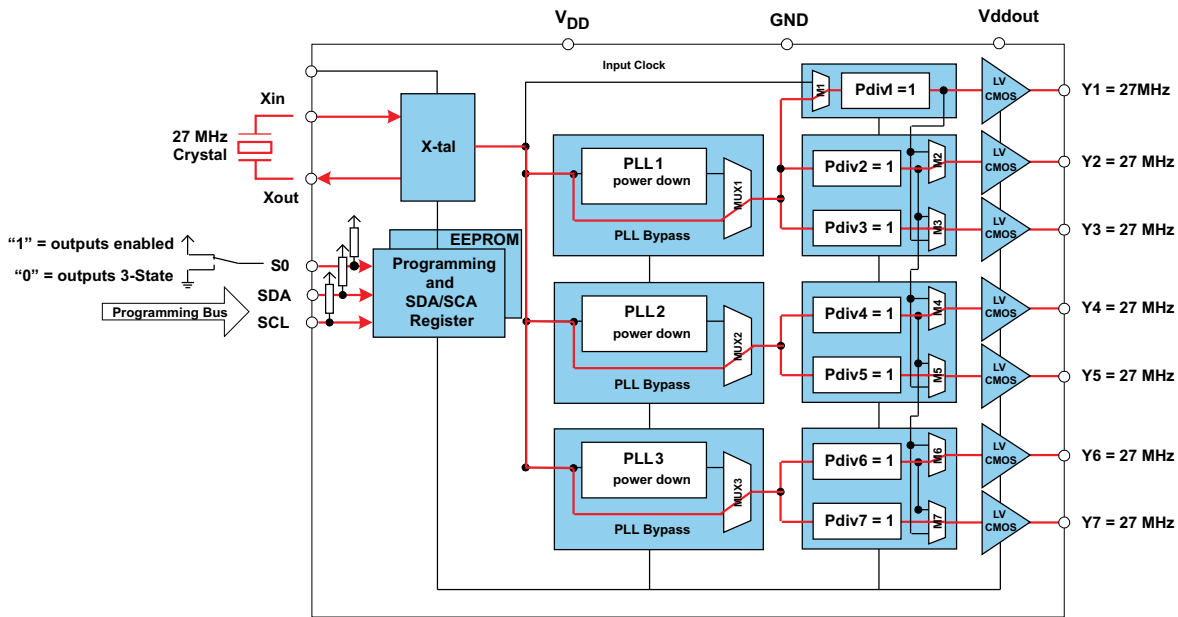

Figure 6. Default Device Setting

Table 4 shows the factory default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 configured as programming pins in default mode.

Table 4. Factory Default Setting for Control Terminal Register⁽¹⁾

| EXTERNAL CONTROL PINS | | | Y1 | PLL1 SETTINGS | | | PLL2 SETTINGS | | | PLL3 SETTINGS | | |
|-----------------------|-----------|----|------------------|---------------------|---------------|------------------|---------------------|---------------|------------------|---------------------|---------------|------------------|
| | | | OUTPUT SELECTION | FREQUENCY SELECTION | SSC SELECTION | OUTPUT SELECTION | FREQUENCY SELECTION | SSC SELECTION | OUTPUT SELECTION | FREQUENCY SELECTION | SSC SELECTION | OUTPUT SELECTION |
| S2 | S1 | S0 | Y1 | FS1 | SSC1 | Y2Y3 | FS2 | SSC2 | Y4Y5 | FS3 | SSC3 | Y6Y7 |
| SCL (I2C) | SDA (I2C) | 0 | 3-state | $f_{VCO1,0}$ | off | 3-state | $f_{VCO2,0}$ | off | 3-state | $f_{VCO1,0}$ | off | 3-state |
| SCL (I2C) | SDA (I2C) | 1 | enabled | $f_{VCO1,0}$ | off | enabled | $f_{VCO2,0}$ | off | enabled | $f_{VCO1,0}$ | off | enabled |

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA/SCL. They do not have any control-pin function but they are internally interpreted as if S1=0 and S2=0. However, S0 is a control-pin which in the default mode switches all outputs ON or OFF (as previously predefined).

8.3.3 SDA/SCL Serial Interface

The CDCE937 operates as a slave device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I²C specification. It operates in the standard-mode transfer (up to 100 kbit/s) and fast-mode transfer (up to 400kbit/s) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDC9xx are dual function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be reprogrammed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].

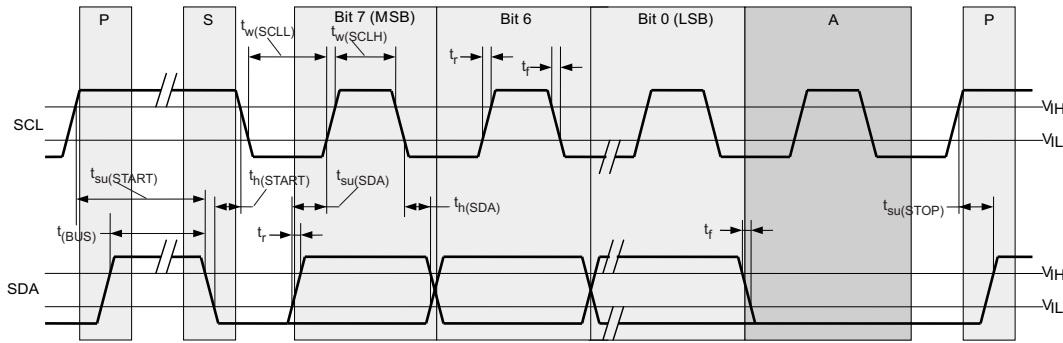


Figure 7. Timing Diagram for SDA/SCL Serial Control Interface

8.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of Bytes read-out are defined by Byte Count in the Generic Configuration Register. At Block Read instruction all bytes defined in the Byte Count has to be readout to correctly finish the read cycle.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte independent of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA register contents are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read during the programming sequence (Byte Read or Block Read). The programming status can be monitored by reading *EEPIP*, Byte 01–Bit [6].

The offset of the indexed byte is encoded in the command code, as described in [Table 5](#).

Table 5. Slave Receiver Address (7 Bits)

| DEVICE | A6 | A5 | A4 | A3 | A2 | A1 ⁽¹⁾ | A0 ⁽¹⁾ | R/W |
|----------|----|----|----|----|----|-------------------|-------------------|-----|
| CDCEx913 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1/0 |
| CDCEx925 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 |
| CDCEx937 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1/0 |
| CDCEx949 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1/0 |

(1) Address bits A0 and A1 are programmable through the SDA/SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

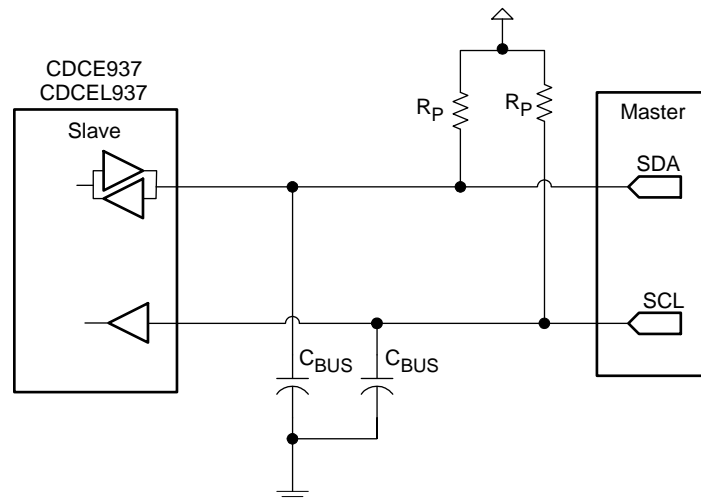
8.4 Device Functional Modes

8.4.1 SDA/SCL Hardware Interface

[Figure 8](#) shows how the CDCEx937 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed may require reduction (400 kHz is the maximum) if many devices are connected.

Note that the pullup resistors (R_P) depends on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 k Ω . It must meet the minimum sink current of 3 mA at $V_{OLmax} = 0.4$ V for the output stages (for more details, see [SMBus](#) or [I²C Bus](#) specification).

Device Functional Modes (continued)



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Figure 8. SDA/SCL Hardware Interface

8.5 Programming

Table 6. Command Code Definition

| BIT | DESCRIPTION |
|-------|----------------------------------------------------------------------------------|
| 7 | 0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation |
| (6:0) | Byte Offset for Byte Read, Block Read, Byte Write and Block Write operation. |

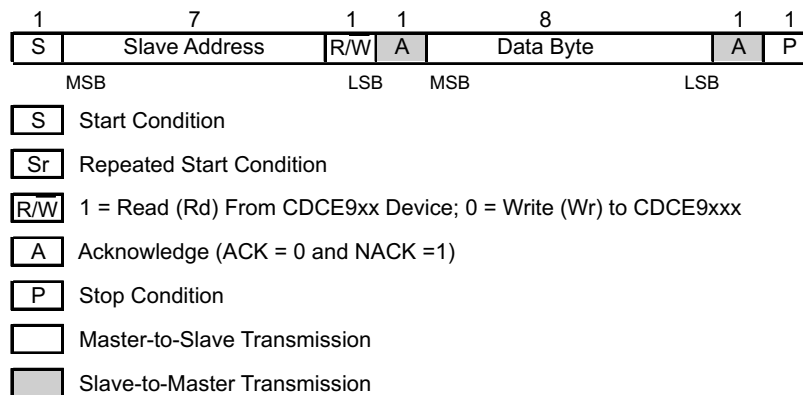


Figure 9. Generic Programming Sequence



Figure 10. Byte Write Protocol

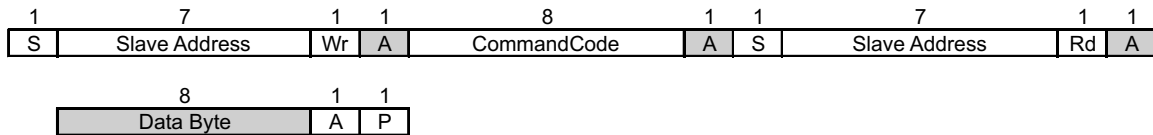
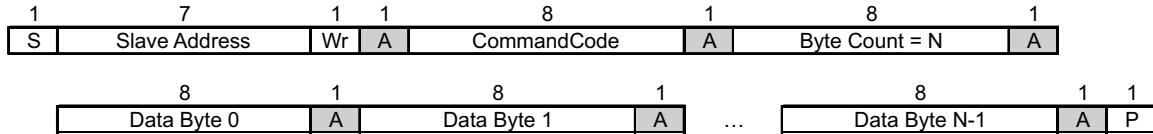


Figure 11. Byte Read Protocol



Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and must not be overwritten.

Figure 12. Block Write Protocol

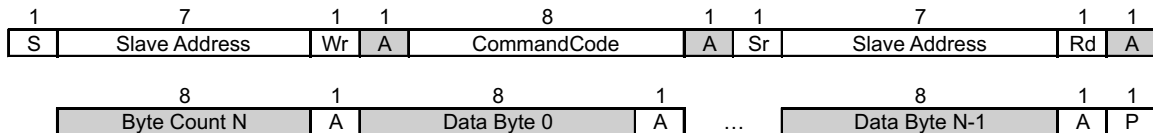


Figure 13. Block Read Protocol

8.6 Register Maps

8.6.1 SDA/SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCEx937. All settings can be manually written into the device through the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock™ software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA and SCL Registers

| ADDRESS OFFSET | REGISTER DESCRIPTION | TABLE |
|----------------|--------------------------------|--------------------------|
| 00h | Generic Configuration Register | Table 9 |
| 10h | PLL1 Configuration Register | Table 10 |
| 20h | PLL2 Configuration Register | Table 11 |
| 30h | PLL3 Configuration Register | Table 12 |

The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2 (see [Control Terminal Setting](#)).

Table 8. Configuration Register, External Control Terminals

| | EXTERNAL CONTROL PINS | | | Y1 | PLL1 SETTINGS | | | PLL2 SETTINGS | | | PLL3 SETTINGS | | |
|-------------------------------|-----------------------|-----|------|------------------|-----------------|---------------|------------------|-----------------|---------------|------------------|-----------------|---------------|------------------|
| | S2 | S1 | S0 | OUTPUT SELECTION | FREQ. SELECTION | SSC SELECTION | OUTPUT SELECTION | FREQ. SELECTION | SSC SELECTION | OUTPUT SELECTION | FREQ. SELECTION | SSC SELECTION | OUTPUT SELECTION |
| | Y1 | FS1 | SSC1 | Y2Y3 | FS2 | SSC2 | Y4Y5 | FS3 | SSC3 | Y6Y7 | | | |
| 0 | 0 | 0 | 0 | Y1_0 | FS1_0 | SSC1_0 | Y2Y3_0 | FS2_0 | SSC2_0 | Y4Y5_0 | FS3_0 | SSC3_0 | Y6Y7_0 |
| 1 | 0 | 0 | 1 | Y1_1 | FS1_1 | SSC1_1 | Y2Y3_1 | FS2_1 | SSC2_1 | Y4Y5_1 | FS3_1 | SSC3_1 | Y6Y7_1 |
| 2 | 0 | 1 | 0 | Y1_2 | FS1_2 | SSC1_2 | Y2Y3_2 | FS2_2 | SSC2_2 | Y4Y5_2 | FS3_2 | SSC3_2 | Y6Y7_2 |
| 3 | 0 | 1 | 1 | Y1_3 | FS1_3 | SSC1_3 | Y2Y3_3 | FS2_3 | SSC2_3 | Y4Y5_3 | FS3_3 | SSC3_3 | Y6Y7_3 |
| 4 | 1 | 0 | 0 | Y1_4 | FS1_4 | SSC1_4 | Y2Y3_4 | FS2_4 | SSC2_4 | Y4Y5_4 | FS3_4 | SSC3_4 | Y6Y7_4 |
| 5 | 1 | 0 | 1 | Y1_5 | FS1_5 | SSC1_5 | Y2Y3_5 | FS2_5 | SSC2_5 | Y4Y5_5 | FS3_5 | SSC3_5 | Y6Y7_5 |
| 6 | 1 | 1 | 0 | Y1_6 | FS1_6 | SSC1_6 | Y2Y3_6 | FS2_6 | SSC2_6 | Y4Y5_6 | FS3_6 | SSC3_6 | Y6Y7_6 |
| 7 | 1 | 1 | 1 | Y1_7 | FS1_7 | SSC1_7 | Y2Y3_7 | FS2_7 | SSC2_7 | Y4Y5_7 | FS3_7 | SSC3_7 | Y6Y7_7 |
| Address Offset ⁽¹⁾ | | | | 04h | 13h | 10h–12h | 15h | 23h | 20h–22h | 25h | 33h | 30h–32h | 35h |

(1) Address Offset refers to the byte address in the Configuration Register in the following pages.

Table 9. Generic Configuration Register

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|-------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00h | 7 | E_EL | Xb | Device identification (read-only): 1 is CDCE937 (3.3 V), 0 is CDCEL937 (1.8 V) |
| | 6:4 | RID | Xb | Revision Identification Number (read only) |
| | 3:0 | VID | 1h | Vendor Identification Number (read only) |
| 01h | 7 | – | 0b | Reserved – always write 0 |
| | 6 | EEPIP | 0b | EEPROM Programming Status: ⁽⁴⁾ (read only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode |
| | 5 | EELock | 0b | Permanently Lock EEPROM Data ⁽⁵⁾ 0 – EEPROM is not locked 1 – EEPROM is permanently locked |
| | 4 | PWDN | 0b | Device Power Down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (PLL1 and all outputs are enabled) 1 – device power down (PLL1 in power down and all outputs in 3-state) |
| | 3:2 | INCLK | 00b | Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 11 – reserved |
| | 1:0 | SLAVE_ADDR | 01b | Programmable Address Bits A0 and A1 of the Slave Receiver Address |
| 02h | 7 | M1 | 1b | Clock source selection for output Y1: 0 – input clock 1 – PLL1 clock |
| | 6 | SPICON | 0b | Operation mode selection for pin 18/19 ⁽⁶⁾ 0 – serial programming interface SDA (pin 19) and SCL (pin 18) 1 – control pins S1 (pin 19) and S2 (pin 18) |
| | 5:4 | Y1_ST1 | 11b | Y1-State0/1 Definition |
| | 3:2 | Y1_ST0 | 01b | 00 – device power down (all PLLs in power down and all outputs in 3-State) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled |
| | 1:0 | Pdiv1 [9:8] | 001h | 10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value |
| 03h | 7:0 | Pdiv1 [7:0] | | |

- (1) Writing data beyond '40h' may affect device function.
- (2) All data transferred with the MSB first.
- (3) Unless customer-specific setting.
- (4) During EEPROM programming, no data is allowed to be sent to the device through the SDA/SCL bus until the programming sequence is completed. However, data can be read out during the programming sequence (Byte Read or Block Read).
- (5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. There is no further programming possible. However, data can still be written through the SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELock is effective only, if written into the EEPROM!
- (6) Selection of control pins is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0 = 0 and A1 = 0.

Table 9. Generic Configuration Register (continued)

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|---------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 04h | 7 | Y1_7 | 0b | Y1_ST0/Y1_ST1 State Selection ⁽⁷⁾ 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1) |
| | 6 | Y1_6 | 0b | |
| | 5 | Y1_5 | 0b | |
| | 4 | Y1_4 | 0b | |
| | 3 | Y1_3 | 0b | |
| | 2 | Y1_2 | 0b | |
| | 1 | Y1_1 | 1b | |
| | 0 | Y1_0 | 0b | |
| 05h | 7:3 | XCSEL | 0Ah | Crystal Load Capacitor Selection ⁽⁸⁾ 00h → 0 pF 01h → 1 pF 02h → 2 pF : 14h-to-1Fh → 20 pF |
| | 2:0 | | 0b | Reserved – do not write other than 0 |
| 06h | 7:1 | BCOUNT | 40h | 7-Bit Byte Count (defines the number of bytes which is sent from this device at the next Block Read transfer); all bytes have to be read out to correctly finish the read cycle.) |
| | 0 | EEWRITE | 0b | Initiate EEPROM Write Cycle ⁽⁴⁾ ⁽⁹⁾ 0 – no EEPROM write cycle 1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM) |
| 07h-0Fh | | — | 0h | Unused address range |

- (7) These are the bits of the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
- (8) The internal load capacitor (C1, C2) has to be used to achieve the best clock performance. External capacitors must be used only to finely adjust C_L by a few pF's. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For C_L > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF//2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see [VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085).
- (9) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE bit has to be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 10. PLL1 Configuration Register

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 10h | 7:5 | SSC1_7 [2:0] | 000b | SSC1: PLL1 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td>Down</td> <td>Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC1_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC1_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 11h | 7 | SSC1_5 [0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC1_4 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 3:1 | SSC1_3 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 0 | SSC1_2 [2] | | | | | | | | | | | | | | | | | | | | |
| 12h | 7:6 | SSC1_2 [1:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 5:3 | SSC1_1 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 2:0 | SSC1_0 [2:0] | | | | | | | | | | | | | | | | | | | | |
| 13h | 7 | FS1_7 | 0b | FS1_x: PLL1 Frequency Selection ⁽⁴⁾ 0 – f _{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f _{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS1_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS1_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS1_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS1_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | FS1_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | FS1_1 | 0b | | | | | | | | | | | | | | | | | | | |
| 0 | FS1_0 | 0b | | | | | | | | | | | | | | | | | | | | |

- (1) Writing data beyond 40h may adversely affect device function.
- (2) All data is transferred MSB-first.
- (3) Unless a custom setting is used
- (4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION | |
|-----------------------|--------------------|----------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 14h | 7 | MUX1 | 1b | PLL1 Multiplexer: 0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down) | |
| | 6 | M2 | 1b | Output Y2 Multiplexer: 0 – Pdiv1 1 – Pdiv2 | |
| | 5:4 | M3 | 10b | Output Y3 Multiplexer: 00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved | |
| | 3:2 | Y2Y3_ST1 | 11b | Y2, Y3- State0/1definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State 10 – Y2/Y3 disabled to low 11 – Y2/Y3 enabled | |
| | 1:0 | Y2Y3_ST0 | 01b | | |
| 15h | 7 | Y2Y3_7 | 0b | Y2Y3_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1) | |
| | 6 | Y2Y3_6 | 0b | | |
| | 5 | Y2Y3_5 | 0b | | |
| | 4 | Y2Y3_4 | 0b | | |
| | 3 | Y2Y3_3 | 0b | | |
| | 2 | Y2Y3_2 | 0b | | |
| | 1 | Y2Y3_1 | 1b | | |
| | 0 | Y2Y3_0 | 0b | | |
| 16h | 7 | SSC1DC | 0b | PLL1 SSC down/center selection: 0 – down 1 – center | |
| | 6:0 | Pdiv2 | 01h | 7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by 1-to-127 is divider value | |
| 17h | 7 | — | 0b | Reserved – do not write others than 0 | |
| | 6:0 | Pdiv3 | 01h | 7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by 1-to-127 is divider value | |
| 18h | 7:0 | PLL1_0N [11:4] | 004h | PLL1_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information, see PLL Frequency Planning). | |
| 19h | 7:4 | PLL1_0N [3:0] | | | |
| | 3:0 | PLL1_0R [8:5] | | | |
| 1Ah | 7:3 | PLL1_0R[4:0] | | | 000h |
| | 2:0 | PLL1_0Q [5:3] | | | 10h |
| 1Bh | 7:5 | PLL1_0Q [2:0] | 010b | f_{VCO1_0} range selection: 00 – $f_{VCO1_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_0} < 175$ MHz 11 – $f_{VCO1_0} \geq 175$ MHz | |
| | 4:2 | PLL1_0P [2:0] | | | |
| 1Ch | 7:0 | PLL1_1N [11:4] | 004h | PLL1_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see PLL Frequency Planning). | |
| 1Dh | 7:4 | PLL1_1N [3:0] | | | |
| | 3:0 | PLL1_1R [8:5] | | | |
| 1Eh | 7:3 | PLL1_1R[4:0] | | | 000h |
| | 2:0 | PLL1_1Q [5:3] | | | 10h |
| 1Fh | 7:5 | PLL1_1Q [2:0] | 010b | f_{VCO1_1} range selection: 00 – $f_{VCO1_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_1} < 175$ MHz 11 – $f_{VCO1_1} \geq 175$ MHz | |
| | 4:2 | PLL1_1P [2:0] | | | |
| | 1:0 | VCO1_1_RANGE | 00b | | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

Table 11. PLL2 Configuration Register

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 20h | 7:5 | SSC2_7 [2:0] | 000b | SSC2: PLL2 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td>Down</td> <td>Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC2_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC2_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 21h | 7 | | SSC2_5 [0] | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC2_4 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 3:1 | SSC2_3 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 22h | 0 | SSC2_2 [2] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7:6 | SSC2_2 [1:0] | | | | | | | | | | | | | | | | | | | | |
| | 5:3 | SSC2_1 [2:0] | | 000b | | | | | | | | | | | | | | | | | | |
| 23h | 2:0 | SSC2_0 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7 | FS2_7 | 0b | FS2_x: PLL2 Frequency Selection ⁽⁴⁾ 0 – f _{VCO2_0} (predefined by PLL2_0 – Multiplier/Divider value) 1 – f _{VCO2_1} (predefined by PLL2_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS2_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS2_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS2_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS2_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | FS2_2 | 0b | | | | | | | | | | | | | | | | | | | |
| 1 | FS2_1 | 0b | | | | | | | | | | | | | | | | | | | | |
| 24h | 0 | FS2_0 | 0b | | | | | | | | | | | | | | | | | | | |
| | 7 | MUX2 | 1b | PLL2 Multiplexer: 0 – PLL2 1 – PLL2 Bypass (PLL2 is in power down) | | | | | | | | | | | | | | | | | | |
| | 6 | M4 | 1b | Output Y4 Multiplexer: 0 – Pdiv2 1 – Pdiv4 | | | | | | | | | | | | | | | | | | |
| | 5:4 | M5 | 10b | Output Y5 Multiplexer: 00 – Pdiv2-Divider 01 – Pdiv4-Divider 10 – Pdiv5-Divider 11 – reserved | | | | | | | | | | | | | | | | | | |
| | 3:2 | Y4Y5_ST1 | 11b | Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down) 01 – Y4/Y5 disabled to 3-State 10 – Y4/Y5 disabled to low 11 – Y4/Y5 enabled | | | | | | | | | | | | | | | | | | |
| 1:0 | Y4Y5_ST0 | 01b | | | | | | | | | | | | | | | | | | | | |
| 25h | 7 | Y4Y5_7 | 0b | Y4Y5_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1) | | | | | | | | | | | | | | | | | | |
| | 6 | Y4Y5_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | Y4Y5_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | Y4Y5_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | Y4Y5_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | Y4Y5_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | Y4Y5_1 | 1b | | | | | | | | | | | | | | | | | | | |
| | 0 | Y4Y5_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 26h | 7 | SSC2DC | 0b | PLL2 SSC down/center selection: 0 – down 1 – center | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv4 | 01h | 7-Bit Y4-Output-Divider Pdiv4: 0 – reset and stand-by value 1-to-127 – divider | | | | | | | | | | | | | | | | | | |
| 27h | 7 | — | 0b | Reserved – do not write others than 0 | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv5 | 01h | 7-Bit Y5-Output-Divider Pdiv5: 0 – reset and stand-by value 1-to-127 – divider | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 40h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 11. PLL2 Configuration Register (continued)

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|----------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28h | 7:0 | PLL2_ON [11:4] | 004h | PLL2_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see PLL Frequency Planning). |
| 29h | 7:4 | PLL2_ON [3:0] | 000h | |
| | 3:0 | PLL2_OR [8:5] | | |
| 2Ah | 7:3 | PLL2_OR[4:0] | 10h | |
| | 2:0 | PLL2_OQ [5:3] | | |
| 2Bh | 7:5 | PLL2_OQ [2:0] | 010b | |
| | 4:2 | PLL2_OP [2:0] | 00b | f_{VCO2_0} range selection: 00 – $f_{VCO2_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO2_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO2_0} < 175$ MHz 11 – $f_{VCO2_0} \geq 175$ MHz |
| | 1:0 | VCO2_0_RANGE | | |
| 2Ch | 7:0 | PLL2_1N [11:4] | 004h | PLL2_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO2_1} (for more information see PLL Frequency Planning). |
| 2Dh | 7:4 | PLL2_1N [3:0] | 000h | |
| | 3:0 | PLL2_1R [8:5] | | |
| 2Eh | 7:3 | PLL2_1R[4:0] | 10h | |
| | 2:0 | PLL2_1Q [5:3] | | |
| 2Fh | 7:5 | PLL2_1Q [2:0] | 010b | |
| | 4:2 | PLL2_1P [2:0] | 00b | f_{VCO2_1} range selection: 00 – $f_{VCO2_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO2_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO2_1} < 175$ MHz 11 – $f_{VCO2_1} \geq 175$ MHz |
| | 1:0 | VCO2_1_RANGE | | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

Table 12. PLL3 Configuration Register

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 30h | 7:5 | SSC3_7 [2:0] | 000b | SSC3: PLL3 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td>Down</td> <td>Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC3_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC3_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 31h | 7 | SSC3_5 [0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC3_4 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 3:1 | SSC3_3 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 0 | SSC3_2 [2] | | | | | | | | | | | | | | | | | | | | |
| 32h | 7:6 | SSC3_2 [1:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 5:3 | SSC3_1 [2:0] | | | | | | | | | | | | | | | | | | | | |
| | 2:0 | SSC3_0 [2:0] | | | | | | | | | | | | | | | | | | | | |
| 33h | 7 | FS3_7 | 0b | FS3_x: PLL3 Frequency Selection ⁽⁴⁾ 0 – f_{VCO3_0} (predefined by PLL3_0 – Multiplier/Divider value) 1 – f_{VCO3_1} (predefined by PLL3_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS3_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS3_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS3_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS3_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | FS3_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | FS3_1 | 0b | | | | | | | | | | | | | | | | | | | |
| | 0 | FS3_0 | 0b | | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 40h may affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) These are the bits of the Control Terminal Register. The user can pre-define up to eight different control settings. At normal device operation, these setting can be selected by the external control pins, S0, S1, and S2.

Table 12. PLL3 Configuration Register (continued)

| OFFSET ⁽¹⁾ | BIT ⁽²⁾ | ACRONYM | DEFAULT ⁽³⁾ | DESCRIPTION | |
|-----------------------|--------------------|----------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 34h | 7 | MUX3 | 1b | PLL3 Multiplexer: 0 – PLL3 1 – PLL3 Bypass (PLL3 is in power down) | |
| | 6 | M6 | 1b | Output Y6 Multiplexer: 0 – Pdiv4 1 – Pdiv6 | |
| | 5:4 | M7 | 10b | Output Y7 Multiplexer: 00 – Pdiv4-Divider 01 – Pdiv6-Divider 10 – Pdiv7-Divider 11 – reserved | |
| | 3:2 | Y6Y7_ST1 | 11b | Y6, Y7- State0/1definition: 00 – Y6/Y7 disabled to 3-State and PLL3 power down 01 – Y6/Y7 disabled to 3-State 10 – Y6/Y7 disabled to low 11 – Y6/Y7 enabled | |
| 1:0 | Y6Y7_ST0 | 01b | | | |
| 35h | 7 | Y6Y7_7 | 0b | Y6Y7_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y6Y7_ST0) 1 – state1 (predefined by Y6Y7_ST1) | |
| | 6 | Y6Y7_6 | 0b | | |
| | 5 | Y6Y7_5 | 0b | | |
| | 4 | Y6Y7_4 | 0b | | |
| | 3 | Y6Y7_3 | 0b | | |
| | 2 | Y6Y7_2 | 0b | | |
| | 1 | Y6Y7_1 | 1b | | |
| | 0 | Y6Y7_0 | 0b | | |
| 36h | 7 | SSC3DC | 0b | PLL3 SSC down/center selection: 0 – down 1 – center | |
| | 6:0 | Pdiv6 | 01h | 7-Bit Y6-Output-Divider Pdiv6: 0 – reset and stand-by 1-to-127 – divider value | |
| 37h | 7 | — | 0b | Reserved – do not write others than 0 | |
| | 6:0 | Pdiv7 | 01h | 7-Bit Y7-Output-Divider Pdiv7: 0 – reset and stand-by 1-to-127 – divider value | |
| 38h | 7:0 | PLL3_0N [11:4] | 004h | PLL3_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO3_0} (for more information, see PLL Frequency Planning). | |
| 39h | 7:4 | PLL3_0N [3:0] | | | |
| | 3:0 | PLL3_0R [8:5] | 000h | | |
| 3Ah | 7:3 | PLL3_0R[4:0] | 10h | | |
| | 2:0 | PLL3_0Q [5:3] | | | |
| 3Bh | 7:5 | PLL3_0Q [2:0] | 010b | | |
| | 4:2 | PLL3_0P [2:0] | | | |
| | 1:0 | VCO3_0_RANGE | 00b | | f_{VCO3_0} range selection: 00 – $f_{VCO3_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO3_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO3_0} < 175$ MHz 11 – $f_{VCO3_0} \geq 175$ MHz |
| 3Ch | 7:0 | PLL3_1N [11:4] | 004h | | PLL3_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO3_1} (for more information, see PLL Frequency Planning). |
| 3Dh | 7:4 | PLL3_1N [3:0] | | | |
| | 3:0 | PLL3_1R [8:5] | 000h | | |
| 3Eh | 7:3 | PLL3_1R[4:0] | 10h | | |
| | 2:0 | PLL3_1Q [5:3] | | | |
| 3Fh | 7:5 | PLL3_1Q [2:0] | 010b | | |
| | 4:2 | PLL3_1P [2:0] | | | |
| | 1:0 | VCO3_1_RANGE | 00b | f_{VCO3_1} range selection: 00 – $f_{VCO3_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO3_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO3_1} < 175$ MHz 11 – $f_{VCO3_1} \geq 175$ MHz | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCE937 device is an easy-to-use, high-performance, programmable CMOS clock synthesizer. It can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCE937 features an on-chip loop filter and spread-spectrum modulation. Programming can be done through SPI, pin-mode, or using on-chip EEPROM. The following section shows some examples of using CDCE937 in various applications.

9.2 Typical Application

Figure 14 shows the use of the CDCE937 devices for replacement of crystals and crystal oscillators on a Gigabit Ethernet Switch application.

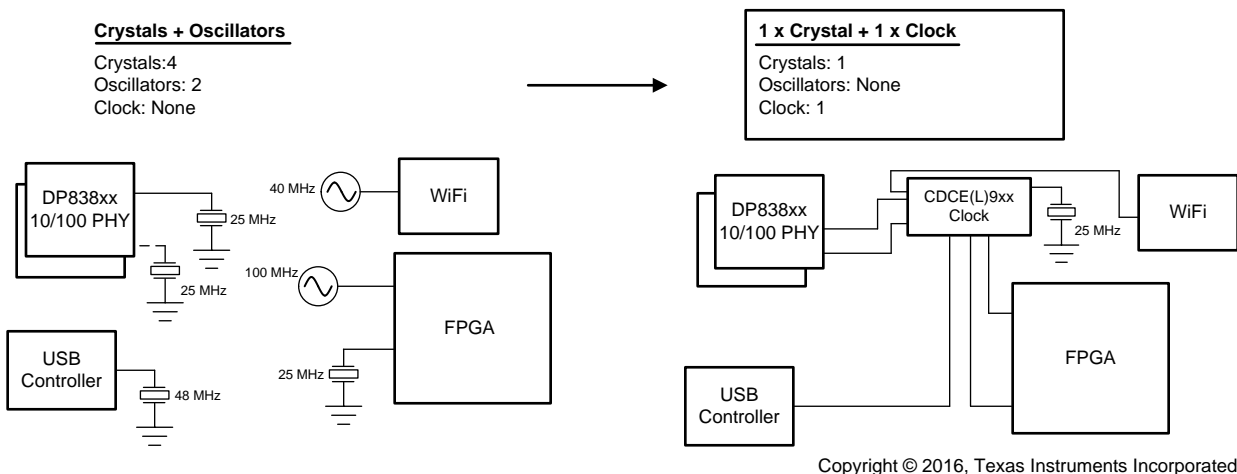


Figure 14. Crystal and Oscillator Replacement Example

9.2.1 Design Requirements

CDCE937 supports spread-spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Modulation shape (triangular)
- Center spread / down spread (\pm or $-$)

Typical Application (continued)

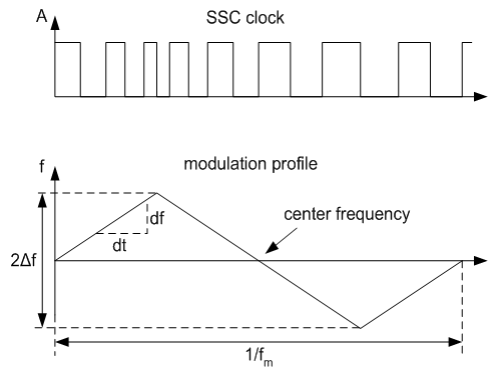
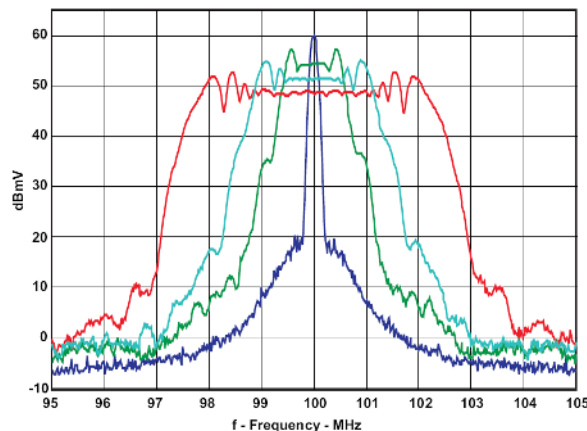


Figure 15. Modulation Frequency (fm) and Modulation Amount

9.2.2 Detailed Design Procedure

9.2.2.1 Spread Spectrum Clock (SSC)

Spread-spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce Electromagnetic Interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, Fout = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

Figure 16. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

9.2.2.2 PLL Frequency Planning

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCEx913 are calculated with [Equation 1](#).

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M}$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
 - Pdiv (1 to 127) is the output divider
- (1)

The target VCO frequency (f_{VCO}) of each PLL is calculated with [Equation 2](#).

$$f_{VCO} = f_{IN} \times \frac{N}{M}$$

(2)

The PLL internally operates as fractional divider and needs the following multiplier/divider settings:

Typical Application (continued)

- N
- $P = 4 - \text{int}(\log_2 N/M)$; if $P < 0$ then $P = 0$
- $Q = \text{int}(N'/M)$
- $R = N' - M \times Q$

where

$$N' = N \times 2^P$$

$$N \geq M;$$

$$80 \text{ MHz} \leq f_{VCO} \leq 230 \text{ MHz}$$

$$16 \leq Q \leq 63$$

$$0 \leq P \leq 4$$

$$0 \leq R \leq 15$$

Example:

for $f_{IN} = 27 \text{ MHz}$; $M = 1$; $N = 4$; $P_{div} = 2$

- $f_{OUT} = 54 \text{ MHz}$
- $f_{VCO} = 108 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 4) = 4 - 2 = 2$
- $N' = 4 \times 2^2 = 16$
- $Q = \text{int}(16) = 16$
- $R = 16 - 16 = 0$

for $f_{IN} = 27 \text{ MHz}$; $M = 2$; $N = 11$; $P_{div} = 2$

- $f_{OUT} = 74.25 \text{ MHz}$
- $f_{VCO} = 148.50 \text{ MHz}$
- $P = 4 - \text{int}(\log_2 5.5) = 4 - 2 = 2$
- $N' = 11 \times 2^2 = 44$
- $Q = \text{int}(22) = 22$
- $R = 44 - 44 = 0$

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

9.2.2.3 Crystal Oscillator Start-Up

When the CDCE937 is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. Figure 17 shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is in the order of approximately 250 μs compared to approximately 10 μs of lock time. In general, lock time will be an order of magnitude less compared to the crystal start-up time.

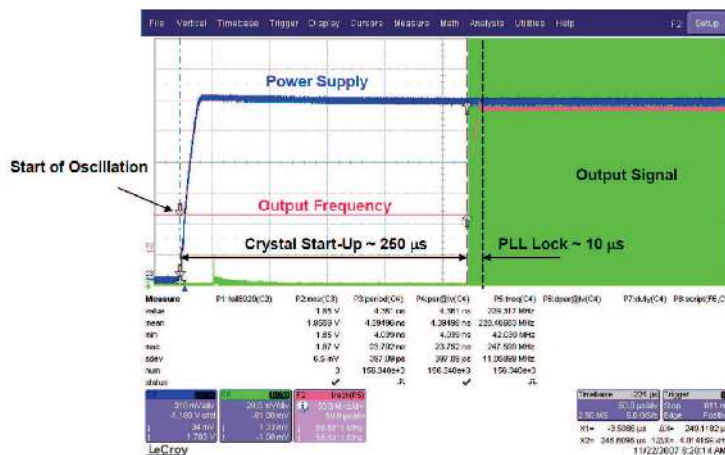
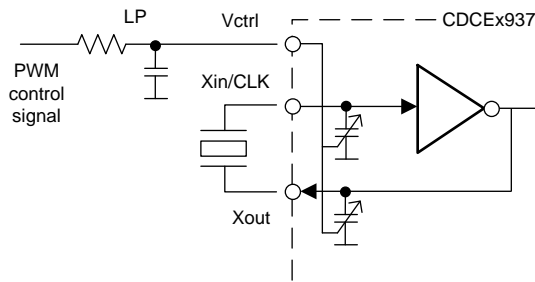


Figure 17. Crystal Oscillator Start-Up vs PLL Lock Time

9.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCE937 is adjusted for media and other applications with the VCXO control input Vctrl. If a PWM modulated signal is used as a control signal for the VCXO, an external filter is needed.

Typical Application (continued)



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Figure 18. Frequency Adjustment Using PWM Input to the VCXO Control

9.2.2.5 Unused Inputs and Outputs

If VCXO pulling functionality is not required, Vctrl should be left floating. All other unused inputs should be set to GND. Unused outputs should be left floating.

If one output block is not used, TI recommends disabling it. However, TI always recommends providing the supply for the second output block even if it is disabled.

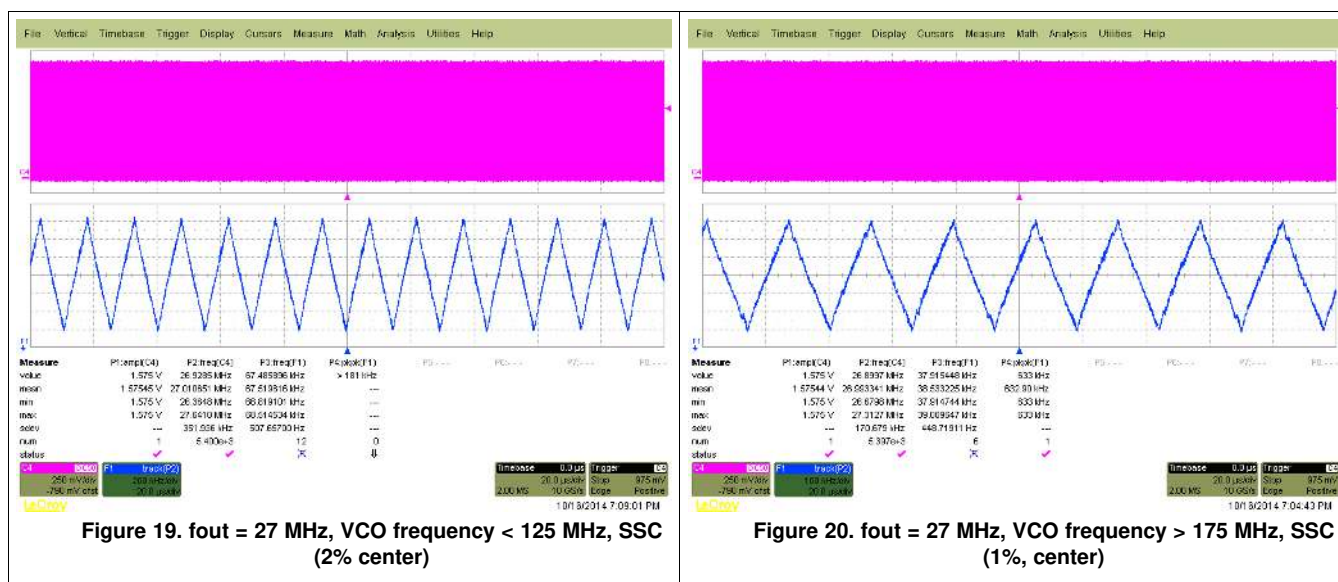
9.2.2.6 Switching Between XO and VCXO Mode

When the CDCE937 is in crystal oscillator or in VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

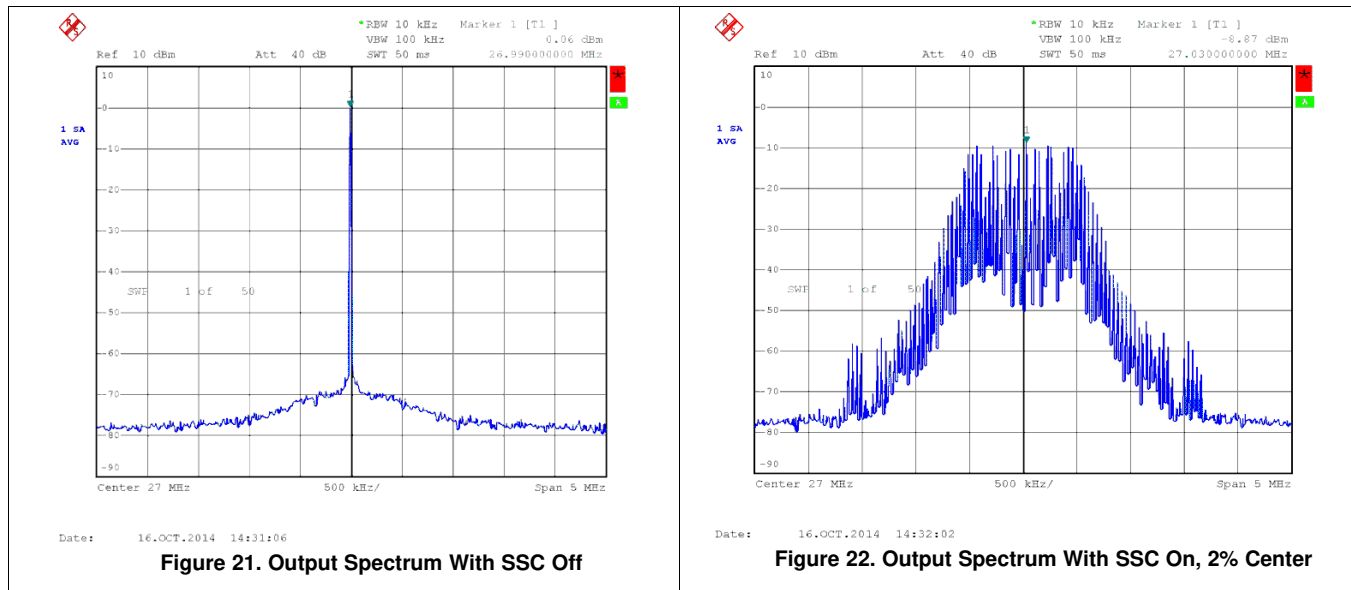
1. While in XO mode, put $Vctrl = Vdd / 2$
2. Switch from XO mode to VCXO mode
3. Program the internal capacitors in order to obtain 0 ppm at the output

9.2.3 Application Curves

Figure 19, Figure 20, Figure 21, and Figure 22 show CDCE937 measurements with the SSC feature enabled. Device configuration: 27-MHz input, 27-MHz output.



Typical Application (continued)



10 Power Supply Recommendations

There is no restriction on the power-up sequence. In case VDDOUT is applied first, TI recommends grounding VDD. In case VDDOUT is powered while VDD is floating, there is a risk of high current flowing on the VDDOUT.

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If there is a 3.3-V VDD available before the 1.8 V, the outputs remain disabled until the 1.8-V supply has reached a certain level.

11 Layout

11.1 Layout Guidelines

When the CDCE937 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, take care in placing the crystal units on the board. Crystals should be placed as close to the device as possible, ensuring that the routing lines from the crystal terminals to XIN and XOUT have the same length.

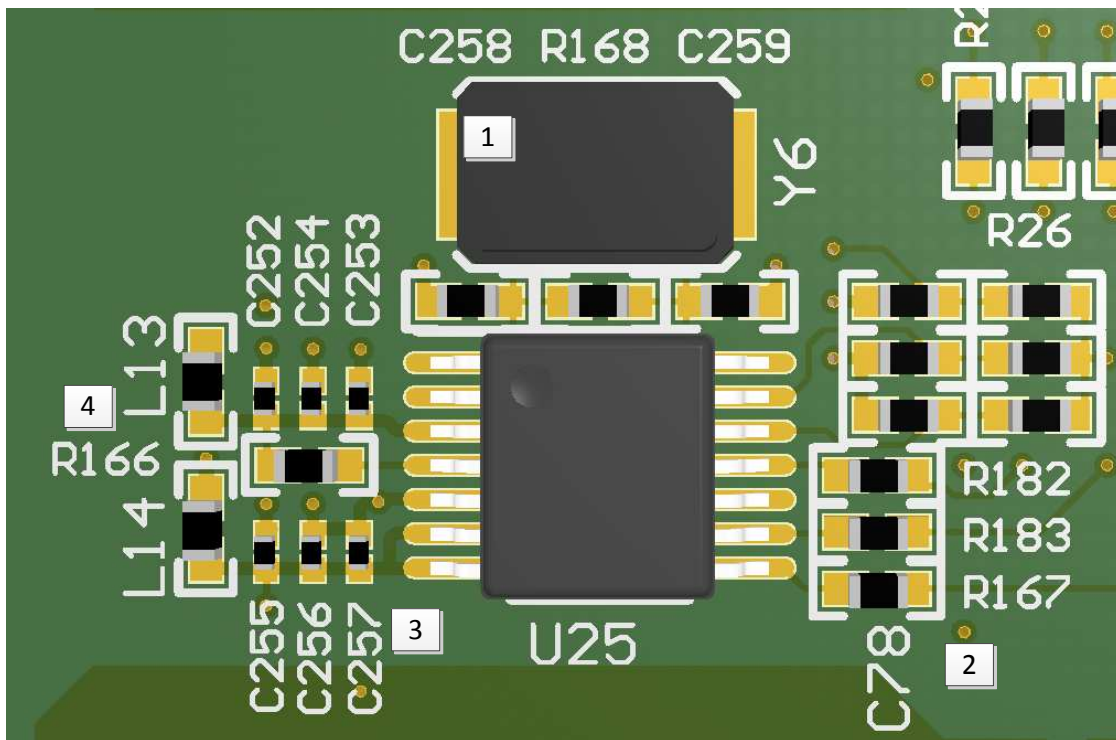
If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10 pF.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

[Figure 23](#) shows a conceptual layout detailing recommended placement of power supply bypass capacitors on the basis of CDCE937. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

11.2 Layout Example



- | | |
|------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
| <p>1 Place crystal with associated load caps as close to the chip</p> | <p>2 Place series termination resistors at Clock outputs to improve signal integrity</p> |
| <p>3 Place bypass caps close to the device pins, ensure wide freq. range</p> | <p>4 Use ferrite beads to isolate the device supply pins from board noise sources</p> |

Figure 23. Annotated Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

For development support see the following:

- [SMBus](#)
- [I²C Bus](#)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

[VCXO Application Guideline for CDCE\(L\)9xx Family](#) (SCAA085)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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Bluetooth is a trademark of Bluetooth SIG.

Ethernet is a trademark of Xerox Corporation.

All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCE937PW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCE937 | Samples |
| CDCE937PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCE937 | Samples |
| CDCE937PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCE937 | Samples |
| CDCE937PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCE937 | Samples |
| CDCEL937PW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCEL937 | Samples |
| CDCEL937PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDCEL937 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CDCE937, CDCEL937 :

- Automotive : [CDCE937-Q1](#), [CDCEL937-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

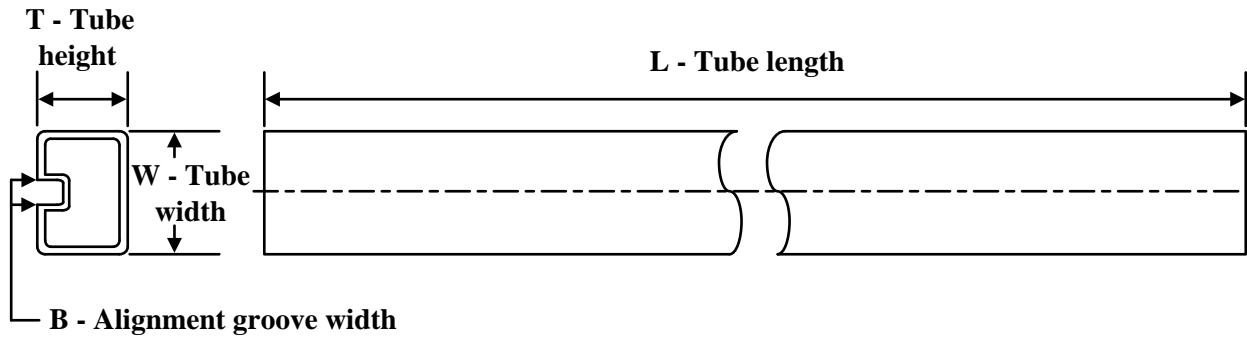

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCE937PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| CDCEL937PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

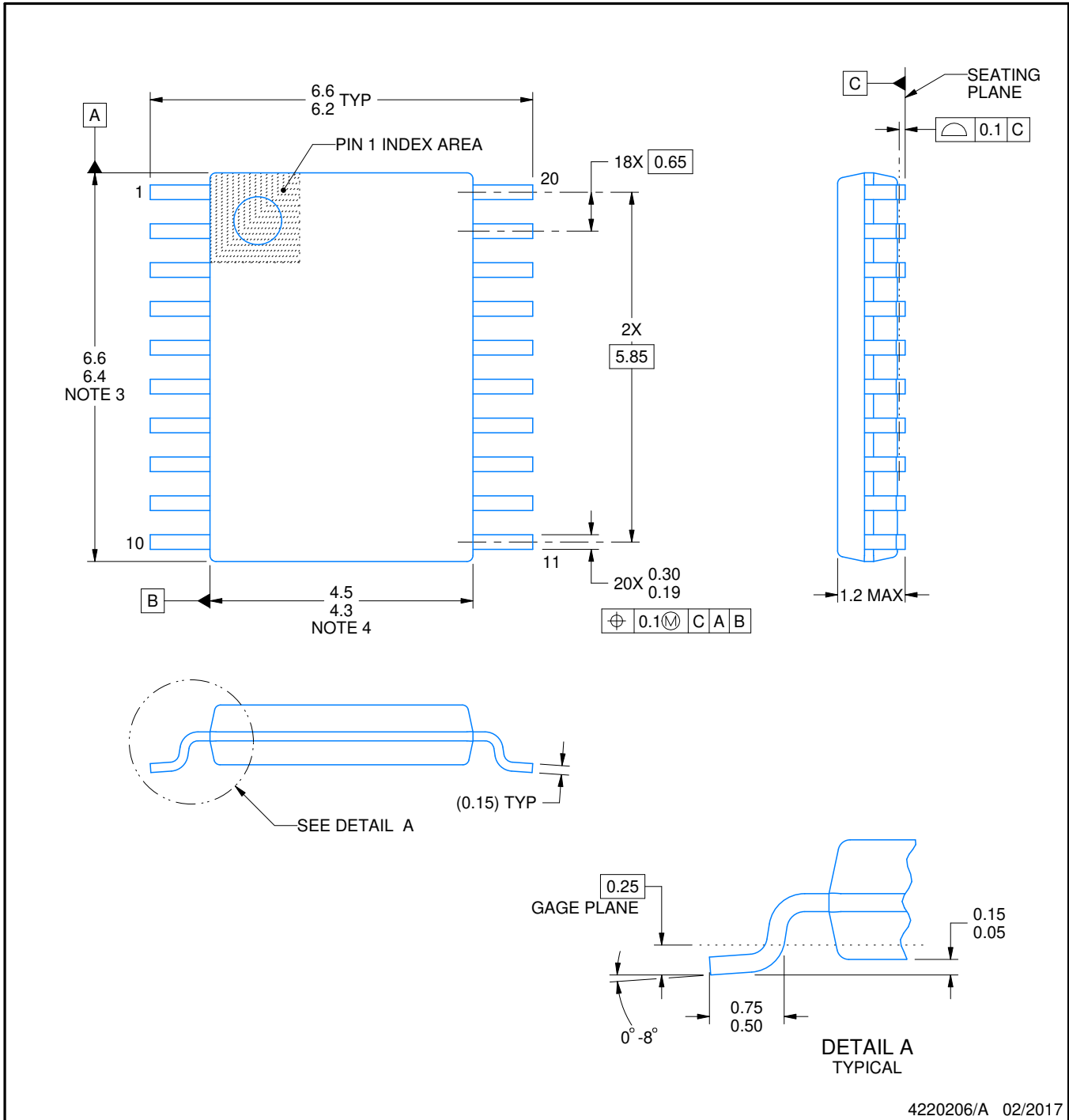
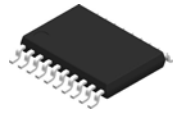

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCE937PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| CDCEL937PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CDCE937PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| CDCE937PWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| CDCEL937PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |



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NOTES:

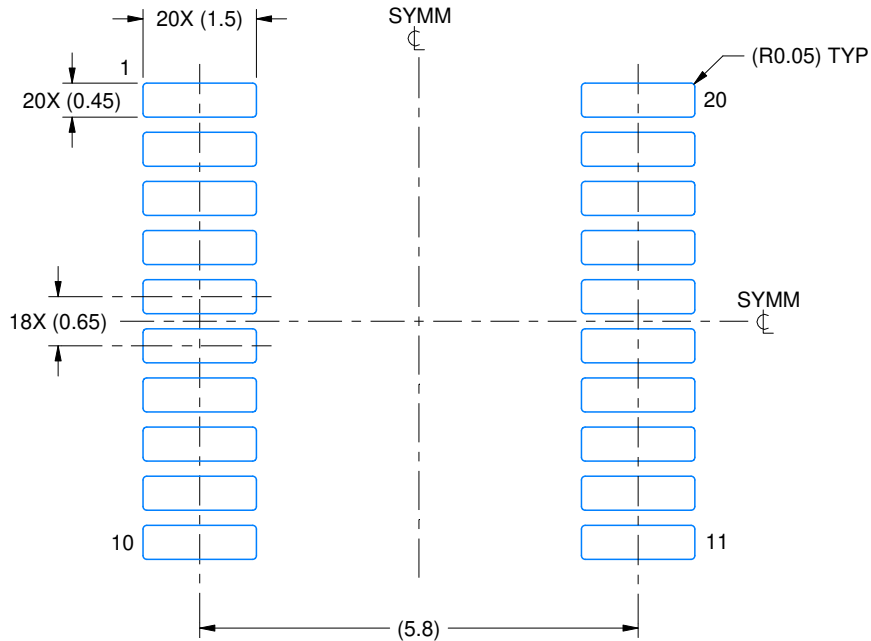
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

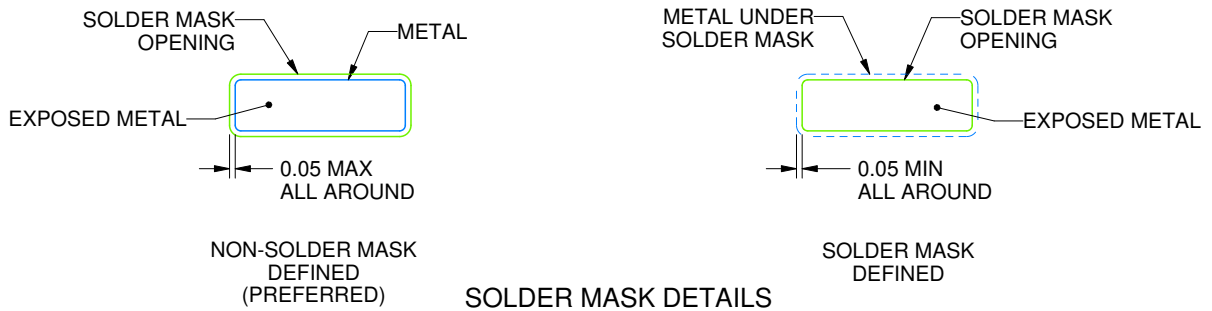
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

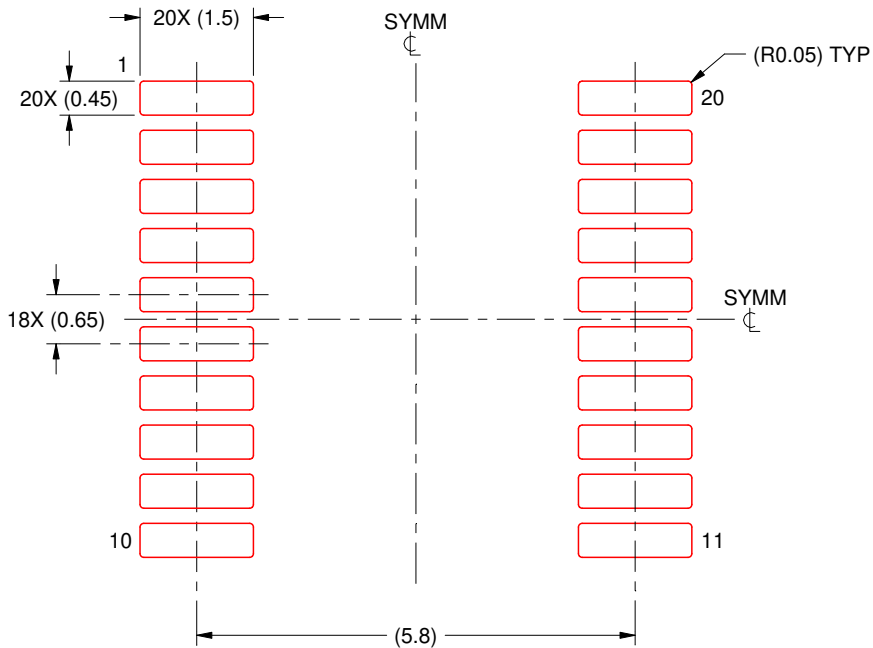
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

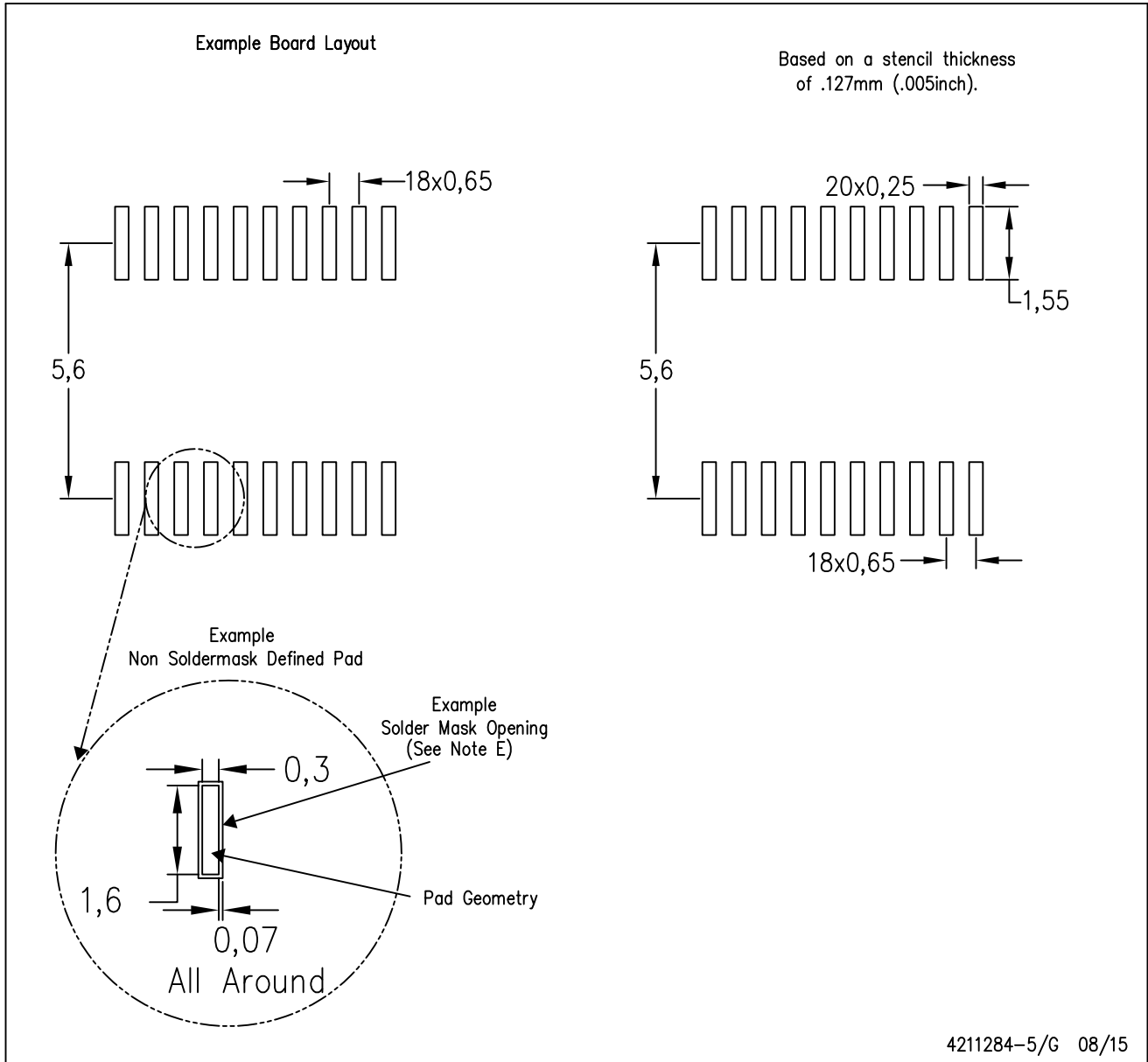
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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