User's Guide

TPS53353 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

The TPS53353EVM-744 evaluation module (EVM) demonstrates the TPS53353. The TPS53353 is a D-CAP™ mode, 20-A, synchronous buck converter with integrated MOSFETs. It provides a fixed 1.5-V output at up to 20 A from a 12-V input bus.

Table of Contents

Trademarks

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1 Description

The TPS53353EVM-744 is designed to use a regulated 12-V bus to produce a regulated 1.5-V output at up to 20 A of load current. The TPS53353EVM-744 is designed to demonstrate the TPS53353 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS53353.

1.1 Typical Application

- Server/storage
- Workstations and desktops
- Telecommunication infrastructure

1.2 Features

The TPS53353EVM-744 features:

- 20-Adc, steady-state output current
- Support prebias output voltage start-up
- J5 for selectable switching frequency setting
- J4 for selectable soft-start time
- J2 for enable function
- J6 for auto-skip and forced CCM selection
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1. TPS53353EVM-744 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range	V_{IN}	8	12	14	V
Maximum input current	V_{IN} = 8 V, I_O = 20 A		4.1		A
No-load input current	V_{IN} = 14 V, I_O = 0 A with auto-skip mode		1		mA
Output Characteristics					
Output voltage VOUT			1.5		V
Output voltage regulation	Line regulation (V_{IN} = 8 V – 14 V)		0.1		%
	Load regulation (V_{IN} = 12 V, I_O = 0 A – 20 A)		1		
Output voltage ripple	V_{IN} = 12 V, I_O = 20 A		20		mVpp
Output load current		0		20	A
Output overcurrent			26		A
Systems Characteristics					
Switching frequency			500		kHz
Peak efficiency	V_{IN} = 12 V, 1.5 V/10 A		91.87		%
Full-load efficiency	V_{IN} = 12 V, 1.5 V/20 A		91.38		%
Operating temperature			25		°C

Note

Jumpers are set at the factory to default locations; for details, see Section 5 of this user's guide.

3 Schematic

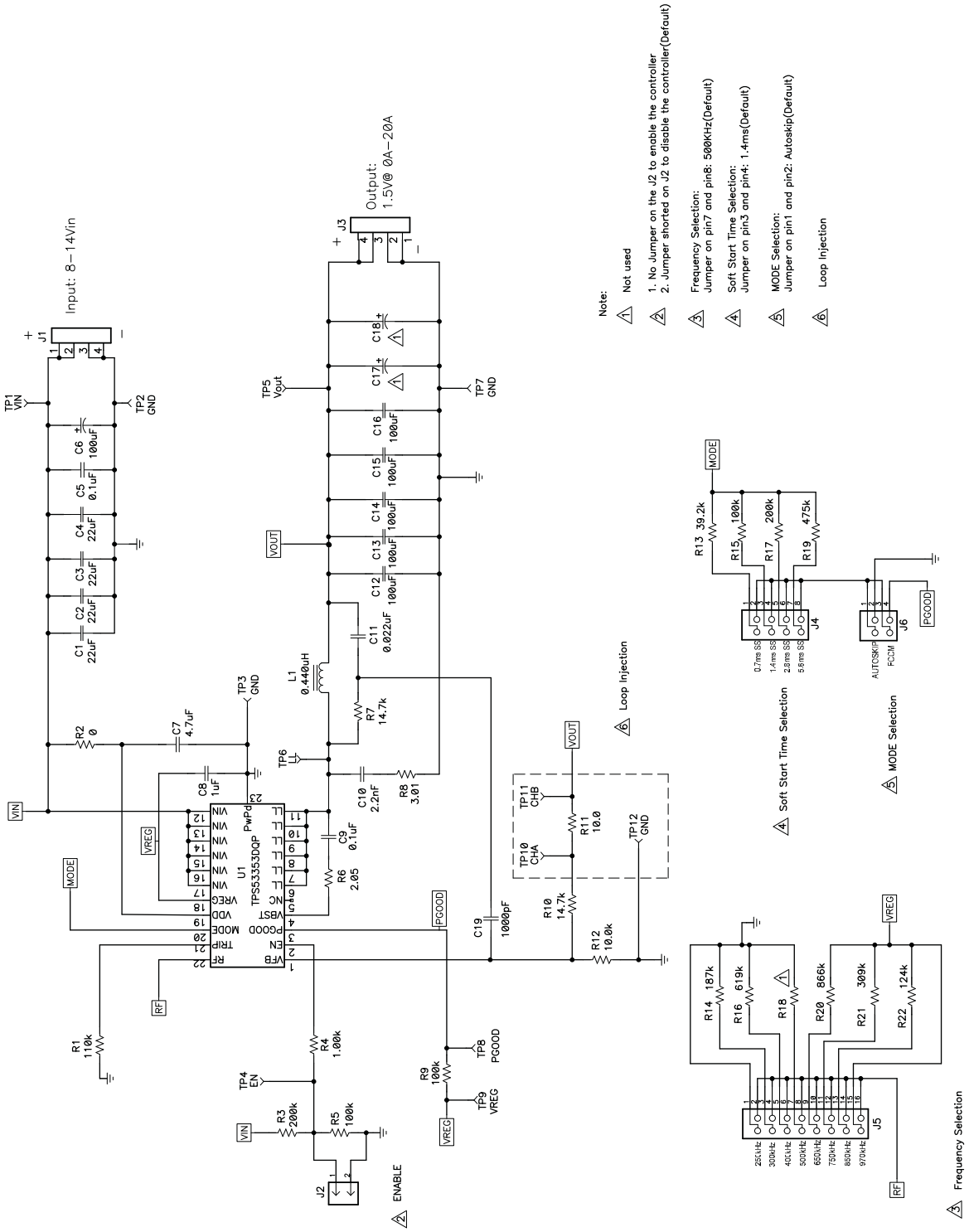

Figure 3-1. TPS53353EVM-744 Schematic

4 Test Setup

4.1 Test Equipment

Voltage Source: The input voltage source V_{IN} must be a 0-V to 14-V variable DC source capable of supplying 10 A_{DC}. Connect V_{IN} to J1 as shown in Figure 4-2.

Multimeters:

- V1: V_{IN} at TP1 (V_{IN}) and TP2 (GND)
- V2: VOUT at TP5 (VOUT) and TP7 (GND)
- A1: V_{IN} input current

Output Load: The output load should be an electronic constant resistance mode load capable of 0 A_{DC}–30 A_{DC} at 1.5 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 2-µs/division horizontal resolution
- 50-mV/division vertical resolution

Test points TP5 and TP7 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP5 and holding the ground barrel on TP7 as shown in Figure 4-1. Using a leaded ground connection may induce additional noise due to the large ground loop.

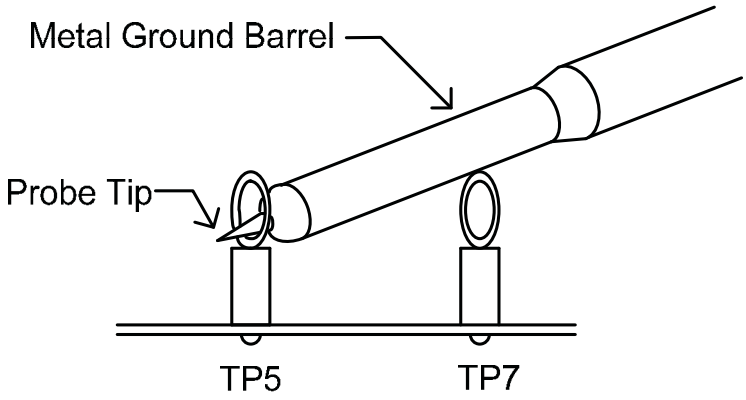

Figure 4-1. Tip and Barrel Measurement for V_{OUT} Ripple

Fan: Some of the components in this EVM can approach temperatures of 60°C during operation. A small fan capable of 200–400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed while the fan is not running.

Recommended Wire Gauge:

1. V_{IN} to J1 (12-V input):

   The recommended wire size is 1× AWG 14 per input connection, with the total length of wire less than four feet (2-foot input, 2-foot return).
2. J3 to LOAD:

   The minimum recommended wire size is 2× AWG 14, with the total length of wire less than four feet (2-foot input, 2-foot return).

4.2 Recommended Test Setup

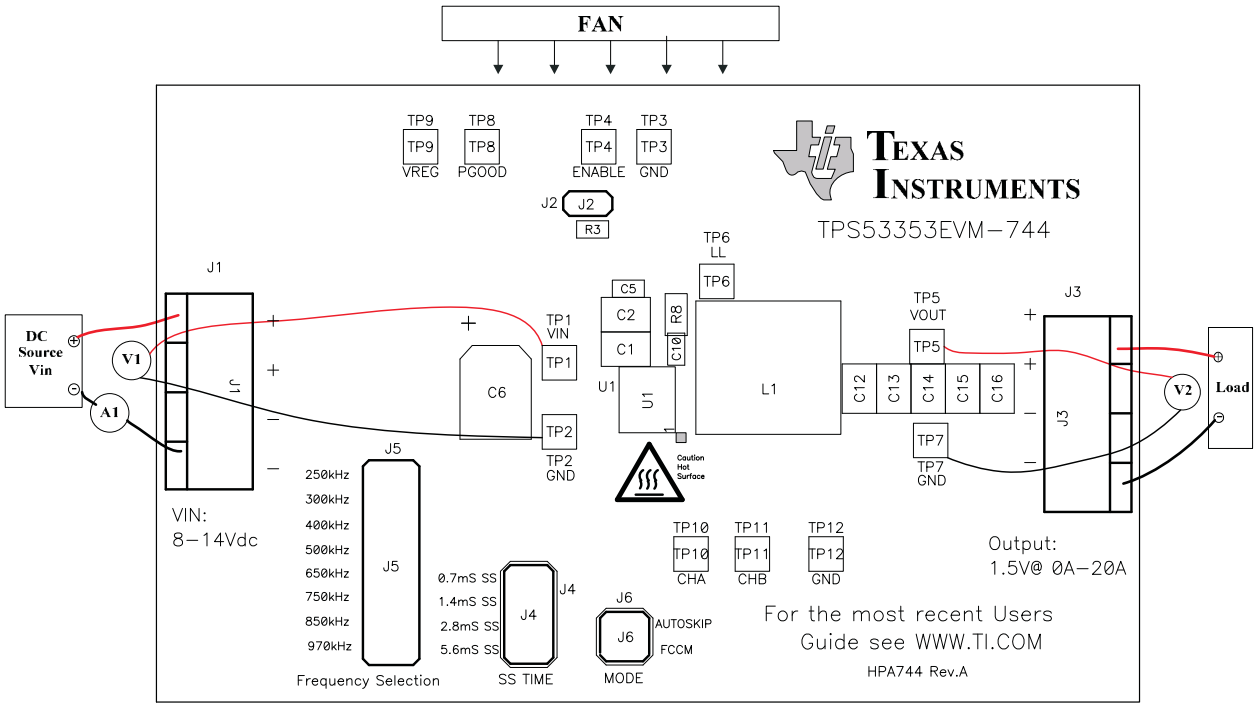

Figure 4-2. TPS53353EVM-744 Recommended Test Setup

Figure 4-2 is the recommended test setup to evaluate the TPS53353EVM-744. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM.

Input Connections:

1. Before connecting the DC input source V_{IN}, it is advisable to limit the source current from V_{IN} to 10-A maximum. Ensure that V_{IN} is initially set to 0 V and connected as shown in Figure 4-2.
2. Connect a voltmeter V1 at TP1 (V_{IN}) and TP2 (GND) to measure the input voltage.
3. Connect a current meter A1 to measure the input current.

Output Connections:

1. Connect the load to J3, and set the load to constant resistance mode to sink 0 A before V_{IN} is applied.
2. Connect a voltmeter V2 at TP5 (V_{OUT}) and TP7 (GND) to measure the output voltage.

Other Connections:

Place a fan as shown in Figure 4-2, and turn it on, ensuring that air is flowing across the EVM.

5 Configurations

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM per the following configurations.

5.1 Switching Frequency Selection

Use J5 to set the switching frequency.

Default setting: 500 kHz

Table 5-1. Switching Frequency Selection

JUMPER SET TO	RESISTOR (RF) CONNECTIONS (kΩ)	SWITCHING FREQUENCY (kHz)
Top (1–2 pin shorted)	0	250
Second (3–4 pin shorted)	187	300
Third (5–6 pin shorted)	619	400
Fourth (7–8 pin shorted)	**Open**	**500**
Fifth (9–10 pin shorted)	866	650
Sixth (11–12 pin shorted)	309	750
Seventh (13–14 pin shorted)	124	850
Bottom (15–16 pin shorted)	0	970

5.2 Soft-Start Selection

Use J4 to set the soft-start time.

Default setting: 1.4 ms

Table 5-2. Soft-Start Time Selection

JUMPER SET TO	R_{MODE} CONNECTIONS (kΩ)	SOFT-START TIME (ms)
Top (1–2 pin shorted)	39.2	0.7
Second (3–4 pin shorted)	**100**	**1.4**
Third (5–6 pin shorted)	200	2.8
Fourth (7–8 pin shorted)	475	5.6

5.3 Mode Selection

Use J6 to set the MODE pin.

Default setting: Auto Skip

Table 5-3. MODE Selection

JUMPER SET TO	R_{MODE} CONNECTIONS (Ω)
Top (1–2 pin shorted)	**Auto Skip**
Second (3–4 pin shorted)	Forced CCM

5.4 Enable Selection

Use J2 to enable and disable the controller.

Default setting: Jumper shorts on J2 to disable the controller

Table 5-4. Enable Selection

JUMPER SET TO	ENABLE SELECTION
Jumper shorts on J2	**Disable the controller**
No Jumper shorts on J2	Enable the controller

6 Test Procedure

6.1 Line and Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in Section 4 and Figure 4-2.
2. Ensure that the load is set to constant resistance mode and to sink 0 A_{DC}.
3. Ensure that all jumpers configuration settings are per Section 5.
4. Ensure that the jumper provided in the EVM shorts on J2 before V_{IN} is applied.
5. Increase V_{IN} from 0 V to 12 V, using V1 to measure input voltage.
6. Remove the jumper on J2 to enable the controller.
7. Use V2 to measure V_{OUT} voltage.
8. Vary the load from 0 A_{DC} to 20 A_{DC}; V_{OUT} must remain in load regulation.
9. Vary V_{IN} from 8 V to 14 V; V_{OUT} must remain in line regulation.
10. Put the jumper on J2 to disable the controller.
11. Decrease the load to 0 A.
12. Decrease V_{IN} to 0 V.

6.2 Control Loop Gain and Phase Measurement Procedure

The TPS53353EVM-744 contains a 10-Ω series resistor in the feedback loop for loop response analysis.

1. Set up EVM as described in Section 4 and Figure 4-2.
2. Connect a isolation transformer to test points marked TP10 and TP11.
3. Connect input signal amplitude measurement probe (channel A) to TP10. Connect a output signal amplitude measurement probe (channel B) to TP11.
4. Connect ground lead of channel A and channel B to TP12.
5. Inject approximately 40 mV or less signal through the isolation transformer.
6. Sweep the frequency from 100 Hz to 1 MHz with a 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolation transformer from bode plot test points before making other measurements (signal injection into feedback can interfere with accuracy of other measurements).

6.3 Test Point List

Table 6-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	VIN	Controller input
TP2	GND	Ground
TP3	GND	Ground
TP4	EN	Enable
TP5	V_{OUT}	Output voltage
TP6	LL	Switching node
TP7	GND	Ground
TP8	PGOOD	Power Good
TP9	VREG	5-V LDO output
TP10	CHA	Input A for loop injection
TP11	CHB	Input B for loop injection
TP12	GND	GND

6.4 Equipment Shutdown

1. Shut down the load.
2. Shut down V_{IN}.
3. Shut down the fan.

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-15 present typical performance curves for TPS53353EVM-744.

7.1 Efficiency

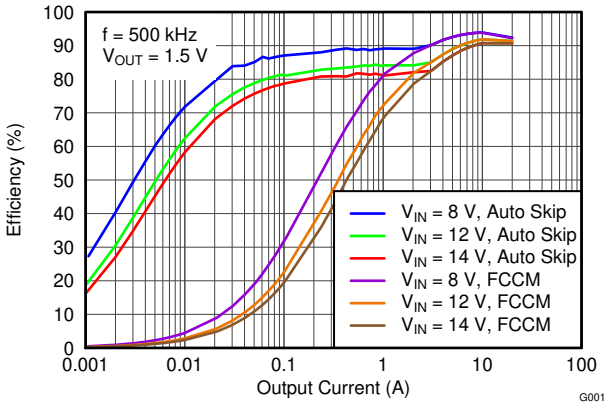

Figure 7-1. Efficiency

7.2 Load Regulation

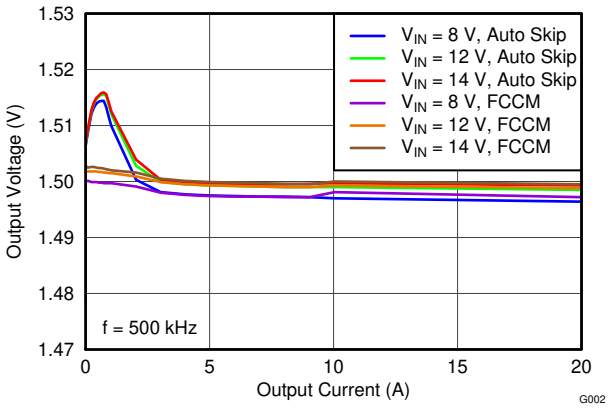

Figure 7-2. Load Regulation

7.3 Load Regulation

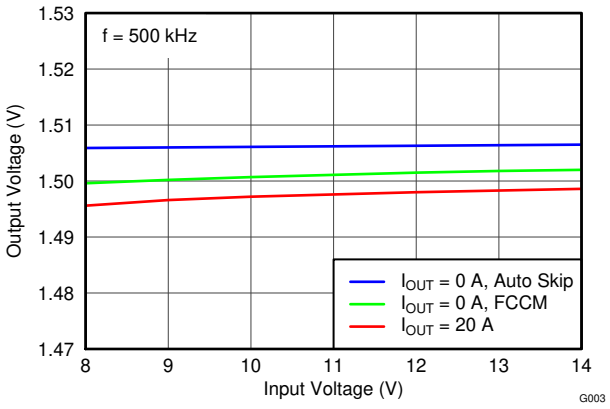

Figure 7-3. Line Regulation

7.4 Enable Turn-On/ Turn-Off

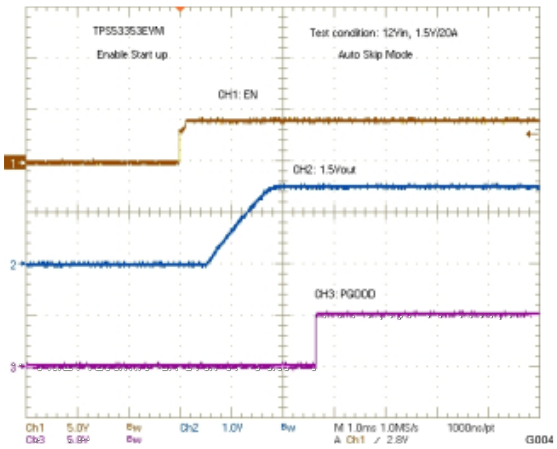

Figure 7-4. Enable Turn-On

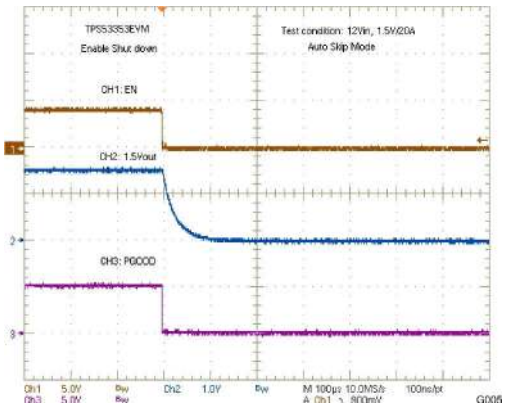

Figure 7-5. Enable Turn-Off

7.5 Output Ripple

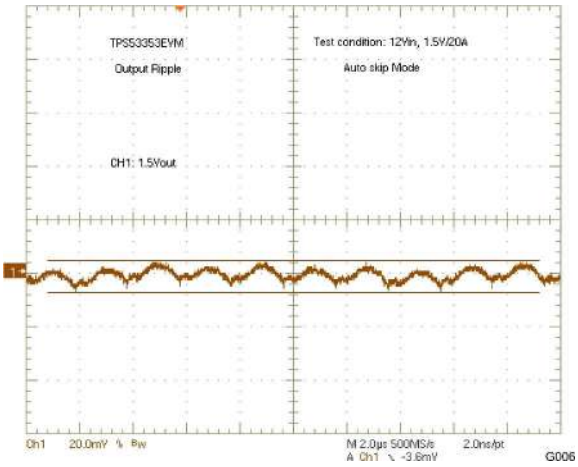

Figure 7-6. Output Ripple

7.6 Switching Node

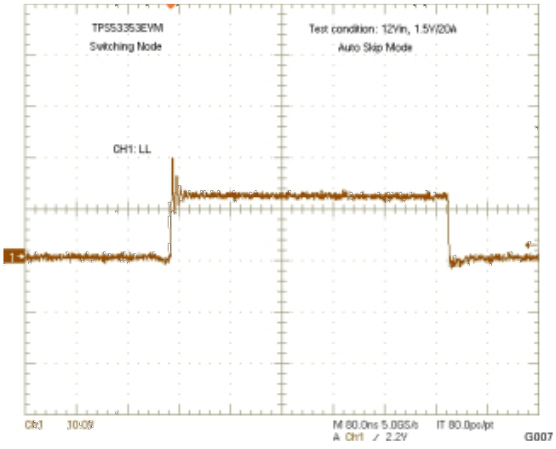

Figure 7-7. Switching Node

7.7 Output Transient With Auto-Skip Mode

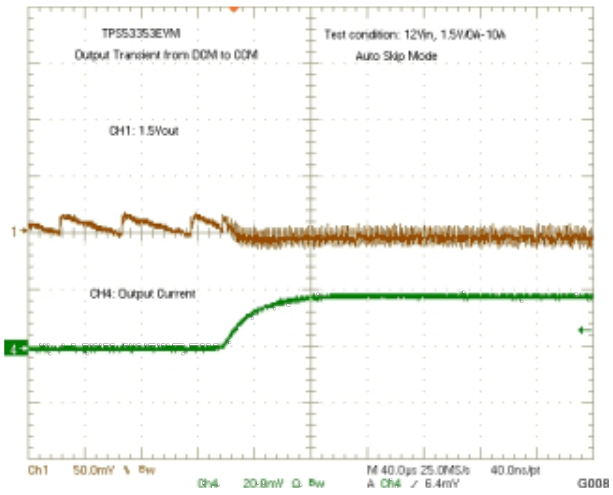

Figure 7-8. Output Transient From DCM to CCM

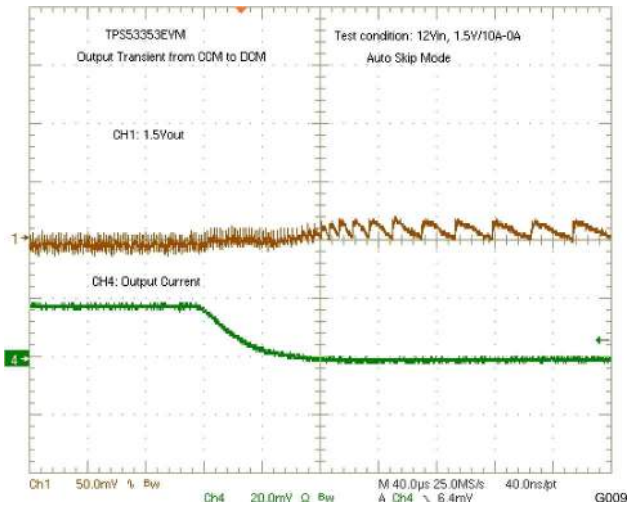

Figure 7-9. Output Transient From CCM to DCM

7.8 Output Transient With FCCM Mode

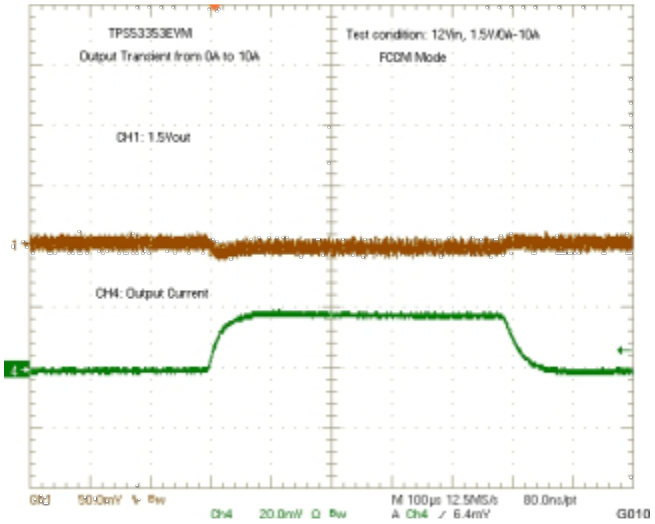

Figure 7-10. Output Transient With FCCM Mode

7.9 Output 0.75-V Prebias Turn-On

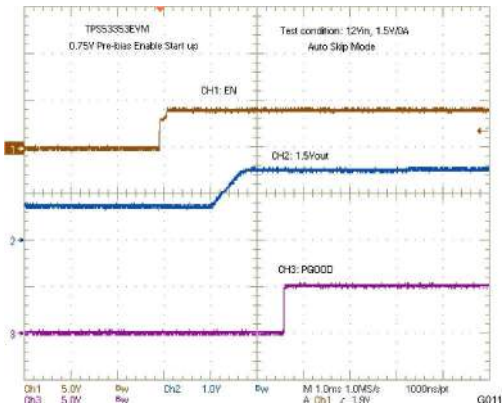

Figure 7-11. Output 0.75-V Prebias Turn-On

7.10 Output Overcurrent and Short-Circuit Protection

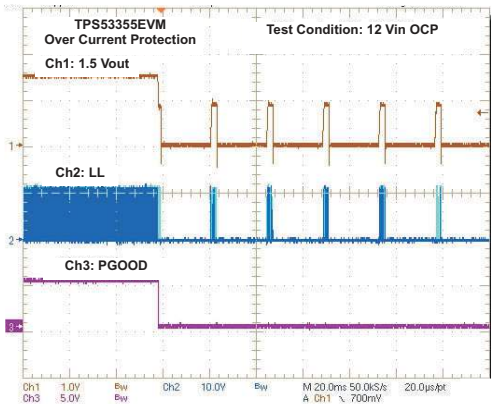

Figure 7-12. Output Overcurrent Protection

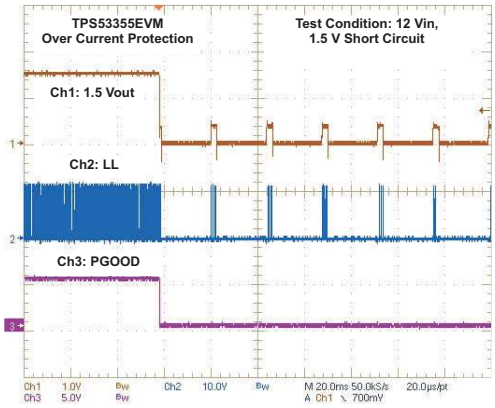

Figure 7-13. Output Short Circuit

7.11 Bode Plot

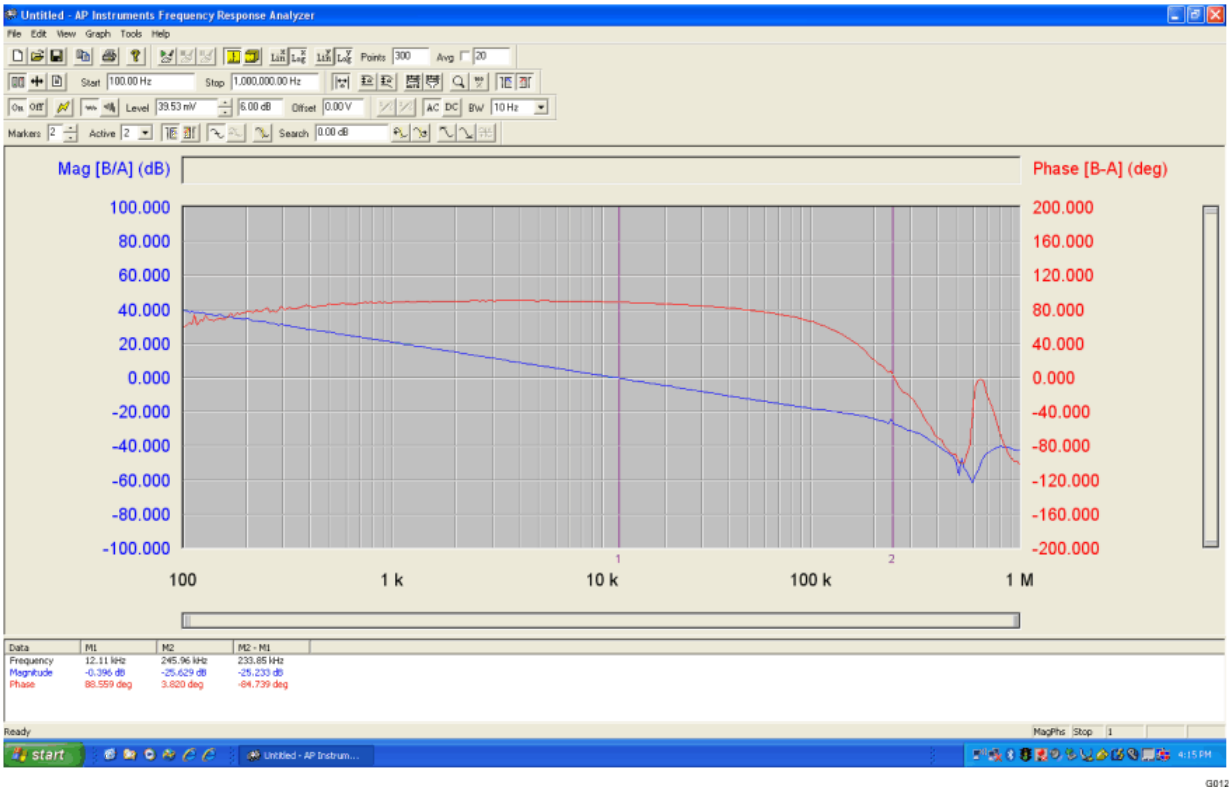

Figure 7-14. Bode Plot at 12 V_{IN}, 1.5 V/20 A

7.12 Thermal Image

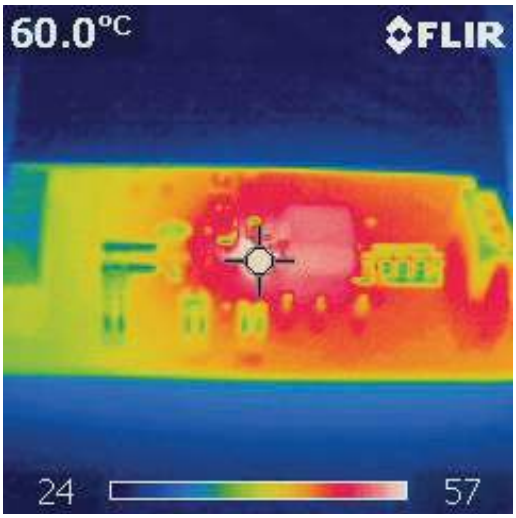

Figure 7-15. Top Board at 12 V_{IN}, 1.5 V/20 A, 25°C Ambient Temperature Without Airflow

8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 8-1 through Figure 8-8) show the design of the TPS53353EVM-744 printed-circuit board (PCB). The EVM was designed using a 6-layer, 2-oz copper, PCB.

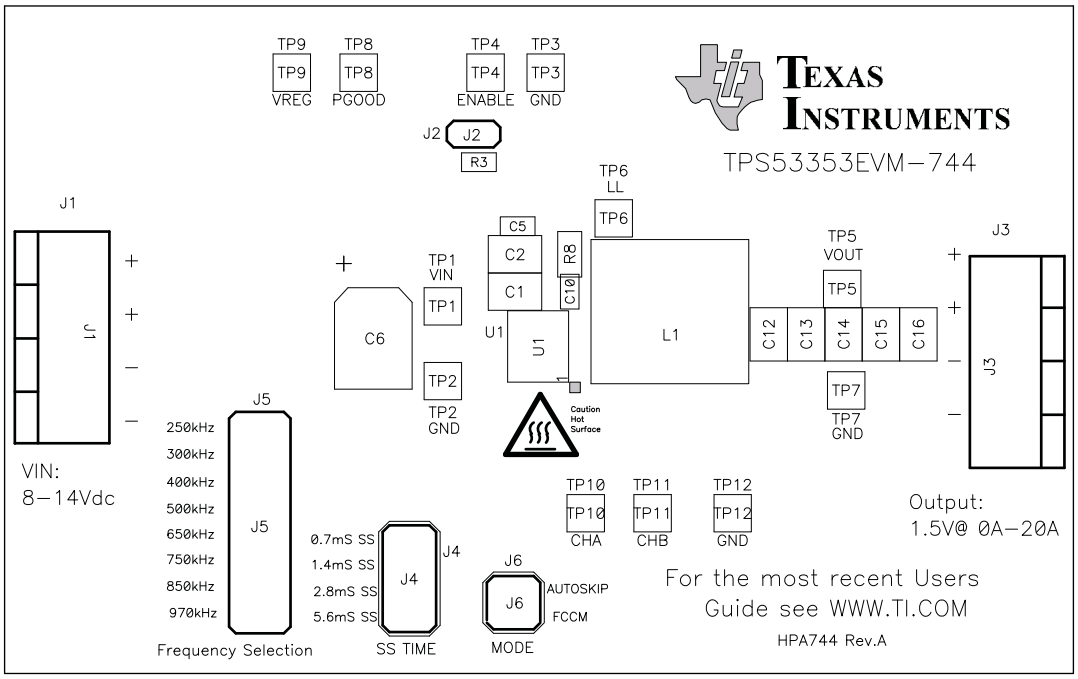

Figure 8-1. TPS53353EVM-744 Top Layer Assembly Drawing

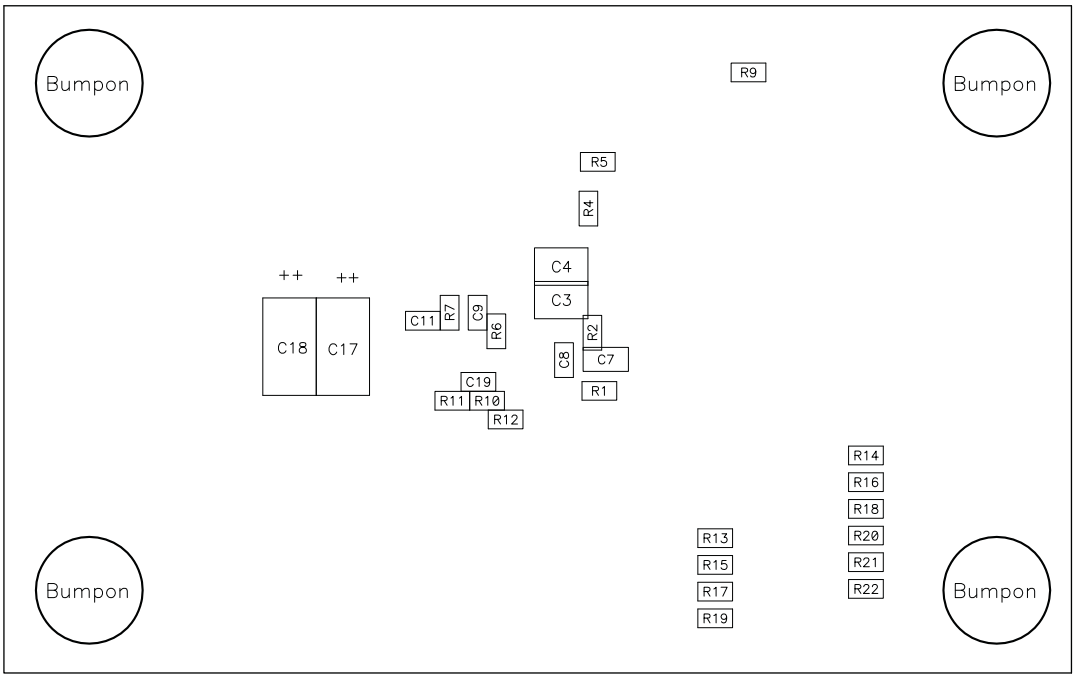

Figure 8-2. TPS53353EVM-744 Bottom Assembly Drawing

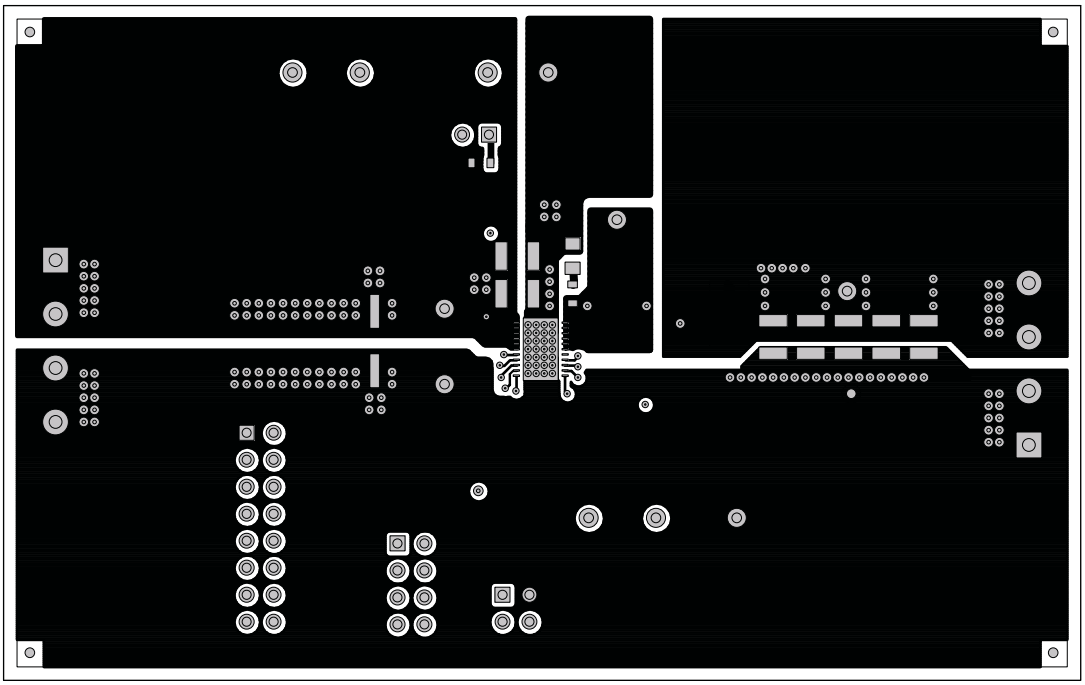

Figure 8-3. TPS53353EVM-744 Top Copper

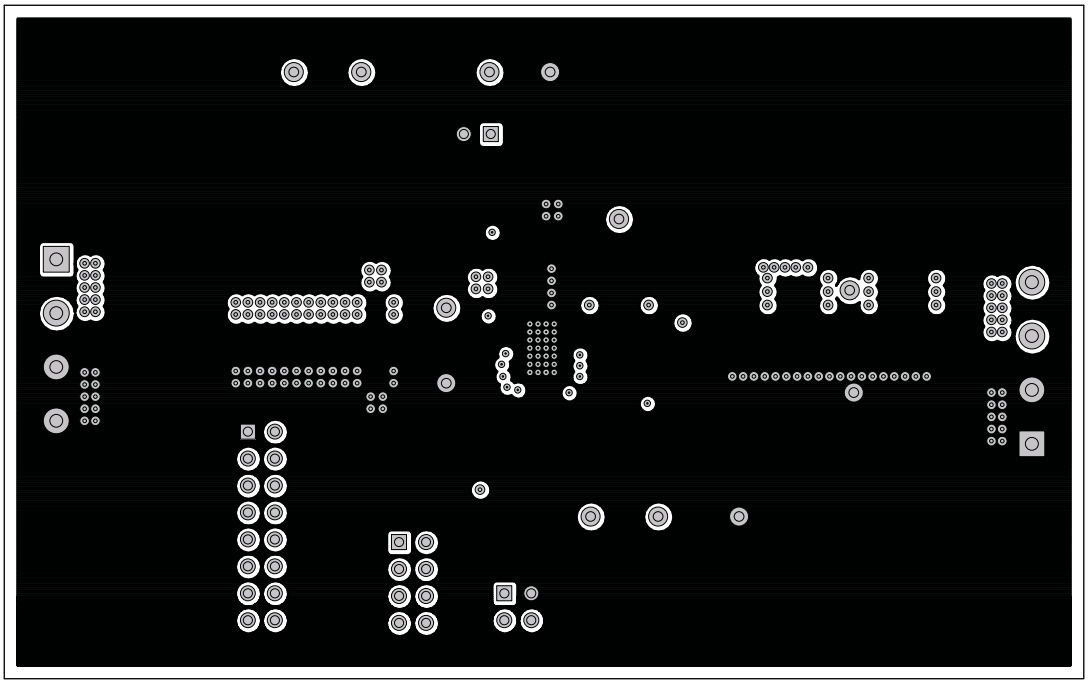

Figure 8-4. TPS53353EVM-744 Layer-2 Copper

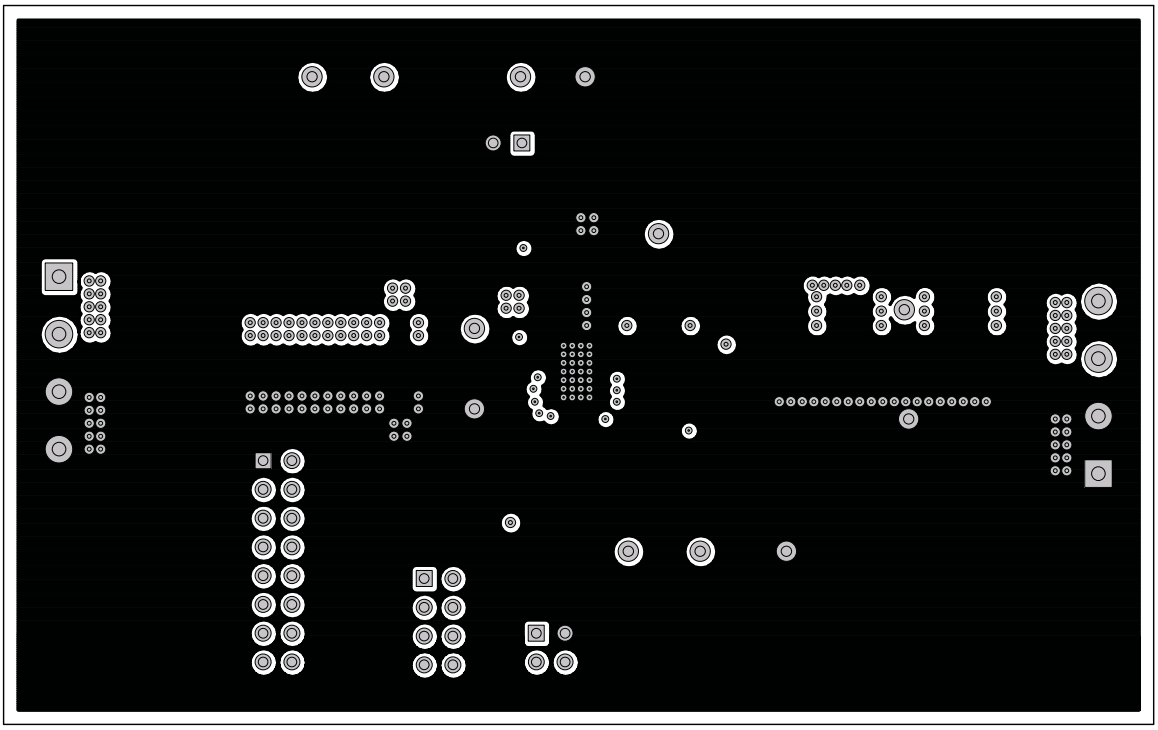

Figure 8-5. TPS53353EVM-744 Layer-3 Copper

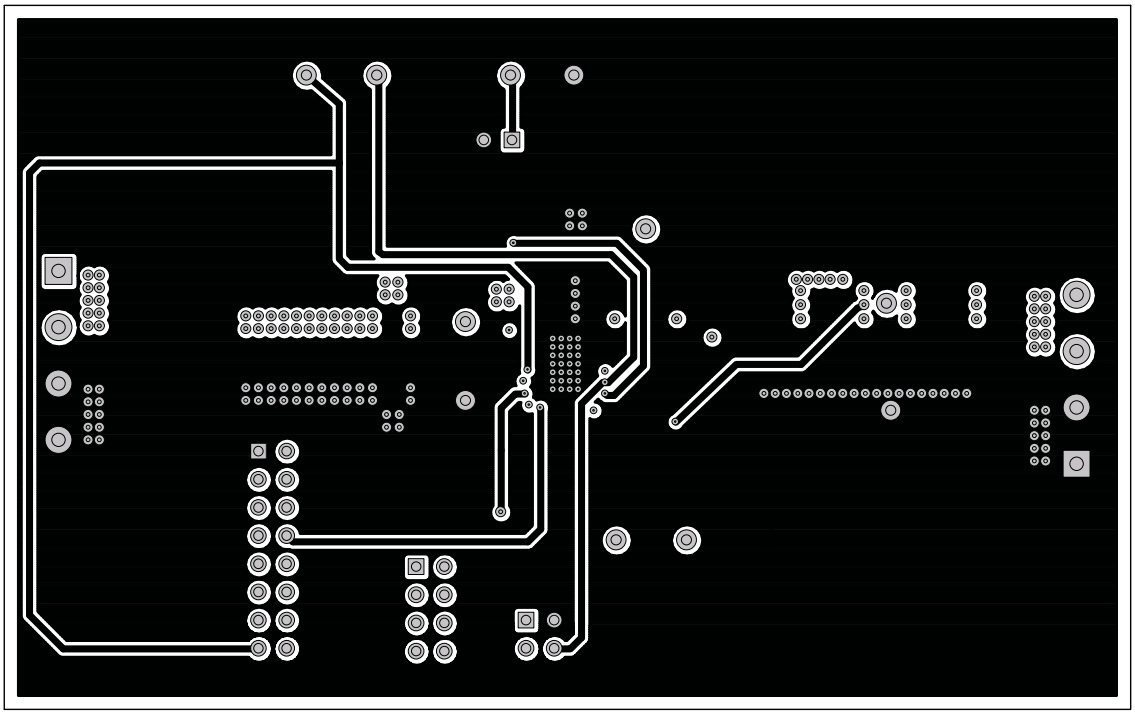

Figure 8-6. TPS53353EVM-744 Layer-4 Copper

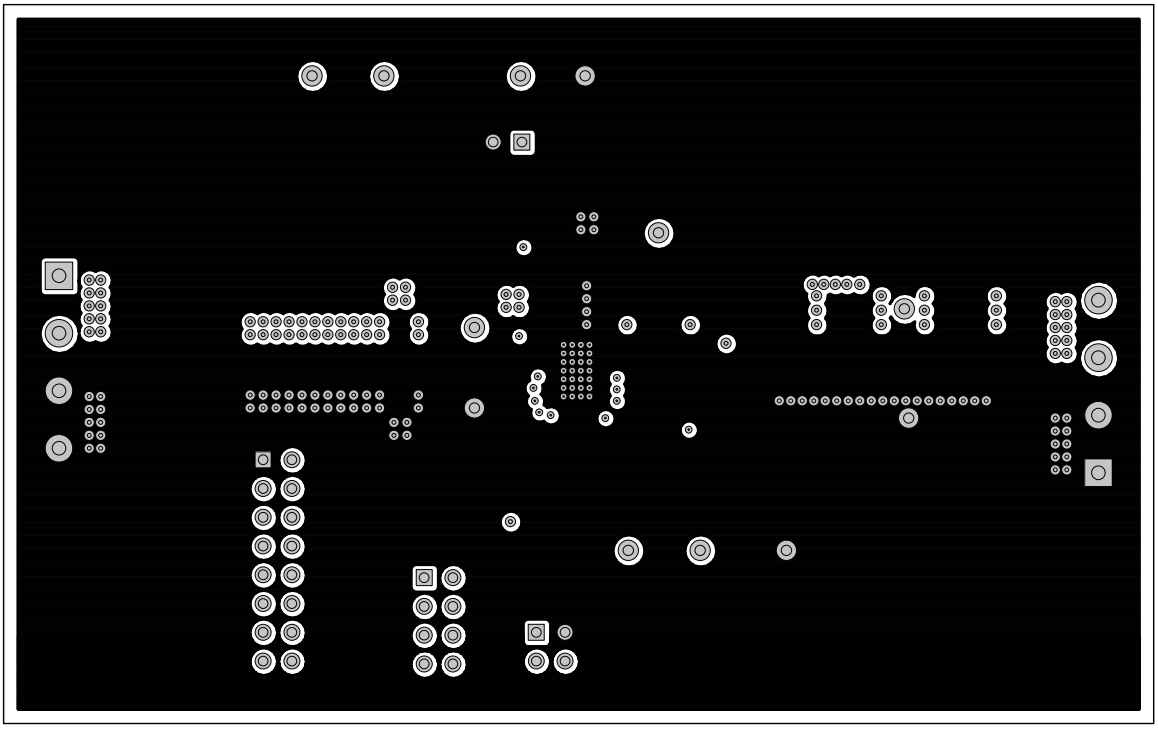

Figure 8-7. TPS53353EVM-744 Layer-5 Copper

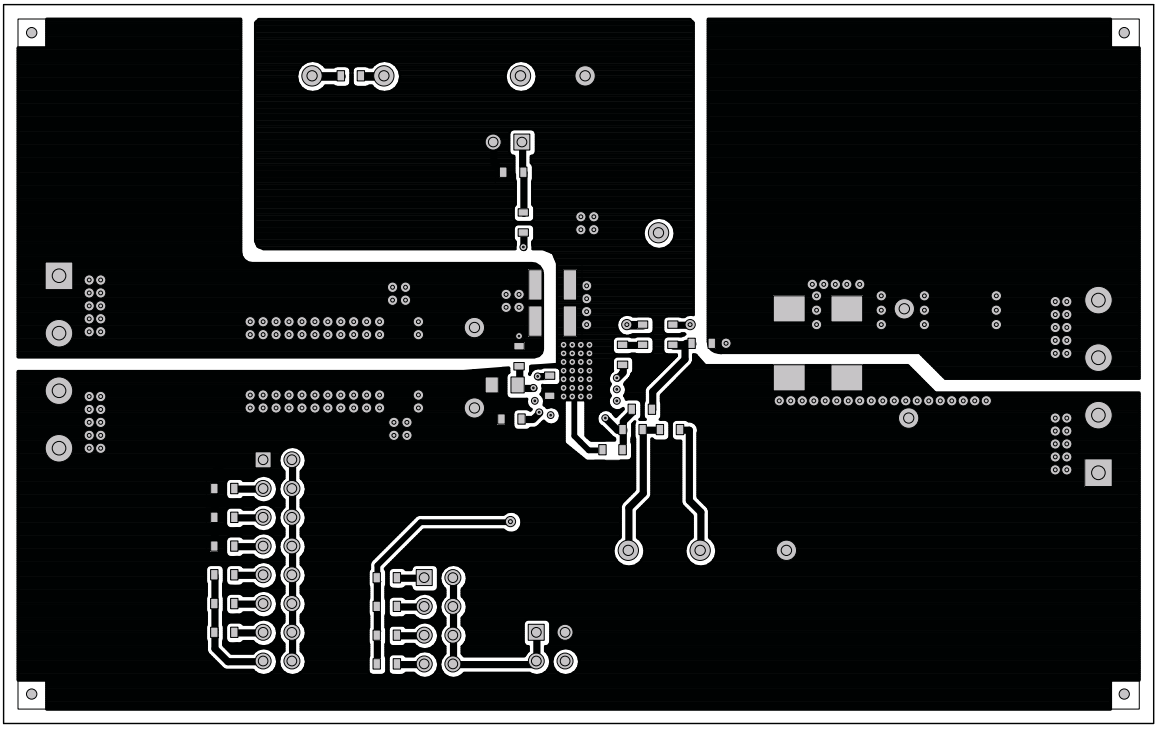

Figure 8-8. TPS53353EVM-744 Bottom Layer Copper

9 Bill of Materials

Table 9-1. TPS53353EVM-744 Bill of Materials

QTY	REFDES	DESCRIPTION	MFR PART	NUMBER
4	C1–C4	Capacitor, Ceramic, 22 µF, 16 V, X5R, 20%, 1210	MURATA	GRM32ER61C226KE20L
5	C12–C16	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 20%, 1210	MURATA	GRM32ER60J107ME20L
1	C10	Capacitor, Ceramic, 2.2 nF, 50 V, X7R, 20%, 0603	STD	STD
1	C11	Capacitor, Ceramic, 0.022 µF, 50V, X7R, 20%, 0603	STD	STD
1	C19	Capacitor, Ceramic, 1000 pF, 50 V, X7R, 20%, 0603	STD	STD
2	C5, C9	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 20%, 0603	STD	STD
1	C6	Capacitor, Aluminum, 100 µF, 16 VDC, 20%, Code D8	Panasonic	EEEFP1C101AP
1	C7	Capacitor, Ceramic, 4.7 µF, 25 V, X5R, 20%, 0805	STD	STD
1	C8	Capacitor, Ceramic, 1 µF, 50 V, X7R, 20%, 0603	STD	STD
1	L1	Inductor, SMT, 0.44 µH, 30 A, 0.0032 Ω, 0.53” x 0.510”	Pulse	PA0513-441NLT
1	R1	Resistor, Chip, 110 k, 1/16W, 1%, 0603	STD	STD
1	R11	Resistor, Chip, 10, 1/16W, 1%, 0603	STD	STD
1	R12	Resistor, Chip, 10.0 k, 1/16W, 1%, 0603	STD	STD
1	R13	Resistor, Chip, 39.2 k, 1/16W, 1%, 0603	STD	STD
1	R14	Resistor, Chip, 187 k, 1/16W, 1%, 0603	STD	STD
1	R16	Resistor, Chip, 619 k, 1/16W, 1%, 0603	STD	STD
1	R19	Resistor, Chip, 475 k, 1/16W, 1%, 0603	STD	STD
1	R2	Resistor, Chip, 0, 1/16W, 1%, 0603	STD	STD
1	R20	Resistor, Chip, 866 k, 1/16W, 1%, 0603	STD	STD
1	R21	Resistor, Chip, 309 k, 1/16W, 1%, 0603	STD	STD
1	R22	Resistor, Chip, 124 k, 1/16W, 1%, 0603	STD	STD
2	R3, R17	Resistor, Chip, 200 k, 1/16W, 1%, 0603	STD	STD
3	R5, R9, R15	Resistor, Chip, 100 k, 1/16W, 5%, 0603	STD	STD
1	R4	Resistor, Chip, 1.00 k, 1/16W, 1%, 0603	STD	STD
1	R6	Resistor, Chip, 2.05, 1/16W, 1%, 0603	STD	STD
2	R7, R10	Resistor, Chip, 14.7 k, 1/16W, 1%, 0603	STD	STD
1	R8	Resistor, Chip, 3.01, 1/16W, 1%, 0805	STD	STD
1	U1	IC, 20-A synchronous buck converter with integrated MOSFETs, DQP-22	TI	TPS53353DQP

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2011) to Revision A (November 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2
- Edited user's guide for clarity..... 2

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