C8051F064 Evaluation Kit User's Guide

1. Kit Contents

C8051F064 Evaluation Kits contain the following items:

- C8051F064 Evaluation Board
- Silicon Laboratories Evaluation Kit IDE and Product Information CD-ROM. CD content includes the following:
  - Silicon Laboratories Integrated Development Environment (IDE)
  - Keil Software 8051 Development Tools (evaluation assembler, linker, and "C" compiler)
  - Source code examples and register definition files
  - Documentation
  - Evaluation Kit Demos, C8051F064 ADC Demo
- 6' USB Cables (2)
- C8051F064 Evaluation Kit User's Guide

2. Kit Overview

Figure 1 illustrates the block diagram of the C8051F064 Evaluation Kit. The board includes an analog front end to signal condition and digitize (through the C8051F064) analog input signals. The board also includes two USB ports to transfer conversions to a PC: the DATA Port and the Self-Demo/IDE Debug port. The DATA port consists of a Silicon Laboratories CP2101 (UART to USB bridge) and a USB connector. The Self-Demo/IDE Debug port consists of Silicon Laboratories' debug interface hardware and a USB connector.

Power for the C8051F064 board can be supplied from either USB connection. An alternative lower noise supply can be used for better measurement performance if desired. Refer to Section 7 "Evaluation board" for more details.

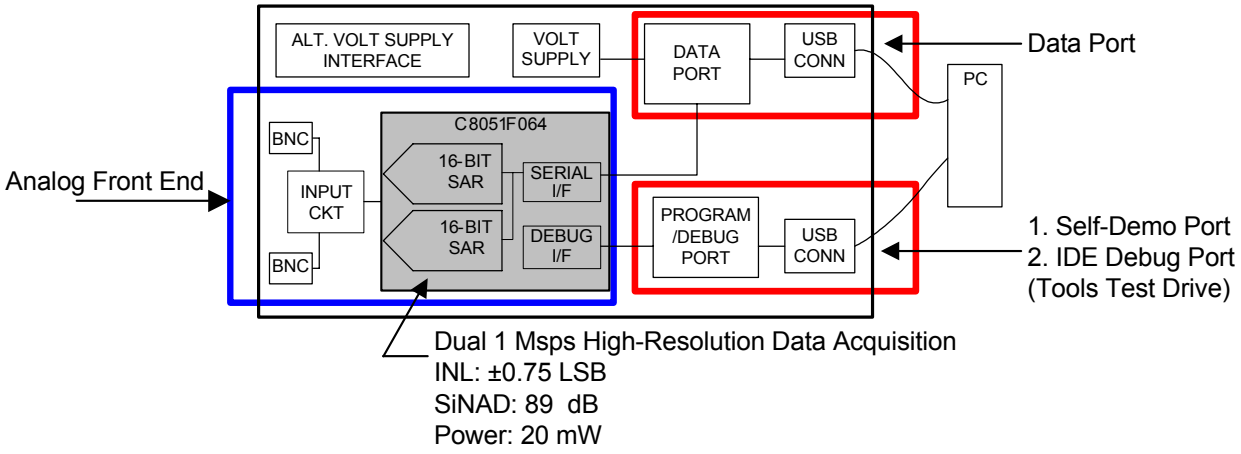

Figure 1. C8051F064 Evaluation Board Block Diagram

The C8051F064EK has three purposes:

- Noise Performance Demonstration—Demonstrates 16-bit dc performance; displays FFT plot and key parameters.
- Performance Evaluation—Facilitates easy programming and analog front end input for dynamic performance evaluation of ac signals.
- Tools Test Drive—Allows easy evaluation of the Silicon Laboratories Integrated Development Environment (IDE) (code download and on-chip debug function).

3. Evaluation Kit ADC Demo

The C8051F064 evaluation kit includes a demonstration of the noise performance of the 16-bit ADCs on the C8051F064 device. A 1.25 V dc input signal is provided on the board as an input to the ADC input pins, AIN0 and AIN1. The ADCs convert and store 32,768 samples (differential, 16-bit samples in 2s complement) in off-chip SRAM. The PC application then downloads the data through the debug USB port. After processing these conversions, the software generates a spectral plot (magnitude versus frequency) of the ADC input signal. The spectral plot illustrates the C8051F064s noise floor for the given sample set. The minimum and maximum values sampled, mean of values sampled, standard deviation, and dynamic range are displayed. To run the ADC Demo, first configure the evaluation board and install the PC application.

3.1. ADC Demo Hardware Setup

Configure the evaluation board according to the instructions below. A diagram of the final configuration is shown in Figure 2. Configuration shorting blocks may already be installed.

1. Place a shorting block on the J2 header connecting pin2 and pin3. This configures the evaluation board to be powered from the DEBUG USB connector (J1).
2. Place a shorting block on the J4 header connecting pin2 and pin3. This configures the external voltage reference to be powered from the DEBUG USB connector (J1).
3. Place shorting blocks on the "V+" (J6) and "V–" (J8) headers.
4. Configure SRAM(U5): Place shorting blocks on J11 and on J14 connecting pin2 and pin3.
5. Connect one end of the provided USB cable to any available USB port on the PC.
6. Connect the other end of the USB cable into the USB connector on the board labeled "DEBUG" (J1). This connection should power the board. Evaluation board power is indicated by the "PWR" LED (D4).

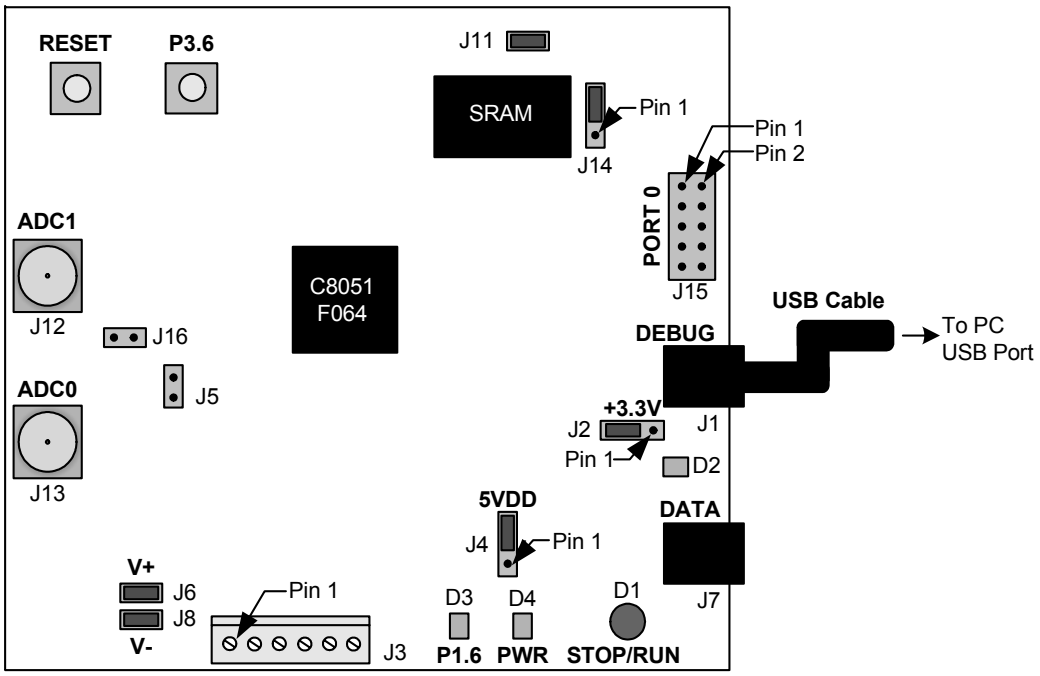

Figure 2. ADC Demo Hardware Setup

3.2. ADC Demo Software Installation

Install the ADC Demo application software according to the instructions below.

1. Place the Evaluation Kit CD-ROM into the PC.
2. An installation dialogue box will appear. Click the “Install Evaluation Kit Demos” button.
3. The Demos windows will open showing the available Evaluation Kit Demos. To install the application, click the “C8051F064EK ADC Demo” button.
4. Follow the installation prompts to install the demo application. By default, the software will be installed in the C:\Silabs\MCU\Demos\C8051F06x directory. In addition, shortcuts to the application will be placed on the desktop and in the Start > Programs menu.

3.3. Running the ADC Demo Software

To run the demo, run the installed application. When executed, the following occurs automatically:

1. Firmware is downloaded to the C8051F064 FLASH code memory.
2. The C8051F064’s 8051 MCU executes the firmware to configure the 16-bit ADC, direct memory access (DMA) interface, and parallel interface to store samples in the onboard SRAM.
3. The ADCs sample a dc voltage (32,768 samples) to measure the inherent noise floor of the ADC and analog front-end (AFE) circuit.
   Note: There is also noise contributed by the circuit board, including noise from the USB connection to the ground on the PC.
4. The ADC performs data conversions, and the DMA stores these samples in the onboard SRAM via a parallel interface.
5. Once the ADC samples are stored, the application reads these samples from the board (download through the DEBUG USB port) and analyzes them.
6. The application displays a frequency analysis plot of the samples and shows their maximum, minimum, and mean values and the standard code deviation or "sigma" (in LSBs) and calculates the dynamic range based on a full-scale signal (rms) value. Such an evaluation is an important dc noise performance measurement of high-resolution ADCs.

4. Software Setup

The included CD-ROM contains the Silicon Laboratories Integrated Development Environment (IDE), Keil software 8051 tools, and additional documentation. Insert the CD-ROM into your PC’s CD-ROM drive. An installer will automatically launch allowing you to install the IDE software or read documentation by clicking buttons on the Installation Panel. If the installer does not automatically start when you insert the CD-ROM, run *autorun.exe* found in the root directory of the CD-ROM. Refer to the *readme.txt* file on the CD-ROM for the latest information regarding known IDE problems and restrictions.

5. Silicon Laboratories Integrated Development Environment (IDE)

The Silicon Laboratories IDE integrates a source-code editor, source-level debugger, and in-system Flash programmer. The use of third-party compilers and assemblers is also supported. This evaluation kit includes the Keil Software A51 macro assembler, BL51 linker, and evaluation version C51 “C” compiler. These tools can be used from within the Silicon Laboratories IDE.

5.1. System Requirements

The Silicon Laboratories’ IDE requirements are as follows:

- Pentium-class host PC running Microsoft Windows 95 or later, or Microsoft Windows NT or later.
- One available COM port.
- 64 MB RAM and 40 MB free HD space recommended.

5.2. Assembler and Linker

A full-version Keil A51 macro assembler and BL51 banking linker are included with the evaluation kit and are installed during IDE installation. The complete assembler and linker reference manual can be found online under the Help menu in the IDE or in the “*SiLabs\MCU\hlp*” directory (A51.pdf).

5.3. Evaluation C51 'C' Compiler

An evaluation version of the Keil C51 "C" compiler is included with the evaluation kit and is installed during IDE installation. The evaluation version of the C51 compiler is the same as the full professional version, except code size is limited to 2 kB and the floating point library is not included. The C51 compiler reference manual can be found under the Help menu in the IDE or in the "*SiLabs\MCU\hlp*" directory (C51.pdf).

5.4. Using the Keil Software 8051 Tools with the Silicon Laboratories IDE

To perform source-level debugging with the IDE, configure the Keil 8051 tools to generate an absolute object file in the OMF-51 format with object extensions and debug records enabled. Build the OMF-51 absolute object file by calling the Keil 8051 tools at the command line (e.g., batch file or make file) or by using the project manager built into the IDE. The default configuration when using the Silicon Laboratories IDE project manager enables object extension and debug record generation. Refer to the application note "AN104: Integrating Keil 8051 Tools Into the Silicon Labs IDE" in the "*SiLabs\MCU\Documentation\Appnotes*" directory on the CD-ROM for additional information on using the Keil 8051 tools with the Silicon Laboratories IDE.

To build an absolute object file using the Silicon Laboratories IDE project manager, first create a project. A project consists of a set of files, IDE configuration, debug views, and a target build configuration (a list of files and tool configurations used as input to the assembler, compiler, and linker when building an output object file).

The following sections describe the steps necessary to manually create a project with one or more source files and build and download a program to the target in preparation for debugging. (If Build/Make Project is selected before a project is defined, the IDE automatically creates a single-file project using the currently open and active source file.)

5.4.1. Creating a New Project

1. Select Project > New Project to open a new project and reset all configuration settings to default.
2. Select File > New File to open an editor window. Create your source file(s) and save the file(s) with a recognized extension such as .c, .h, or .asm, to enable color syntax highlighting.
3. Right-click on New Project in the project window. Select Add Files to Project. Select files in the file browser and click Open. Continue adding files until all project files have been added.
   For each of the files in the project window that you want assembled, compiled, and linked into the target build, right-click on the file name and select Add File to Build. Each file will be assembled or compiled as appropriate (based on its file extension) and linked into the build of the absolute object file.
   Note: If a project contains a large number of files, the Group feature of the IDE can be used to organize them. Right-click on New Project in the project window. Select Add Groups to Project. Add predefined or customized groups. Right-click on the group name and choose Add File to Group. Select the files to be added. Continue adding files until all project files have been added.

5.4.2. Building and Downloading the Program for Debugging

1. Once all source files have been added to the target build, build the project by clicking on the Build/Make Project button in the toolbar or by selecting Project > Build/Make Project from the menu.
   Note: After the project has been built the first time, the Build/Make Project command will only build the files that have been changed since the previous build. To rebuild all files and project dependencies, click the Rebuild All button in the toolbar or select Project > Rebuild All from the menu.
2. C8051F064 family devices use the JTAG debug interface. You must select JTAG in the Options > Debug Interface menu to enable connection to C80512xx target devices. Click the Connect button in the toolbar or select Debug > Connect from the menu to connect to the device.
3. Download the project to the target by clicking the Download Code button in the toolbar.
   Note: To enable automatic downloading if the program build is successful, select Enable Automatic Connect/Download after Build in the Project > Target Build Configuration dialog. If errors occur during the build process, the IDE will not attempt the download.
4. Save the project when finished with the debug session to preserve the current target build configuration, editor settings, and the location of all open debug views. To save the project, select Project > Save Project As... from the menu. Create a new name for the project and click Save.

6. Example Source Code

Example source code and register definition files are provided in the "*SiLabs\MCU\Examples\C8051F06x*" directory during IDE installation. These files may be used as a template for code development. Example applications include a blinking LED example that configures the green LED on the evaluation board to blink at a fixed rate.

6.1. Register Definition Files

Register definition files *C8051F060.inc and C8051F060.h* define all SFR registers and bit-addressable control/status bits. They are installed into the "*SiLabs\MCU\Examples\C8051F06x*" directory during IDE installation. The register and bit names are identical to those used in the C8051F06x data sheet. Both register definition files are also installed in the default search path used by the Keil Software 8051 tools. Therefore, when using the Keil 8051 tools included with the evaluation kit (A51, C51), it is not necessary to copy a register definition file to each project's file directory.

6.2. Blinking LED Example

The example source files, *blink.asm* and *blinky.c*, show examples of several basic C8051F06x functions. These include disabling the watchdog timer (WDT), configuring the Port I/O crossbar, configuring a timer for an interrupt routine, initializing the system clock, and configuring a GPIO port. When compiled/assembled and linked, this program flashes the green LED on the evaluation board about five times a second using the interrupt handler with a timer.

7. Evaluation board

The C8051F064 Evaluation Kit includes an evaluation board with a C8051F064 device pre-installed for evaluation and preliminary software development. Numerous input/output (I/O) connections are provided to facilitate prototyping using the evaluation board. Refer to Figure 3 for the locations of the various I/O connectors.

J1	DEBUG USB port connector for code download and on-chip debug functions
J2	Evaluation board power supply selector
J3	Analog I/O terminal block
J4	External voltage reference supply selector
J5	External conversion start header
J7	DATA USB port connector for data communications with the PC
J6, J8	Op-amp supply voltage headers
J11, J14	External memory interface connectors
J12, J13	ADC1 & ADC0; BNC connectors for analog inputs
J15	Port 0 header
J16	ADC differential input header

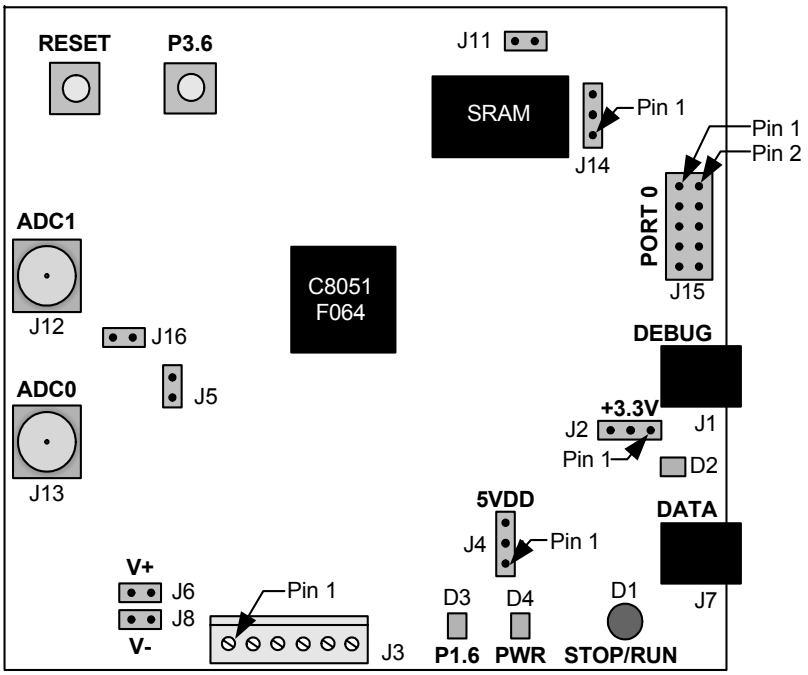

Figure 3. C8051F064 Evaluation Board

7.1. System Clock Sources

The C8051F064 device installed on the evaluation board features a calibrated programmable internal oscillator that is enabled as the system clock source on reset. After reset, the internal oscillator operates at a frequency of 3.0625 MHz (±2%) by default but may be configured by software to operate at other frequencies. Therefore, in many applications, an external oscillator is not required. However, an external 22.1184 MHz crystal is installed on the evaluation board for additional applications. Refer to the C8051F06x data sheet for more information on configuring the system clock source.

7.2. Switches and LEDs

Two switches are provided on the evaluation board. Switch SW1 is connected to the RESET pin of the C8051F064. Pressing SW1 puts the device into its hardware-reset state. Switch SW2 is connected to the C8051F060's general-purpose I/O (GPIO) pin P3.7. Pressing SW2 generates a logic low signal on the port pin.

Four LEDs are also provided on the evaluation board.

D1—The bi-color LED labeled "Run/Stop" indicates communications between the PC and the DEBUG USB port.
D2—The red LED D2 reflects the state of the SUSPEND signal of the DATA port device.
D3—The green LED labeled "P1.6" is connected to the C8051F064's GPIO pin P1.6.
D4—The red LED labeled "PWR" indicates a power connection to the evaluation board.

7.3. DEBUG Interface (J1)

The evaluation board DEBUG USB port (J1) provides the interface between a PC USB port and the C8051F064's in-system debug/programming circuitry. In addition, this port is used for the ADC Demo detailed in Section 3 "Evaluation Kit ADC Demo". Table 1 shows the DEBUG USB pin definitions.

Table 1. DEBUG USB Connector Pin Descriptions

Pin #	Description
1	VBUS
2	D–
3	D+
4	GND

7.4. DATA Interface (J7)

The evaluation board DATA USB port (J7) provides a data interface between a PC USB port and the CP2101 (Silicon Labs USB to UART bridge). This interface provides a virtual COM port via USB and will appear as a COM port to PC applications.Table 2 shows the DATA USB pin definitions.

Table 2. DATA USB Connector Pin Descriptions

Pin #	Description
1	VBUS
2	D–
3	D+
4	GND

7.5. Analog Inputs (J4, J5, J6, J8, J16, ADC0 [J13], ADC1 [J12])

Two BNC connectors (J13 (ADC0) and J12 (ADC1)) are provided on the C8051F064 board for easy evaluation of the 16-bit on-chip ADCs. These analog inputs can be used to input an ac analog signal to the ADCs, ADC0 and ADC1. Additionally, front-end circuitry is provided to condition the analog signals. To use this circuitry, follow the guidelines listed below in conjunction with the schematic located in Section 8 "Schematics". See "AN190: Understanding ADC Specifications" for a detailed discussion of issues related to ADC performance.

- Select the 5 V supply voltage for the Voltage References U3 and U6 at header J4. Place a shorting block on J4, pin1 and pin2, to select the DATA VBUS signal. Place a shorting block on J4, pin2 and pin3, to select the DEBUG VBUS signal.
- A single-supply voltage option is provided on the evaluation board for the op-amps. Place a shorting block on J6 to connect the "V+" op-amp supply to AV+. Additionally, place a shorting block on J8 to connect the "V–" op-amp supply to GND.
- Provide a dual-supply voltage to the op-amps for optimal performance by removing the shorting blocks on headers J6 and J8. To supply the voltages, +5 V and –5 V signals will need to be provided at the J3 terminal block (pin1 and pin2).

  Note: Remove shorting blocks from J6 and J8 BEFORE applying voltages to the J3 terminal block. Voltages applied to J3 while shorting blocks are on J6 and J8 could cause damage to the evaluation board.
- Provide an external Conversion Start signal to ADC0 at header J5 pin1.
- Provide an external Conversion Start signal to ADC1 at header J5 pin2.
- Differential measurement from one test source: input signal to ADC0 and place shorting block on header J16.

7.6. Analog I/O (Terminal Block [J3])

J3 is used to provide off-board voltage supply and voltage references for better noise performance evaluation in a lab environment. Refer to Table 3 for terminal block connections.

Table 3. Terminal Block (J3) Pin Descriptions

Pin #	Description
1	–5 V
2	+5 V
3	AGND
4	GND
5	+3.3 VIN
6	5VDD

7.7. External Memory Interface (J11, J14)

The C8051F064 evaluation board provides an External Memory Interface by connecting a 128 kB SRAM to the device port pins. The device's External Memory Interface can be enabled by installing a shorting block at header J11. This connects port pin P4.5 to the Chip Select ($\overline{CS}$) signal on the SRAM, pulling this signal low. Placing a shorting block on header J14, pin2 and pin3, enables the use of the lower address bank on the SRAM. Moving the shorting block to J14, pin1 and pin2, enables port pin P3.7 to select between the upper and lower address banks on the SRAM. Refer to Table 4 for the external memory interface signal descriptions.

Table 4. External Memory Interface Signal Descriptions

SRAM Signal	C8051F060 Signal	Description
$\overline{WE}$	P4.7	Write Enable
$\overline{CS}$	P4.5 (J11)	Chip Select
$\overline{OE}$	P4.6	Output Enable
V_{DD}	+3VD2	Digital Power
GND	GND	Digital Ground
I/O0...I/O7	P7.0...P7.7	Data Bus
A0...A7	P6.0...P6.7	Address Bus Low Byte
A8...A15	P5.0...P5.7	Address Bus High Byte
A16	P3.7 (J14[1-2])	Bank Select
A16	GND (J14[2-3])	Bank Select Always 0

7.8. PORT I/O Connectors (J15)

The Port 0 signals on the C8051F064 have their own 10-pin header (J15). This header provides a pin for each of the corresponding port pins 0-7, +3.3 V and digital ground. See Table 5 for the J15 pin connections.

Table 5. J15 Port Connector Pin Descriptions

Pin #	Description
1	P0.0
2	P0.1
3	P0.2
4	P0.3
5	P0.4
6	P0.5
7	P0.6
8	P0.7
9	+3 VD (+3.3 V)
10	GND (Ground)

7.9. Power Supply Selector (J2)

The C8051F064 evaluation board can be powered from either the DEBUG or DATA ports through the USB connection. The J2 header allows the user to select between these ports. Each configuration includes an on-board voltage regulator to supply 3.3 V to the board. To power the 3.3 V supply from the DATA port, place a shorting block on J2, pin1 and pin2. To supply the 3.3 V supply from the DEBUG port, place a shorting block on J2, pin2 and pin3.

Note: If supplying the 3.3 V supply from an off-board source via the J3 terminal block, do not place a shorting block on J2.

8. Schematics

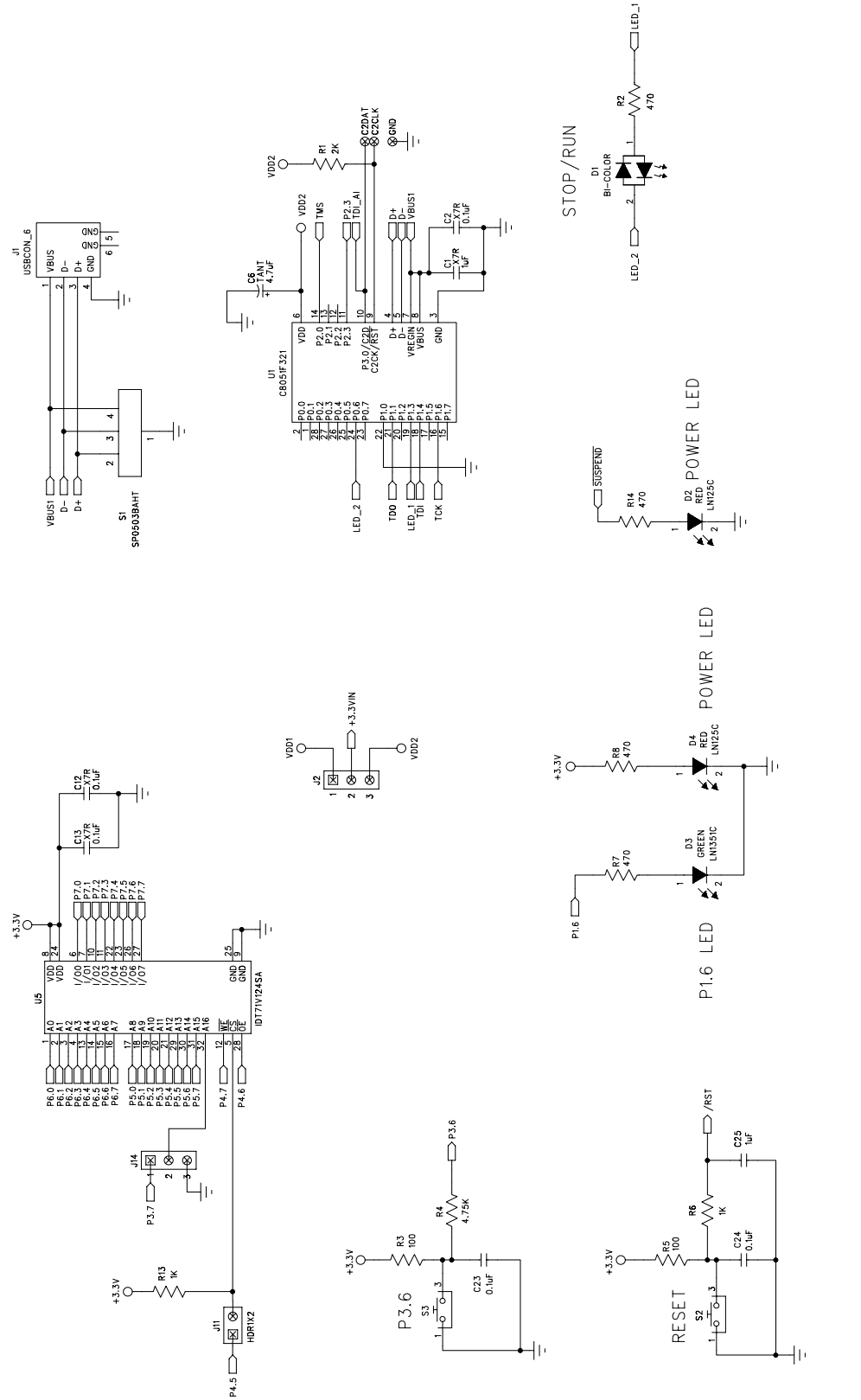

Figure 4. C8051F064 Evaluation Board Schematic Page 1

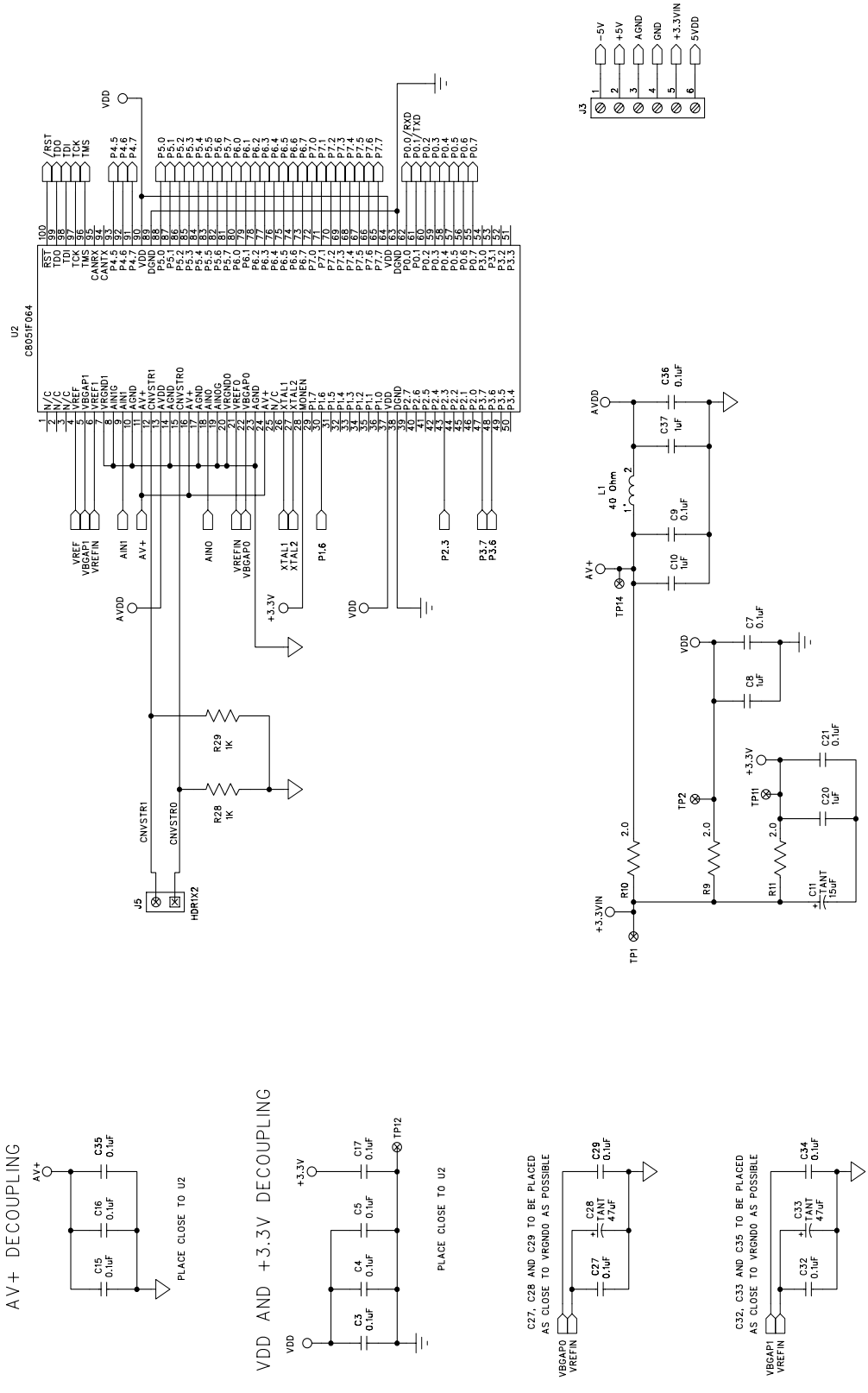

Figure 5. C8051F064 Evaluation Board Schematic Page 2

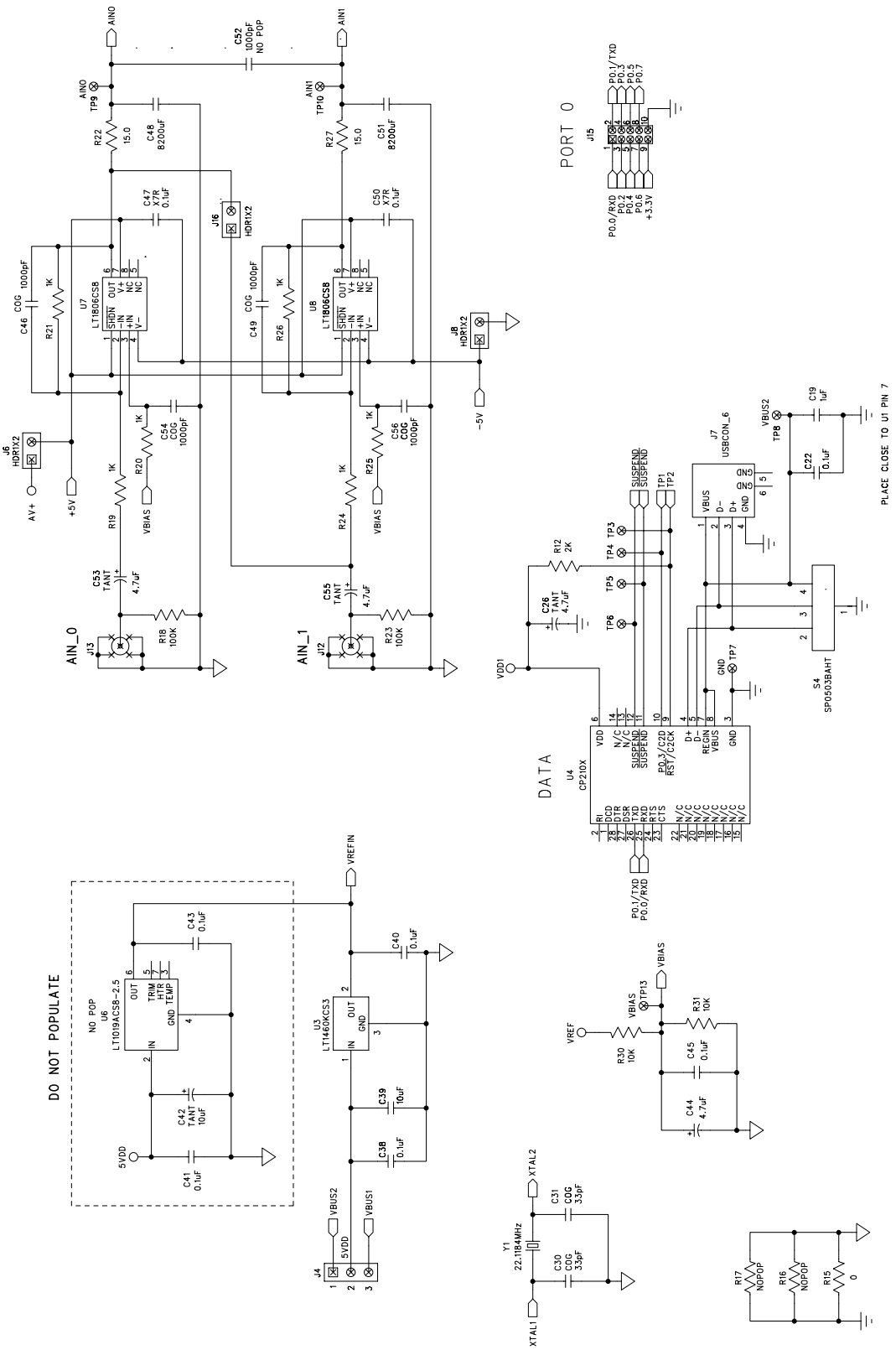

Figure 6. C8051F064 Evaluation Board Schematic Page 3

NOTES:

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