DLP-2232H

LEAD-FREE

DUAL-CHANNEL HIGH-SPEED USB ADAPTER

The DLP-2232H is DLP Design's premier USB-to-UART/FIFO interface module based on FTDI's 5th generation USB 2.0 High Speed (480Mb/s) silicon. The DLP-2232H is manufactured in a lead-free, RoHS-compliant, compact 40-pin, 0.1-inch spaced standard 0.6 inch wide DIP footprint.

FEATURES:

The DLP-2232H is drop in compatible with the DLP-2232M except for the difference in the VCCIO voltage. The DLP-2232H has a maximum VCCIO of +3.6 Volts, but as inputs it's IO pins are +5.0 Volt tolerant.

The DLP-2232H is shipped from the factory in DLP-2232M compatible mode. Refer to section 2.1 for mode select jumper configuration details.

The DLP-2232H has the capability of being configured in a variety of industry standard serial or parallel interfaces supporting these features:

- Entire USB protocol handled on the module. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Multi-Protocol Synchronous Serial Engine (MPSSE) to simplify synchronous serial protocol (USB to JTAG, I2C, SPI or bit-bang) design.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec.
- Single channel synchronous FIFO mode for transfers up to 25 Mbyte/Sec.
- Enhanced bit bang mode interface option with read and write strobes
- USB to Fast Serial Interface mode provides a method of communicating with an external device over USB using 4 wires that can have opto-isolators in their path for galvanic isolation
- MCU host bus emulation mode uses both ports to emulate a standard 8048/8051 host bus
- CPU-style FIFO interface mode simplifies CPU interface design.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.

• Adjustable receive buffer timeout.
• Transmit and receive LED drive signals.
• FT245B-style FIFO interface option with bidirectional data bus and simple 4 wire handshake interface.
• Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
• Fully assisted hardware or X-On / X-Off software handshaking.
• UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
• Auto-transmit enable control for RS485 serial applications using TXDEN pin.
• Operational configuration mode and USB Description strings configurable in on-board EEPROM over the USB interface.
• Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
• Low operating and USB suspend current.
• Supports bus powered, self powered and high-power bus powered USB configurations.
• UHCI/OHCI/EHCI host controller compatible.
• USB Bulk data transfer mode (512 byte packets in High Speed mode).
• +3.3V I/O interfacing (+5V Tolerant).
• Extended -40°C to 85°C industrial operating temperature range.

APPLICATION AREAS:

• Upgrading legacy peripherals to USB
• Interfacing MCU/PLD/FPGA-based designs to USB
• USB to UART (RS232, RS422 or RS485)
• USB to FIFO
• USB to Fast Serial Interface
• USB to JTAG
• USB to SPI
• USB to I2C
• USB to Bit-Bang
• USB to CPU target interface (as memory)
• USB to MCU (8048/8051 style) host bus emulation
• PDA to USB data transfer
• USB Smart Card Readers
• USB Instrumentation
• USB Industrial Control
• USB MP3 Player Interface
• USB FLASH Card Reader / Writers
• Set Top Box PC - USB interface
• USB Digital Camera Interface
• USB Bar Code Readers
• USB audio and low-bandwidth video data transfer
• USB hardware modems
• USB wireless modems

DRIVER SUPPORT:

Royalty-Free Virtual COM Port (VCP) Drivers for:
• Windows 2000, Server 2003, Server 2008
• Windows XP and XP 64-bit

• Windows Vista and Vista 64-bit
• Windows 7
• Windows CE 4.2, 5.0, and 5.2 based OS
• Mac OS-X
• Linux 2.6.31 or later

Royalty-Free D2XX Direct Drivers (USB Drivers + DLL S/W Interface) for:

• Windows 2000, Server 2003, Server 2008
• Windows XP and XP 64-bit
• Windows Vista and Vista 64-bit
• Windows 7
• Windows CE 4.2, 5.0, and 5.2 based OS
• Linux 2.6.31 or later

The drivers listed above are all available for free download from the DLP Design website **www.dlpdesign.com** and FTDI website **www.ftdichip.com**.

Various third-party drivers are also available for other operating systems; see the FTDI website **www.ftdichip.com** for details.

ABSOLUTE MAXIMUM RATINGS

• Storage Temperature	-65°C to +150°C
• Ambient Temperature (Power Applied)	-40 to +85°C
• VCC Supply Voltage	-0.5V to +6.00V
• DC Input Voltage: Inputs	-0.5V to VCC + 0.5V
• DC Input Voltage: High-Impedance Bidirectionals	-0.5V to VCC + 0.5V
• DC Output Current: Outputs	16mA

D.C. CHARACTERISTICS (AMBIENT TEMPERATURE: -40 TO 85°C)

• VCC Operating-Supply Voltage	4.0 - 5.5V
• VCCIO Digital IO Voltage	3.3V
• Operating Supply Current	75mA (Normal Operation)
• Operating Supply Current	500uA USB Suspend

1.0 GENERAL DESCRIPTION

The DLP-2232H USB 2.0 High Speed (480Mb/s) to UART/FIFO uses FTDI's 5th generation USB silicon. It has the capability of being configured in a variety of industry standard serial or parallel interfaces. The DLP-2232H can be configured for UART, FIFO, Fast serial interface, JTAG, SPI, I2C or bit-bang mode. In addition to these, the DLP-2232H supports a CPU interface FIFO mode and MCU host bus emulation mode.

Refer to the FT2232H datasheet for additional detail on how to set up and use these modes.

2.0 PIN DESCRIPTIONS

This section describes the operation of the DLP-2232H pins. The function of the I/O pins is determined by the configuration that is stored in the EEPROM connected to the FT2232H IC.

The following table details the function of each pin for the specified mode. Note that the convention used throughout this document for active low signals is the signal name followed by a #. Pins marked ** default to tri-stated inputs with an internal 75K Ohm (approx) pull up resistor to VCCIO (3.3V). Pins marked *** may require mode select jumper configuration. This is explained in section 2.1.

Table 1: DLP-2232H Pin Definitions

DLP-2232H										
Pin		Pin Functions For Each Supported Mode								
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial I/F	CPU Target	Host Emul-ation
Channel A										
40	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	Uses Chan B	D0	AD0
39	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
38	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
37	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
36	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0		D4	AD4
35	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1		D5	AD5
34	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2		D6	AD6
33	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3		D7	AD7
32	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOH0		CS#	A8
31	ACBUS1	**	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1		A0	A9
30	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
29	ACBUS3	TXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
28	ACBUS4	RXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4		SIWUA	A12
27	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
26	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
25	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
Channel B										
13	BDBUS0	TXD	Uses Chan A	D0	D0	D0	TCK/SK	FSDI	D0	CS#
12	BDBUS1	RXD		D1	D1	D1	TDI/DI	FSCLK	D1	ALE
11	BDBUS2	RTS#		D2	D2	D2	TDO/DO	FSDO	D2	RD#
10	BDBUS3	CTS#		D3	D3	D3	TMS/CS	FSCTS	D3	WR

9	BDBUS4	DTR#		D4	D4	D4	GPIOL0		D4	IORDY
8	BDBUS5	DSR#		D5	D5	D5	GPIOL1		D5	CLK OUT
7	BDBUS6	DCD#		D6	D6	D6	GPIOL2		D6	I/O0
6	BDBUS7	RI#		D7	D7	D7	GPIOL3		D7	1/01
5	BCBUS0	TXDEN		RXF#	**	**	GPIOH0			**
4	BCBUS1	**		TXE#			GPIOH1			**
3	BCBUS2	**		RD#			GPIOH2			**
2	BCBUS3	RXLED#		WR			GPIOH3			**
1	BCBUS4	TXLED#		SIWUB			GPIOH4			**
24	BCBUS5	**		**	**	**	GPIOH5		**	**
17[1]	BCBUS6	**		**	**	**	GPIOH6		**	**
18[2]	BCBUS7	PWR SAV#					GPIOH7			**

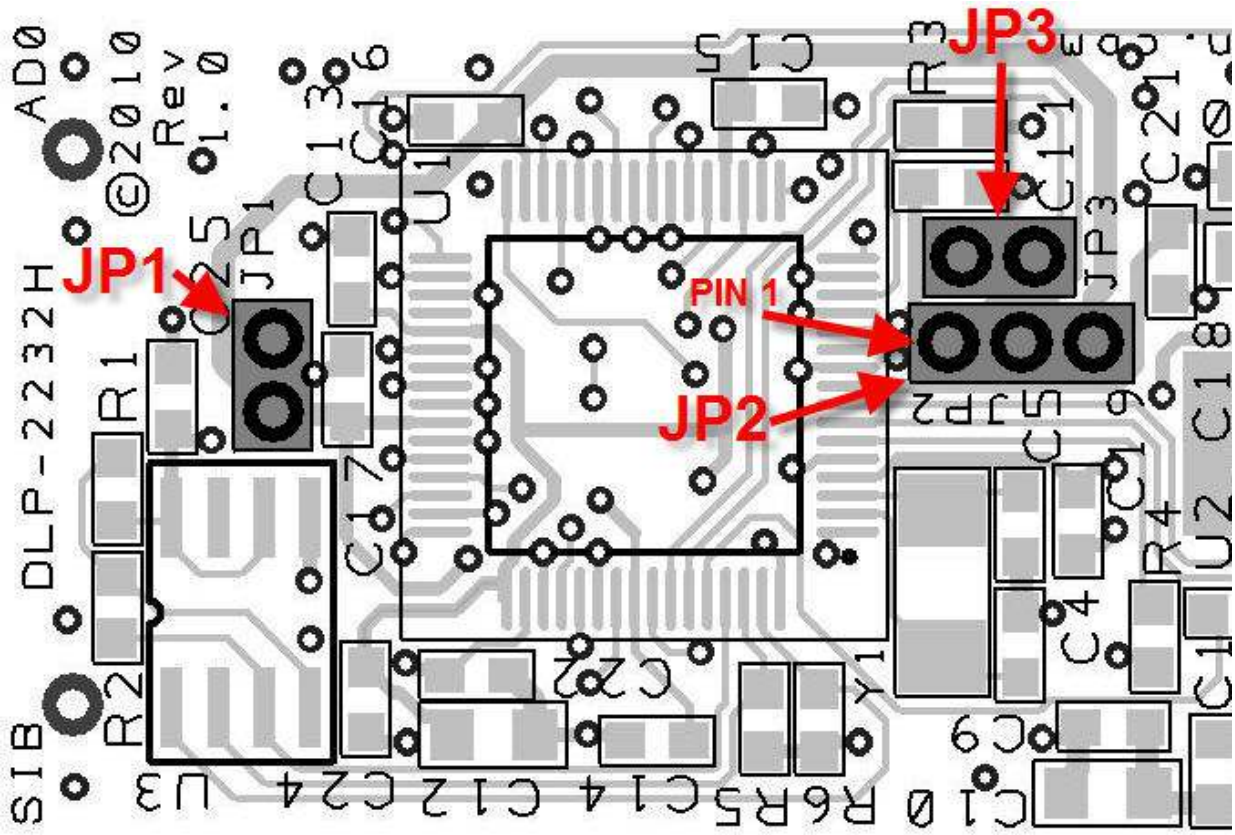
Support Pins		
Pin		**Function**
14	GND	**GROUND**
15	GND	**GROUND**
16	VCCSW	**VCCSW** - Use for powering external devices. This voltage is derived from the USB input +5.0V. It is switched off by the FT2232H PWREN# pin when the device is not enumerated. 500mA is the maximum current available to the USB adapter and target electronics if the USB device is configured for high power.
19	EXTVCC	**EXTVCC** - Use for applying main power (+4.5 to +5.25 V) to the module. Connect to PORTVCC if the module is to be powered by the USB port (typical configuration).
20	PORTVCC	**PORTVCC** - Power from the USB port (typically +5.0 V). Connect to EXTVCC if the module is to be powered by the USB port (typical configuration). 500mA is the maximum current available to the USB adapter and target electronics if the USB device is configured for high power.
21	VCCUSB	**VCCUSB** – Filtered power from the USB port (typically +5.0 V). 500mA is the maximum current available to the USB adapter and target electronics if the USB device is configured for high power.
22	GND	**GROUND**
23	GND	**GROUND**

Notes:

1. Pin 17 is configured via jumper JP2. Refer to section 2.1 for more details.
2. Pin 18 is configured via jumper JP3. Refer to section 2.1 for more details.

2.1 JUMPER CONFIGURATION

The DLP-2232H module was design so that it can be used as a drop in replacement for the DLP-2232M module. The DLP-2232H provides a high speed USB interface compared to the DLP-2232M module's full speed USB interface.



The mode select jumpers (**JP1 – JP3**) are identified above and on the silkscreen. They are located in the center and top of the DLP-2232H module. These three jumpers control the usage of the DLP-2232H module's pins 17 and 18 as follows:

JP1 (supports option for VCCIO +3.3V to be supplied internally):

1. Shunt installed on pins 1 and 2: VCCIO provided internally. **Insure that either JP2 shunt is in position 1, or no external voltage is applied to pin 17.**
2. Shunt not installed on pins 1 and 2: VCCIO applied externally (compatible with DLP-2232M). **VCCIO must not exceed +3.6V or module can be damaged.**

JP2 (controls pin 17):

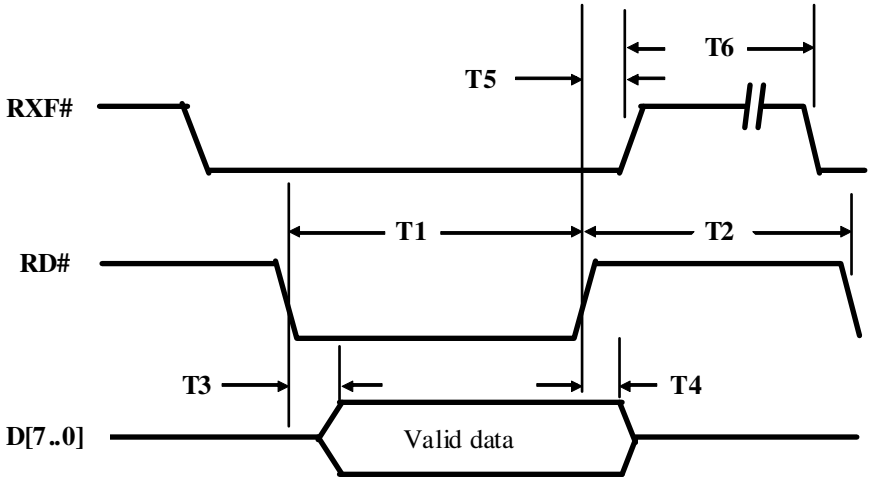
1. Shunt installed on pins 1 and 2: BCBUS6 signal available on pin 17.
2. Shunt installed on pins 2 and 3: VCCIO input available on pin 17 (compatible with DLP-2232M). **VCCIO must not exceed +3.6V or module can be damaged.**

JP3 (controls pin 18):

1. Shunt installed on pins 1 and 2: BCBUS7 signal available on pin 18.
2. No shunt installed: Pin 18 unconnected (compatible with DLP-2232M).

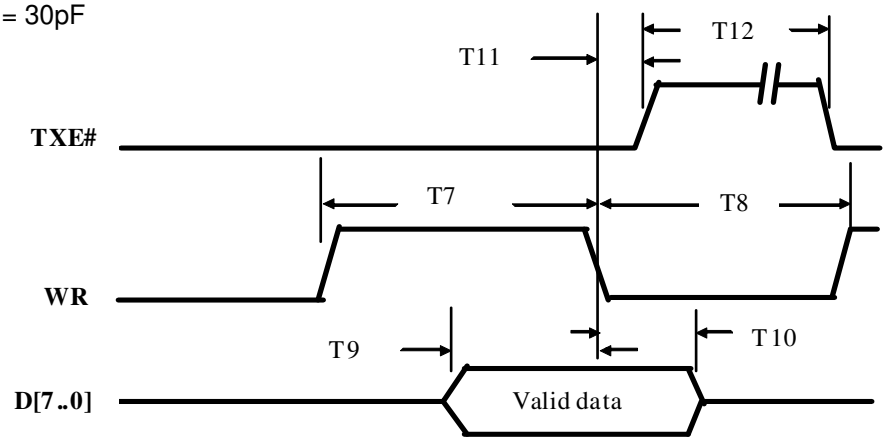
2.2 TIMING DIAGRAMS - 245 FIFO MODE

The following diagram details the FT2232H operation in 245 FIFO asynchronous mode. For detailed timing on the remaining modes refer to the FT2232H datasheet from FTDI.



TIME	DESCRIPTION	MIN	MAX	UNIT
T1	RD# Active Pulse Width	50	-	nS
T2	RD# to RD# Pre-Charge	T5 + T6	-	nS
T3	RD# Active to Valid Data*	20	50	nS
T4	Valid Data Hold Time from RD# Inactive*	0	-	nS
T5	RD# Inactive to RXF# output active	0	25	nS
T6	RXF# Inactive After RD Cycle	33	67	nS

*Load = 30pF



TIME	DESCRIPTION	MIN	MAX	UNIT
T7	WR Active Pulse Width	10	-	nS
T8	WR to WR Pre-Charge Time	50	-	nS
T9	Valid Data Setup to WR Falling Edge*	20	-	nS
T10	Valid Data Hold Time from WR Inactive*	10	-	nS
T11	WR Inactive to TXE#	10	25	nS
T12	TXE# Inactive After WR Cycle	49	84	nS

*Load = 30pF

3.0 APPLICATION NOTES

USB devices transfer data in packets. If data is to be sent from the PC, a packet is built up by the application program and is sent via the device driver to the USB scheduler. This scheduler adds a request to the list of tasks that the USB host controller will perform. This will typically take at least 1 millisecond to execute because it will not pick up the new request until the next USB frame (the frame period is 1 millisecond). There is, therefore, sizeable overhead (depending upon your required throughput) associated with moving data from the application to the USB device. If data is sent one byte at a time by an application, this will severely limit the overall throughput of the system.

It must be stressed that in order to achieve maximum throughput, application programs should send or receive data using buffers and not individual characters.

4.0 DRIVER SOFTWARE

FTDI's VCP (Virtual COM Port) USB driver files are provided royalty free on the condition that they are only used with designs incorporating an FTDI device (i.e. the FT2232H and DLP-2232H). The latest version of the drivers can be downloaded from either **www.dlpdesign.com** or **www.ftdichip.com**.

The CDM driver download file is a combined set of drivers for the Windows operating system and contains both the VCP and D2XX driver versions. To download, simply unzip the file to a folder on your PC. (The drivers can coexist on the same floppy disk or folder since the INF files determine which set of drivers to load for each operating-system version.) Once loaded, the VCP drivers will allow your application software—running on the host PC—to communicate with the DLP-2232H as though it were connected to a COM (RS-232) port.

In addition to VCP drivers, FTDI's D2XX direct drivers for Windows offer an alternative solution to the VCP drivers that allow application software to interface with the FT2232H device using a DLL instead of a Virtual COM Port. The architecture of the D2XX drivers consists of a Windows WDM driver that communicates with the FT2232H device via the Windows USB stack and a DLL that interfaces with the application software (written in VC++, C++ Builder, Delphi, VB, etc.) to the WDM driver.

The D2XX direct drivers add support for simultaneous access and control of multiple DLP-2232H devices. The extended open function (FT_OpenEx) allows the device to be opened either by its product description or serial number, both of which can be programmed to be unique. The list devices function (FT_ListDevices) allows the application software to determine which devices are currently available for use, again by either product description or serial number.

Download FTDI Application Notes AN_103, AN_104, and AN_119 for detailed instructions on how to install the drivers on Windows XP, Vista, and 7 platforms.

5.0 EEPROM WRITE UTILITY

The DLP-2232H has the option to accept manufacturer-specific information that is written into EEPROM memory. Parameters that can be programmed include the VID and the PID identifiers, the manufacturer's product string and a serial number.

MPROG is the EEPROM programming utility for the FT2232H device. You must install the latest release of the CDM drivers in order to run this application. If you have CDM drivers installed on the PC that is to perform the EEPROM write process, you can run MPROG and update the EEPROM contents with either mode (VCP or D2XX) active.

6.0 QUICK START GUIDE

This guide requires the use of a Windows XP/Vista/7 PC that is equipped with a USB port.

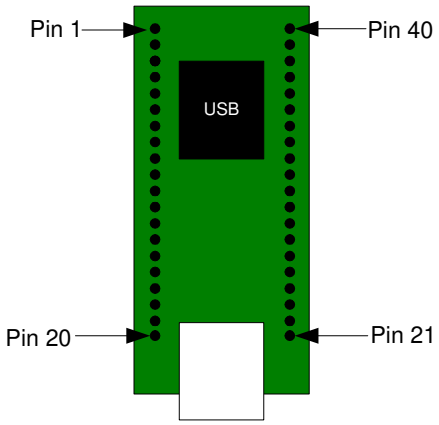
1. Configure mode select jumpers using the shunts provided. Refer to section 2.1 on page 5.

2. Download the latest CDM device drivers from either **www.dlpdesign.com** or **www.ftdichip.com**. Unzip the drivers into a folder on the hard drive.

3. Connect the DLP-2232H module to the PC via a USB 'A' to mini-B cable. This action initiates the loading of the USB drivers. When prompted, select the folder where the device drivers were stored in Step 1. Windows will then complete the installation of the device drivers for the DLP-2232H module. The next time the DLP-2232H module is attached, the host PC will immediately load the correct drivers without any prompting. Reboot the PC if prompted to do so.

At this point, the DLP-2232H is ready for use. Note that if the DLP-2232H is configured for 245 FIFO mode that it will appear non-responsive if data sent from the host PC is not read by an attached microcontroller, microprocessor, DSP, FPGA, ASIC, etc.

7.0 PIN LOCATIONS



Top View
(Interface Headers on bottom of PCB)

8.0 PIN USAGE EXAMPLES

The following tables highlight two possible configurations for the DLP-2232H module. There are numerous additional combinations available. For the complete DLP-2232H pin list refer to the pin descriptions in section 2.0.

CASE 1: Port A: 245 FIFO Synchronous, Port B 245 FIFO Asynchronous

PIN #	PORT A PARALLEL SYNC, PORT B PARALLEL ASYNC SIGNAL USAGE DESCRIPTION
1	**SIWUB** –The Port B Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.
2	**PORT B WR#** - When taken from a high to a low state, WR reads the 8 data lines and writes the byte into the FIFO's transmit buffer. Data written to the transmit buffer is sent to the host PC within the TX buffer timeout value (default 16mS) and placed in the buffer that was created when the USB port was opened.
3	**PORT B RD#** - When pulled low, RD# takes the 8 data lines from a high-impedance state to the current byte in the FIFO's buffer. Taking RD# high returns the data pins to a high- impedance state and prepares the next byte (if available) in the FIFO to be read.
4	**PORT B TXE#** - Transmit Buffer Empty: When high, do not write data into the FIFO. When low, data can be written into the FIFO by toggling WR. During reset this signal pin is tri-state. Data is latched into the FIFO on the falling edge of the WR pin.
5	**PORT B RXF#** - Receive Buffer Full : When low, at least 1 byte is present in the FIFO's receive buffer and is ready to be read with RD#. RXF# goes high when the receive buffer is empty. During reset this signal pin is tri-state. If the Remote Wakeup option is enabled in the internal EEPROM, during USB Suspend Mode (PWREN#=1) RXF# becomes an input. This can be used to wake up the USB host from Suspend Mode by strobing this pin low for a minimum of 20ms which will cause the device to request a resume on the USB bus.
6	**PORT B DB7** – Port B FIFO Data Bus Bit 7
7	**PORT B DB6** – Port B FIFO Data Bus Bit 6
8	**PORT B DB5** – Port B FIFO Data Bus Bit 5
9	**PORT B DB4** – Port B FIFO Data Bus Bit 4
10	**PORT B DB3** – Port B FIFO Data Bus Bit 3
11	**PORT B DB2** – Port B FIFO Data Bus Bit 2
12	**PORT B DB1** – Port B FIFO Data Bus Bit 1
13	**PORT B DB0** – Port B FIFO Data Bus Bit 0
14	**GROUND**
15	**GROUND**
19	**EXTVCC** - Use for applying main power (4.5 to 5.25 volts) to the module. Connect to PORTVCC if the module is to be powered by the USB port (typical configuration).
20	**PORTVCC** - Power from the USB port. Connect to EXTVCC if the module is to be powered by the USB port (typical configuration). 500mA is the maximum current available to the USB adapter and target electronics if the USB device is configured for high power.

22	**GROUND**
23	**GROUND**
26	**PORT A OE#** - Output enable: when low drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn around.
27	**PORT A CLKOUT** – 60 MHz Clock driven from the FTDI chip. All signals should be synchronized to this clock.
28	**SIWUA** –The Port A Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.
29	**PORT A WR#** - When taken from a high to a low state, WR reads the 8 data lines and writes the byte into the FIFO's transmit buffer. Data written to the transmit buffer is sent to the host PC within the TX buffer timeout value (default 16mS) and placed in the buffer that was created when the USB port was opened.
30	**PORT A RD#** - When pulled low, RD# takes the 8 data lines from a high-impedance state to the current byte in the FIFO's buffer. Taking RD# high returns the data pins to a high- impedance state and prepares the next byte (if available) in the FIFO to be read.
31	**PORT A TXE#** - Transmit Buffer Empty: When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state. Data is latched into the FIFO on the falling edge of the WR pin.
32	**PORT A RXF#** - Receive Buffer Full : When low, at least 1 byte is present in the FIFO's receive buffer and is ready to be read with RD#. RXF# goes high when the receive buffer is empty. During reset this signal pin is tri-state. If the Remote Wakeup option is enabled in the internal EEPROM, during USB Suspend Mode (PWREN#=1) RXF# becomes an input. This can be used to wake up the USB host from Suspend Mode by strobing this pin low for a minimum of 20ms which will cause the device to request a resume on the USB bus.
33	**PORT A DB7** – Port A FIFO Data Bus Bit 7
34	**PORT A DB6** – Port A FIFO Data Bus Bit 6
35	**PORT A DB5** – Port A FIFO Data Bus Bit 5
36	**PORT A DB4** – Port A FIFO Data Bus Bit 4
37	**PORT A DB3** – Port A FIFO Data Bus Bit 3
38	**PORT A DB2** – Port A FIFO Data Bus Bit 2
39	**PORT A DB1** – Port A FIFO Data Bus Bit 1
40	**PORT A DB0** – Port A FIFO Data Bus Bit 0

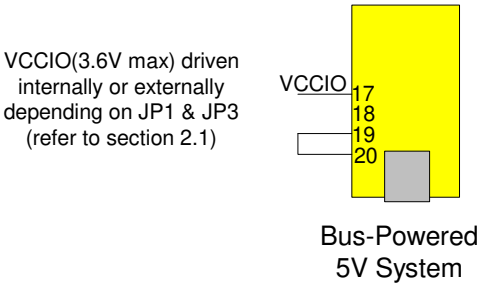
CASE 2: Port A: 232 Serial Asynchronous, Port B Fast Serial Interface

PIN #	PORT A 232 SERIAL SIGNAL USAGE DESCRIPTION
1	**SIWUB** –The Port B Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.
10	**FSCTS** – Fast serial Clear To Send output. Driven low to indicate that the FTDI chip is ready to send data.
11	**FSDO** – Fast serial data output
12	**FSCLK** – Fast serial clock input. Clock input to FTDI chip to clock data in or out.
13	**FSDI** – Fast serial data input
14	**GROUND**
15	**GROUND**
19	**EXTVCC** - Use for applying main power (4.5 to 5.25 volts) to the module. Connect to PORTVCC if the module is to be powered by the USB port (typical configuration).
20	**PORTVCC** - Power from the USB port. Connect to EXTVCC if the module is to be powered by the USB port (typical configuration). 500mA is the maximum current available to the USB adapter and target electronics if the USB device is configured for high power.
22	**GROUND**
23	**GROUND**
28	**RXLED** - Receive signaling output. Pulses low when receiving data via USB. This should be connected to an LED through a current limiting resistor.
29	**TXLED#** - Transmit signaling output. Pulses low when transmitting data via USB. This should be connected to an LED through a current limiting resistor.
32	**TXDEN -** (TTL level). For use with RS485 level converters.
33	**RI#** - Ring Indicator Control Input. When remote wake-up is enabled in the internal EEPROM taking RI# low (20ms active low pulse), this can be used to resume the PC USB host controller from Suspend.
34	**DCD#** - Data Carrier Detect Control Input
35	**DSR#** - Data Set Ready Control Input/Handshake Signal
36	**DTR#** - Data Terminal Ready Control Output/Handshake Signal
37	**CTS#** - Clear To Send Control Input/Handshake Signal
38	**RTS#** - Request to Send Control Output/Handshake Signal
39	**RXD** - Receiving Asynchronous Data Input
40	**TXD** - Transmit Asynchronous Data Output

9.0 DEVICE CONFIGURATION EXAMPLES

USB Bus-Powered and Self-Powered Configurations

Figure 1.



The figure above illustrates a typical USB bus-powered configuration. A USB bus-powered device gets its power from the USB bus.

Figure 2.

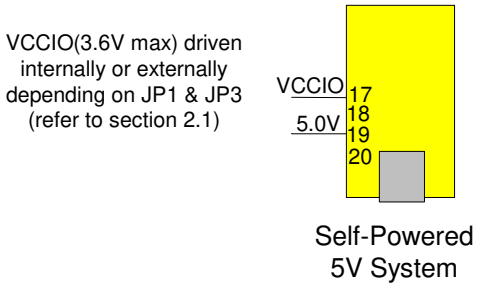


Figure 2 illustrates a typical USB self-powered configuration. A USB self-powered device gets its power from its own power supply and does not draw current from the USB bus.

Figure 3.

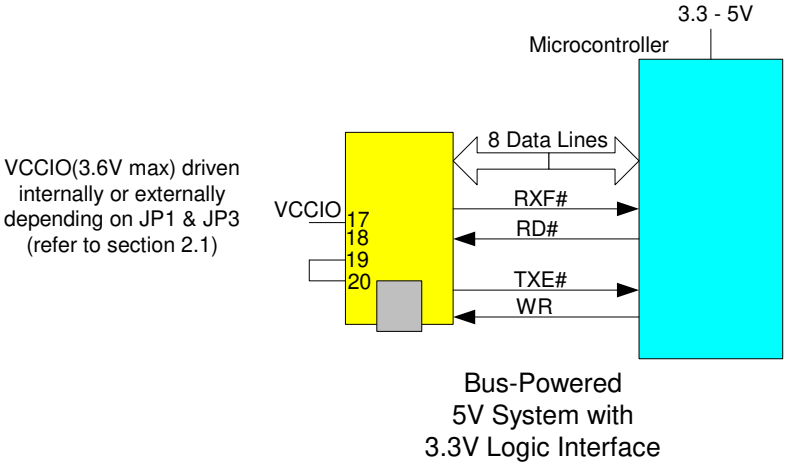


Figure 3 shows how to configure the DLP-2232H to interface with a microcontroller via the parallel 245 FIFO interface mode. In this example, the target electronics can operate at from 3.3 - 5 volts since the DLP-2232H interface I/O pins are 5 volt tolerant.

Figure 4.

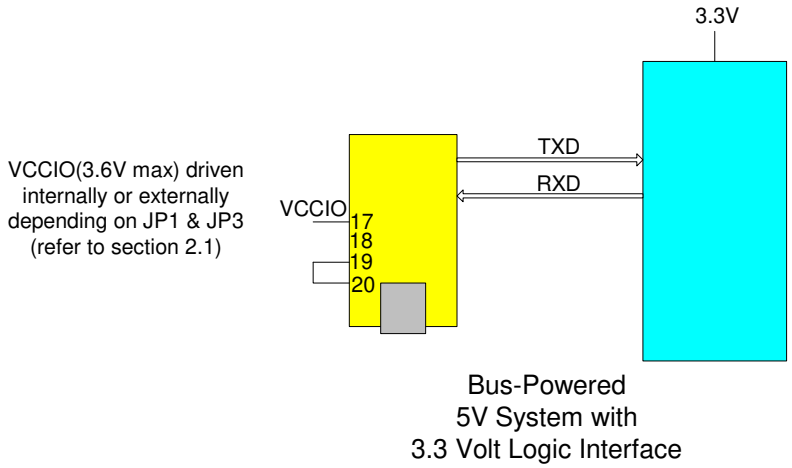


Figure 4 shows how to configure the DLP-2232H to interface with a 3.3V logic device via the ASYNC serial mode. In this example, the target electronics provide the 3.3 volts to power the microcontroller.

10.0 BUS-POWERED CIRCUIT WITH POWER CONTROL

USB bus-powered circuits need to be able to power down in USB Suspend Mode in order to meet the Suspend current requirement (including external logic). The DLP-2232H module provides a switched power output to accomplish this with no external components required:

Figure 4.

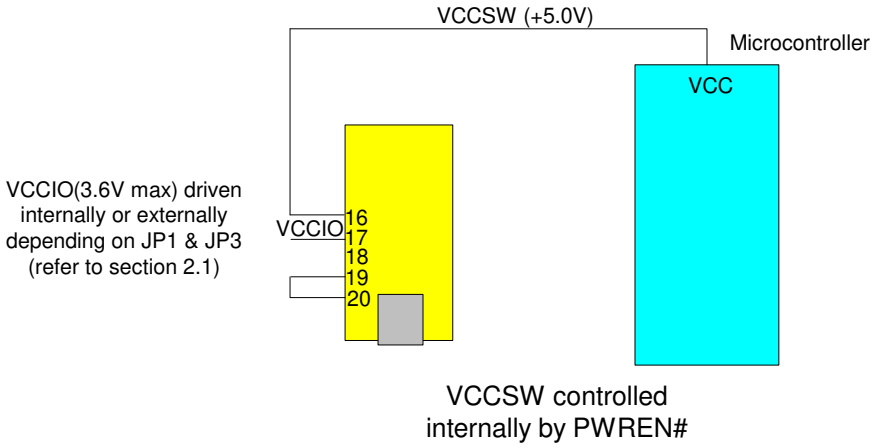
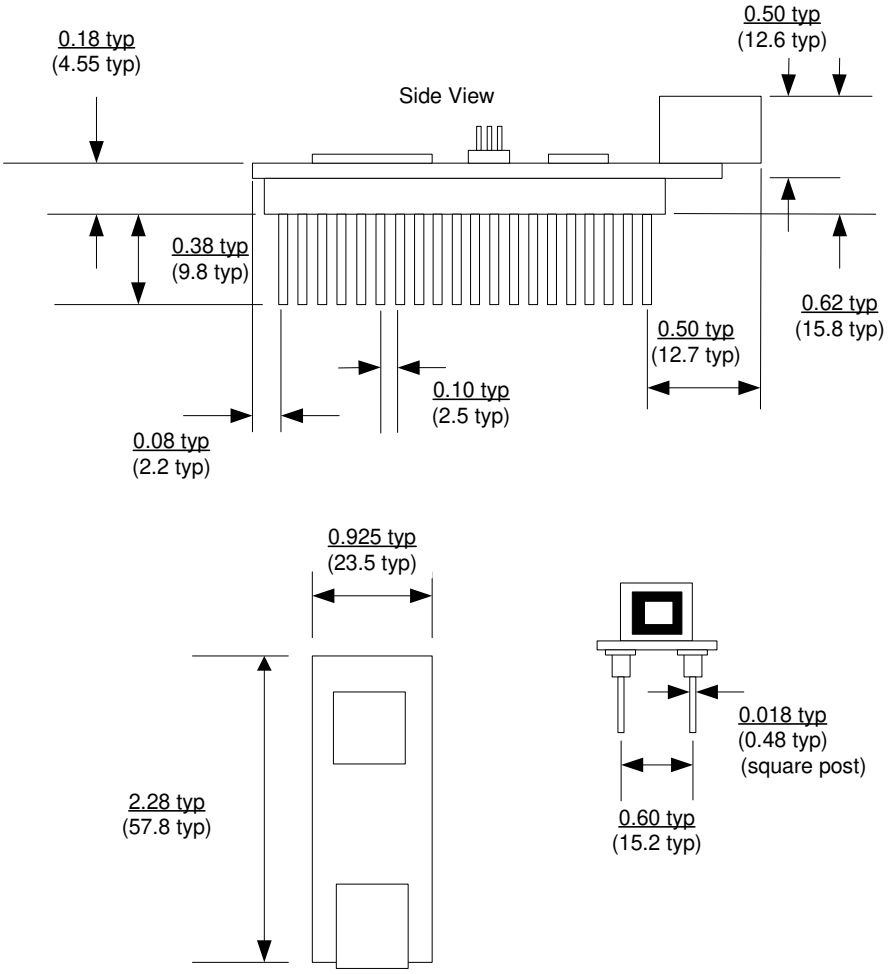


Figure 4 shows how to connect the switched +5.0V power to external logic circuits. The internal "soft-start" circuit on the DLP-2232H accommodates designs that draw more than 100mA at power up.

11.0 MECHANICAL DRAWINGS (PRELIMINARY) INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED



11.0 DISCLAIMER

This product and its documentation are supplied on an as-is basis, and no warranty as to their suitability for any particular purpose is either made or implied. DLP Design, Inc. will not accept any claim for damages whatsoever arising as a result of the use or failure of this product. Your statutory rights are not affected. This product or any variant of it is not intended for use in any

medical appliance, device or system in which the failure of the product might reasonably be expected to result in personal injury.

This document provides preliminary information that may be subject to change without notice.

12.0 CONTACT INFORMATION

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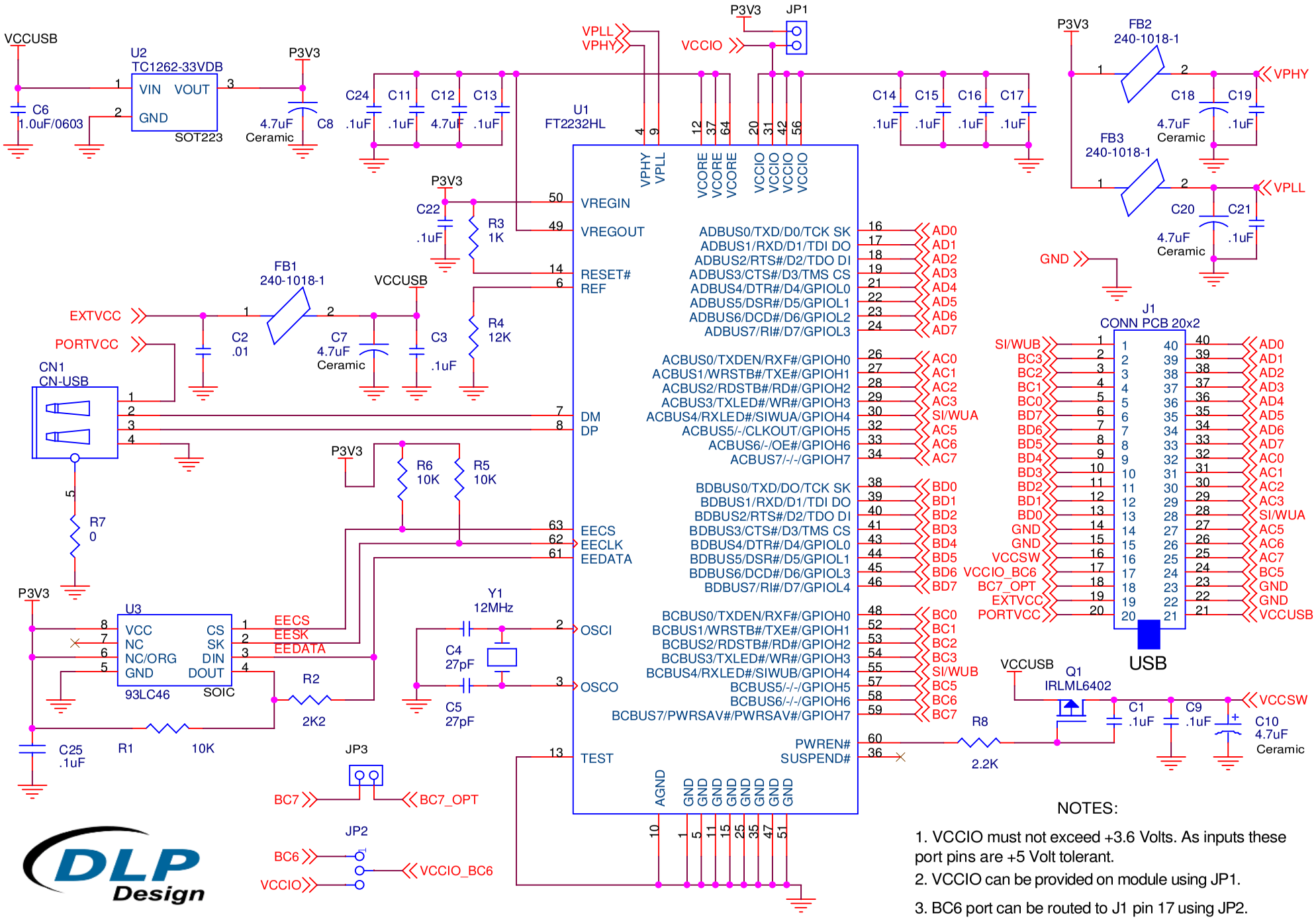
VCCUSB
U2
TC1262-33VDB
VIN
VOUT
GND
SOT223
C6
1.0uF/0603
4.7uF
Ceramic
C8
P3V3
VPLL
VPHY
VCCIO
JP1
C24
C11
C12
C13
.1uF
4.7uF
U1
FT2232HL
C14
C15
C16
C17
FB2
240-1018-1
FB3
240-1018-1
C18
C19
C20
C21
VPHY
VPLL
GND
C22
R3
1K
VREGIN
VREGOUT
RESET#
REF
FB1
240-1018-1
EXTVCC
PORTVCC
C2
.01
C7
4.7uF
Ceramic
C3
.1uF
R4
12K
CN1
CN-USB
DM
DP
R6
10K
R5
10K
R7
0
EECS
EECLK
EEDATA
U3
93LC46
SOIC
VCC
NC
NC/ORG
GND
CS
SK
DIN
DOUT
R2
2K2
Y1
12MHz
C4
27pF
C5
27pF
OSCI
OSCO
TEST
C25
.1uF
R1
10K
JP3
BC7
BC7_OPT
JP2
BC6
VCCIO
VCCIO_BC6
ADBUS0/TXD/D0/TCK SK
ADBUS1/RXD/D1/TDI DO
ADBUS2/RTS#/D2/TDO DI
ADBUS3/CTS#/D3/TMS CS
ADBUS4/DTR#/D4/GPIOL0
ADBUS5/DSR#/D5/GPIOL1
ADBUS6/DCD#/D6/GPIOL2
ADBUS7/RI#/D7/GPIOL3
ACBUS0/TXDEN/RXF#/GPIOH0
ACBUS1/WRSTB#/TXE#/GPIOH1
ACBUS2/RDSTB#/RD#/GPIOH2
ACBUS3/TXLED#/WR#/GPIOH3
ACBUS4/RXLED#/SIWUA/GPIOH4
ACBUS5/-/CLKOUT/GPIOH5
ACBUS6/-/OE#/GPIOH6
ACBUS7/-/-/GPIOH7
BDBUS0/TXD/DO/TCK SK
BDBUS1/RXD/D1/TDI DO
BDBUS2/RTS#/D2/TDO DI
BDBUS3/CTS#/D3/TMS CS
BDBUS4/DTR#/D4/GPIOL0
BDBUS5/DSR#/D5/GPIOL1
BDBUS6/DCD#/D6/GPIOL3
BDBUS7/RI#/D7/GPIOL4
BCBUS0/TXDEN/RXF#/GPIOH0
BCBUS1/WRSTB#/TXE#/GPIOH1
BCBUS2/RDSTB#/RD#/GPIOH2
BCBUS3/TXLED#/WR#/GPIOH3
BCBUS4/RXLED#/SIWUB/GPIOH4
BCBUS5/-/-/GPIOH5
BCBUS6/-/-/GPIOH6
BCBUS7/PWRSAV#/PWRSAV#/GPIOH7
PWREN#
SUSPEND#
R8
2.2K
Q1
IRLML6402
C1
.1uF
C9
.1uF
C10
4.7uF
Ceramic
VCCSW
J1
CONN PCB 20x2
USB
SI/WUB
BC3
BC2
BC1
BC0
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
GND
GND
VCCSW
VCCIO_BC6
BC7_OPT
EXTVCC
PORTVCC
VCCUSB
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AC0
AC1
AC2
AC3
SI/WUA
AC5
AC6
AC7
BC5
GND
GND
VCCUSB
NOTES:
1. VCCIO must not exceed +3.6 Volts. As inputs these port pins are +5 Volt tolerant.
2. VCCIO can be provided on module using JP1.
3. BC6 port can be routed to J1 pin 17 using JP2.
4. BC7 port can be routed to J1 pin 18 using JP3.
DLP Design
DLP-2232H v1.1
FT2232H pin definitions: PIN NAME/232/245/MPSSE