Universal Active ORing Controller IC

Description

The PI2001 *Cool-ORing™* solution is a universal high-speed Active ORing controller IC designed for use with N-channel MOSFETs in redundant power system architectures. The PI2001 *Cool-ORing* controller enables an extremely low power loss solution with fast dynamic response to fault conditions, critical for high availability systems. The PI2001 controls single or parallel MOSFETs to address Active ORing applications protecting against power source failures. The PI2001 can be used in either high-side or low-side Active ORing applications and a master/slave feature allows the paralleling of IC/MOSFET chipsets for high current Active ORing.

The gate drive output turns the MOSFET on in normal steady state operation, while achieving high-speed turn-off during input power source fault conditions, that cause reverse current flow, with auto-reset once the fault clears. The MOSFET drain-to-source voltage is monitored to detect normal forward, excessive forward, light load and reverse current flow. The PI2001 provides an active low fault flag output to the system during excessive forward current, reverse current, light load, over-voltage, under-voltage and over-temperature fault conditions. There is an internal shunt regulator at the VC input for high voltage applications and the under-voltage and over-voltage thresholds are programmable via external resistor dividers.

Features

- Fast Dynamic Response to Power Source failures, with 160ns reverse current turn-off delay time
- 4A gate discharge current
- Accurate MOSFET drain-to-source voltage sensing to indicate system level fault conditions
- Programmable under & over-voltage detection
- Over temperature fault detection
- Adjustable reverse current blanking timer
- 100V for 100ms operation in low side applications
- Master/Slave I/O for paralleling (TDFN only)
- Active low fault flag output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- Low & High-side Active ORing
- High current Active ORing

Package Information

The PI2001 is offered in the following packages:

- 10 Lead 3mm x 3mm TDFN package
- 8 Lead SOIC package

Typical Applications:

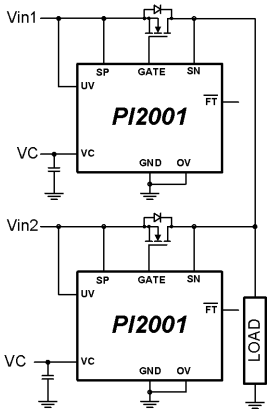


Figure 1a: PI2001 High Side Active ORing

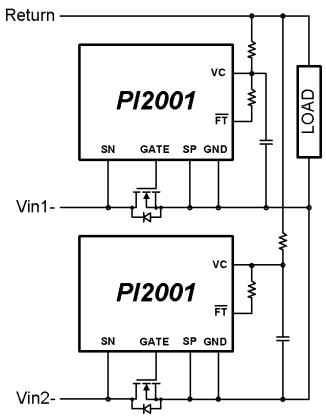
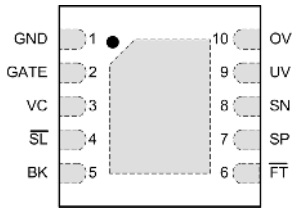


Figure 1b: PI2001 Low Side Active ORing

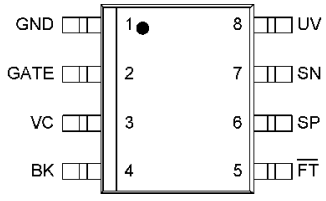
Pin Description

Pin Name	Pin Number		Description
	10 Lead TDFN	8 Lead SOIC	
GND	1	1	**Ground:** This pin is ground for the gate driver and control circuitry.
GATE	2	2	**Gate Drive Output:** This pin drives the gate of the external N-channel MOSFET. Under normal operating conditions, the GATE pin pulls high to 9.5V (typ) with respect to the SP pin. The controller turns the gate off during a reverse current fault that exceeds the reverse voltage threshold.
VC	3	3	**Controller Input Supply:** This pin is the supply pin for the control circuitry and gate driver. Connect a 1µF capacitor between VC pin and the GND pin. Voltage on this pin is limited to 15.5V by an internal shunt regulator. For high voltage auxiliary supply applications connect a shunt resistor between VC and the auxiliary supply.
$\overline{SL}$	4	n/a	**Slave Input-Output:** This pin is used for paralleling multiple PI2001 solutions in high power applications. When the PI2001 is configured as the Master, this pin functions as an output capable of driving up to 10 $\overline{SL}$ pins of slaved PI2001 devices. It serves as an input when the PI2001 is configured in slave mode.
BK	5	4	**Blanking Timer Input-Output:** Connect a resistor from BK to GND to set the blanking time for the Reverse Comparator function. To configure the controller in slave mode, connect BK to VC. To configure the controller in master mode with the fastest turn-off response, connect BK directly to GND.
$\overline{FT}$	6	5	**Fault State Output:** This open collector pin pulls low when a fault occurs. Fault logic inputs are VC Under-Voltage, Input Under-Voltage, Input Over-Voltage, Forward Over-Current, light load, reverse current, and Over-Temperature. Leave this pin open if unused.
SP	7	6	**Positive Sense Input & Clamp:** Connect SP pin to the Source pin of the external N-channel MOSFET. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
SN	8	7	**Negative Sense Input & Clamp:** Connect SN to the Drain pin of the external N-channel MOSFET. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
UV	9	8	**Input Under-Voltage Input:** The UV pin is used to detect an input source under-voltage condition in ground referenced applications. When the UV pin voltage drops below the UV threshold, the $\overline{FT}$ pin pulls low indicating a fault condition. The input voltage UV threshold is programmable through an external resistor divider. Connect UV to VC to disable this function.
OV	10	n/a	**Input Over-Voltage Input:** The OV pin is used to detect an input source over-voltage condition in ground referenced applications. When the OV pin voltage crosses the OV threshold, the $\overline{FT}$ pin pulls low indicating a fault condition. The input voltage OV threshold is programmable through an external resistor divider. Connect OV to GND to disable this function.

Package Pin-Outs



10 Lead TDFN (3mm x 3mm)
Top view



8 Lead SOIC (5mm x 6mm)
Top view

Absolute Maximum Ratings

VC	-0.3V to 17.3V / 40mA
SP, OV, $\overline{SL}$	-0.3V to 8.0V / 10mA
UV, BK, $\overline{FT}$	-0.3V to 17.3V / 10mA
GATE	-0.3V to 17.3V / 5A
SN (Continuous)	-0.3V to 80V / 10mA
SN (100ms Pulse)	100V / 10mA
GND	-0.3V / 5A peak
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to Over Temperature Fault (T_{FT})
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{GATE} = 4nF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range (3)	V_{VC-GND}	4.5		13.2	V	No VC limiting Resistors
Quiescent Current	I_{VC}		3.7	4.2	mA	Normal Operating Condition, No Faults
VC Clamp Voltage	V_{VC-CLM}	15	15.5	16	V	I_{VC}=10mA
VC Clamp Shunt Resistance	R_{VC}			7.5	Ω	Delta I_{VC}=10mA
VC Under-Voltage Rising Threshold	V_{VCUVR}		4.3	4.5	V	
VC Under-Voltage Falling Threshold	V_{VCUVF}	4.0	4.15		V	
VC Under-Voltage Hysteresis	$V_{VCUV-HS}$		150		mV	
FAULT						
Under-Voltage Rising Threshold	V_{UVR}		500	540	mV	
Under-Voltage Falling Threshold	V_{UVF}	440	475		mV	
Under-Voltage Threshold Hysteresis	V_{UV-HS}		25		mV	
Under-Voltage Bias Current	I_{UV}	-1		1	µA	
Over-Voltage Rising Threshold	V_{OVR}		500	540	mV	
Over-Voltage Falling Threshold	V_{OVF}	440	475		mV	
Over-Voltage Threshold Hysteresis	V_{OV-HS}		25		mV	
Over-Voltage Bias Current	I_{OV}	-1		1	µA	
Fault Output Low Voltage	V_{FTL}		0.2	0.5	V	I_{FT}=2mA, VC>3.5V
Fault Output High Leakage Current	I_{FT-LC}			10	µA	V_{FT}=14V
Fault Delay Time	t_{FT-DEL}	20	40	60	µs	Includes output glitch filter

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{GATE} = 4nF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
FAULT (Continued)						
Over Temperature Fault (1)	T_{FT}		160		°C	
Over Temperature Fault Hysteresis(1)	T_{FT-HS}		-10		°C	
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-0.1		5.5	V	SP to GND & SN to GND
Differential Operating Input Voltage	V_{SP-SN}	-50		125	mV	SP-SN
SP Input Bias Current	I_{SP}	-50	-37		µA	SP=SN=1.25V
SN Input Bias Current	I_{SN}		3.5	8	µA	SP=SN=1.25V
SN Voltage	V_{SN}			80	V	I_{SN} ≤ 7mA,SP=0V, I_{VC} = 10mA
Reverse Comparator Off Threshold	V_{RVS-TH}	-10	-6	-2	mV	V_{CM} = 3.3V
Reverse Comparator Hysteresis	V_{RVS-HS}	2		5	mV	V_{CM} = 3.3V
Reverse Fault to Gate Turn-off Delay Time	t_{RVS-MS}		160	220	ns	V_{SP-SN} = ± 50mV step to 90% of V_G max, V_{BK}=0 (minimum blanking)
Reverse Fault to Gate Turn-off Delay Time	t_{RVS-SL}		430	600	ns	V_{SP-SN} = ± 50mV step to 90% of V_G max, V_{BK}= V_{VC} (maximum blanking)
Forward Comparator On Threshold	V_{FWD-TH}	2	6	9	mV	V_{CM} = 3.3V
Forward Comparator Hysteresis	V_{FWD-HS}	-5		-2	mV	V_{CM} = 3.3V
Forward Over-Current Comparator Threshold	V_{OC-TH}	60	66	70	mV	V_{CM} = 3.3V
Forward Over-Current Comparator Hysteresis	V_{OC-HS}	-8		-4	mV	V_{CM} = 3.3V
GATE DRIVER						
Gate Source Current	I_{G-SC}		-1.0	-0.4	mA	V_G = 1V, Normal Operating Conditions, No Faults
Pull Down Peak Current(1)	I_{G-PD}	1.5	4.0		A	
Pull-down Gate Resistance (1)	R_{G-PD}		0.3		Ω	V_G = 1.5V @ 25°C
AC Gate Pull-down Voltage(1)	V_{G-PD}			0.2	V	
DC Gate Pull-down Voltage to SP(1)	V_{G-PD}		1.1		V	I_G=100mA, in reverse fault
Gate Voltage @ VC UVLO	V_{G-UVLO}		0.7	1	V	I_G =10µA,1.5V<VC<3.5V
Gate to SP Clamp Voltage	V_{G-CLMP}	8.5	9.5	10.5	V	I_G = 100µA
Gate Voltage High	V_G	VC-0.5V	VC-0.25V		V	VC- V_{SP} < V_{G-CLMP}
Gate Fault Condition Clear(1)	V_{G-CL}		77		%	
Gate Fall Time	t_{G-F}		10	15	ns	90% to 10% of V_G max.

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{GATE} = 4nF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
SLAVE						
Slave Source Current	I_{SL}		-60	-25	µA	V_{SL} = 1V, Normal Operating Conditions, No Faults
Slave Output Voltage High	V_{SL-Hi}		4.3	5.5	V	Normal Operating Conditions, No Faults
Slave Output Voltage Low	V_{SL-Lo}		0.2	0.5	V	I_{SL}=4mA
Slave Hold-off Voltage at VC UVLO	V_{SL-UV}		0.7	1	V	I_{SL}=5µA,1.5V<VC<3.5V
Slave Threshold	V_{SL-TH}		1.75	2	V	
Slave Fall Time	t_{SL-FL}		15	25	ns	90% to 50% of V_{SL} max V_{BK} =0
Slave to Gate Delay Time After Reverse Current Fault ***Master Mode***	t_{SL-G}		20	30	ns	50%of V_{SL} to 90% of $V_G$max; V_{BK} =0
Slave to Gate Delay Time ***Slave Mode***	t_{SL-G}		100	130	ns	50%of V_{SL} to 90% of $V_G$max; V_{BK}=VC
BLANK						
Blank Source Current	I_{BK}	-60	-45	-30	µA	V_{BK}=0V
Blank Output Voltage	V_{BK}		0.77	0.9	V	I_{BK}=5µA Connected to GND
Blank Slave Mode Threshold	V_{BK-TH}	1.2	1.45	1.7	V	

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Refer to the *Auxiliary Power Supply* section in the *Application Information* for details on the VC requirement to meet the MOSFET Vgs requirement.

Functional Description:

The PI2001 *Cool-ORing* controller IC is designed to drive single or paralleled N-channel MOSFETs in Active ORing applications. The PI2001 used with an external MOSFET can function as an ideal ORing diode in the high or low side of a redundant power system, significantly reducing power dissipation and eliminating the need for heatsinking.

An N-channel MOSFET in the conduction path offers extremely low on-resistance resulting in a dramatic reduction of power dissipation versus the performance of a diode used in conventional ORing applications due to its high forward voltage drop. This can allow for the elimination of complex heat sinking and other thermal management requirements. Due to the inherent characteristics of the MOSFET, while the gate remains enhanced above the gate threshold voltage it will allow current to flow in the forward and reverse direction. Ideal ORing applications do not allow for reverse current flow, so the controller has to be capable of very fast and accurate detection of reverse current caused by input power source failures, and turn off the gate of the MOSFET as quickly as possible. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus. During forward over-current conditions caused by load faults, the controller maintains gate drive to the MOSFET to keep power dissipation as low as possible, otherwise the inherent body diode of the MOSFET would conduct, which has higher effective forward drop. Conventional ORing solutions using diodes offer no protection against forward over-current conditions. During the forward over-current condition, the PI2001 will provide an active-low fault flag to the system via the $\overline{FT}$ pin. The fault flag is also issued during the reverse current condition, light load conditions, VC Under-Voltage, Input Under-Voltage and Over-Voltage and Over-Temperature conditions.

Differential Amplifier:

The PI2001 integrates a high-speed low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to three comparators: Reverse comparator, Forward comparator, and Forward over-current comparator.

Reverse Comparator: RVS

The reverse comparator is the most critical comparator. It looks for negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will enable the BK current source to charge an internal 2pF capacitor. The blanking timer provides noise filtering for typical switching power conversion that might cause premature reverse current detection. Once the voltage across the capacitor reaches the timer threshold voltage (1.25V) the gate will be discharged by a 4Apk current. The shortest blanking time is 50ns when BK is connected to ground. The Blanking time programmed by the BK pin will be added to the controller delay time. The Electrical Specifications in the *DIFFERENTIAL AMPLIFIER AND COMPARATOR* section for Reverse Fault to Slave Low Delay Time "$t_{RVS\text{-}MS}$ or $t_{RVS\text{-}SL}$" is the controller delay time plus the blanking time.

Reverse Blanking Timer: BK

Connecting an external resistor (R_{BK}) between the BK pin and ground will increase the blanking time as shown in Figure 2.

Where: $R_{BK} \leq 200K\Omega$

If BK is connected to VC for slave mode operation, then the blanking time will be about 320ns typically, and total delay time will be 430ns.

The reverse comparator has 3mV of hysteresis referenced to SP-SN.

If the conditions are met for a reverse current fault, then the active-low fault flag output will also indicate a fault to the system after the 40µs fault delay time.

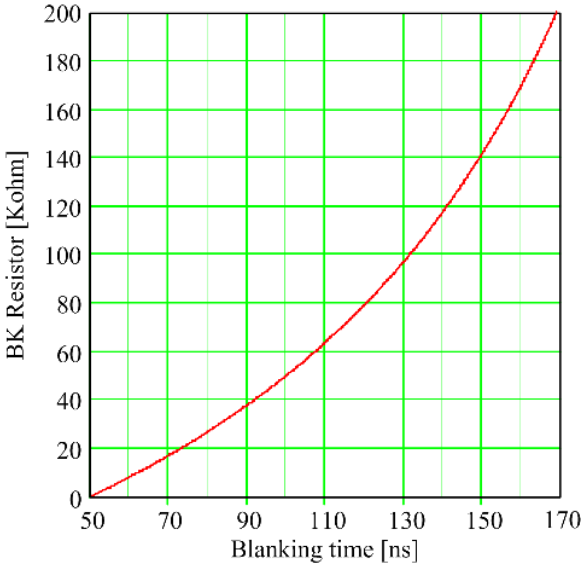


Figure 2: Blanking time vs. BK resistor value

Forward Voltage Comparator: FWD

The FWD comparator detects when a forward current condition exists and SP is 6mV(typical) positive with respect to SN. When SP-SN is less than 6mV, the FWD comparator will assert the Fault flag to report a fault condition indicative of a light load or "load not present" condition or possible shorted MOSFET.

Forward Over Current Comparator: FOC

The FOC comparator indicates an excessive forward current condition when SP is 66mV(typical) higher than SN. When the GATE output voltage is greater than 77% of the regulated gate voltage and SP-SN is higher than 66mV, the PI2001 will initiate a fault condition via the $\overline{FT}$ pin.

Slave:
In high current applications multiple parallel MOSFETs may be needed for a single ORing function. Driving multiple MOSFETs with one controller will increase the loading on the GATE pin and the gate connection parasitic thereby impacting the reverse turn-off response.

The Slave function synchronizes multiple controllers so that one, or more, of the paralleled MOSFETs will have its own local driving source. In this configuration, one controller will be designated as the master and it will control the response of the slaved controllers.

When the controller is configured in "Master Mode", by connecting the BK to ground, the $\overline{SL}$ will be an output having the same signal characteristics as the GATE signal. In this configuration, the $\overline{SL}$ output is capable of driving up to ten controllers, configured in "Slave Mode", through their corresponding $\overline{SL}$ pins. Logic high for the $\overline{SL}$ pin is limited to 5.5V (max).

When the BK pin is tied to VC, the controller is configured in "Slave Mode" and the $\overline{SL}$ pin becomes an input. The Gate driver section and reverse current section are the only active circuits in the slave controller while the master performs the diagnostics and gate drive control.

VC and Internal Voltage Regulator:
The PI2001 has a separate input (VC) that provides power to the control circuitry and the gate driver. An internal regulator clamps the VC voltage to 15.5V.

For high side applications, the VC input should be high enough above the bus voltage to properly enhance the external N-channel MOSFET. In a low side drive application VC may be tied to the bus voltage through a resistor.

The internal regulator circuit has a comparator to monitor VC voltage and initiates a FAULT condition when VC is lower than the VC Under-Voltage Threshold.

UV:
The Under-Voltage (UV) input trip point can be programmed through an external resistor divider to monitor the input voltage. The UV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low when UV falls below the Under-Voltage Falling Threshold. The GATE pin does not respond to a UV fault. If the PI2001 is configured in a floating application, where the GND pin is connected to the input voltage, the UV pin cannot detect the input voltage. In this case, the UV pin should be disabled by connecting it to the VC pin.

OV:
The Over Voltage (OV) input trip point can be programmed through an external resistor divider to monitor the input voltage. The OV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low when OV rises above the Over-Voltage Rising Threshold. The GATE pin does not respond to an OV fault. If the PI2001 is configured in a floating application, where the GND pin is connected to the input voltage, the OV pin cannot detect the input voltage. In this case, the OV pin should be disabled by connecting it to the GND pin.

Over-Temperature Detection:
The internal Over-Temperature block monitors the junction temperature of the controller. The Over-Temperature threshold is set to 160°C with -10°C of hysteresis. When the controller temperature exceeds this threshold, the Over-Temperature circuit initiates a fault condition and pulls the $\overline{FT}$ pin low. By maintaining proper thermal matching between the controller and the power MOSFET, this function can be used to protect the ORing device from thermal runaway conditions. The GATE pin does not respond to an Over-Temperature fault.

Gate Driver:
The gate driver (GATE) output is configured to drive an external N-channel MOSFET. In the high state, the gate driver applies a 1mA current source to the MOSFET gate and regulates the voltage to 9.5V typical ($V_{G\text{-}CLMP}$) above the SP pin voltage (V_{SP}) when the VC input voltage is higher than V_{SP} plus $V_{G\text{-}CLMP}$. Otherwise the gate voltage (V_G) to V_{SP} will

be {V_{G-SP} = VC - V_{SP} – 0.5V}. Note that VC is the controller internal regulated voltage.

When a reverse current fault is initiated, the gate driver pulls the GATE pin low and discharges the FET gate with 4Apeak capability.

When the input source voltage is applied and before the MOSFET is fully enhanced, a voltage greater than the Forward Over Current (FOC) Threshold will be present across the MOSFET. To avoid an erroneous FOC detection, a VGS detector blanks the FOC and FWD comparators from initiating a fault, until the GATE pin reaches 77% of V_{G-CLMP}. If VC is too low to establish the Gate Clamp condition the reference for detection is 77% of {VC-V(SP) - 0.25V}.

Fault:
The fault circuit output is an open collector with 40µs delay to prevent any false triggering. The $\overline{FT}$ pin will be pulled low when any of the following faults occur:

- Reverse current
- Forward Over-Current
- Forward Low Current
- Over-Temperature
- Input Under-Voltage
- Input Over-Voltage
- VC pin Under-Voltage

The only fault condition that initiates gate turn-off of the MOSFET (as well as a fault flag signal) is when the reverse current fault conditions are met. All other fault conditions issue only a fault flag signal via the $\overline{FT}$ pin, but do not affect the gate of the MOSFET. The $\overline{FT}$ pin serves as an indicator that a fault condition may be present. This information can be reported to a Host to signal that some system level maintenance may be required.

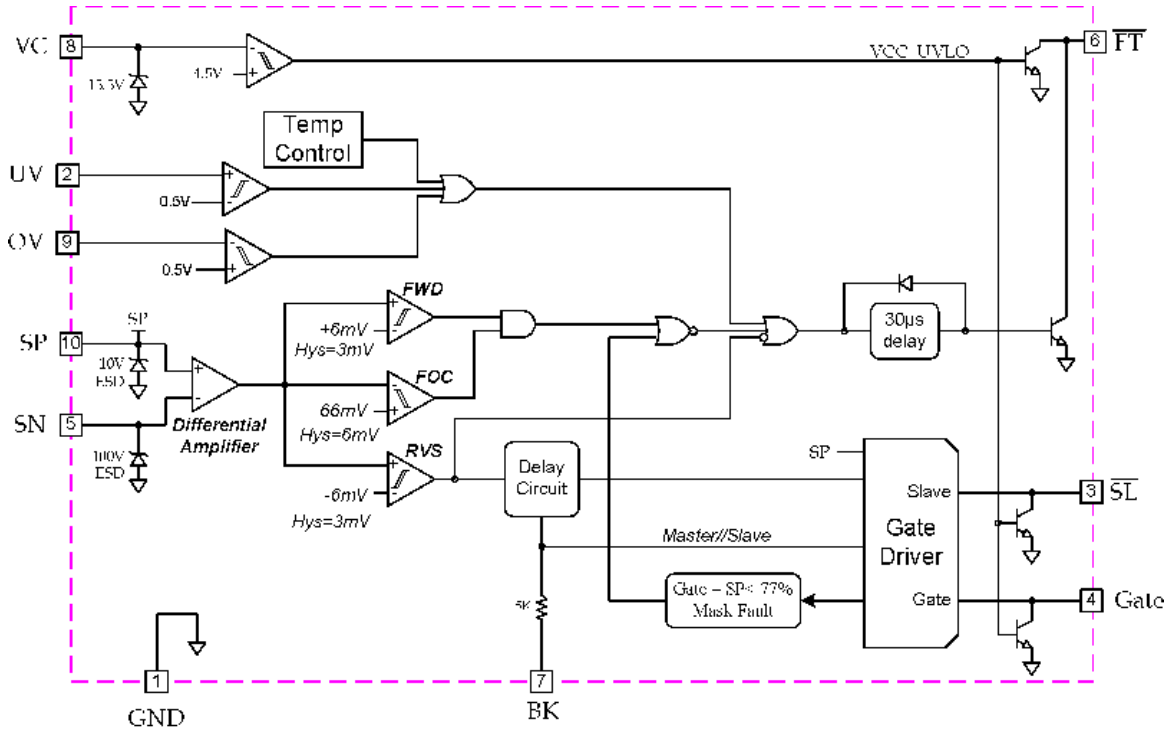


Figure 3: PI2001 Controller Internal Block Diagram (10 Lead TDFN package pin out shown)

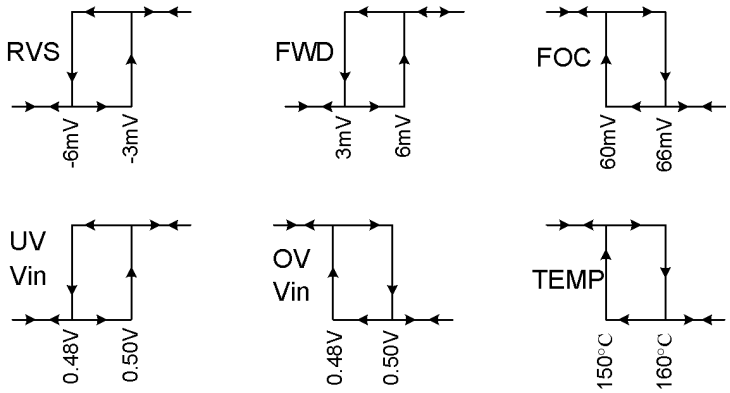


Figure 4: Comparator hysteresis, values are for reference only, please refer to the electrical specifications

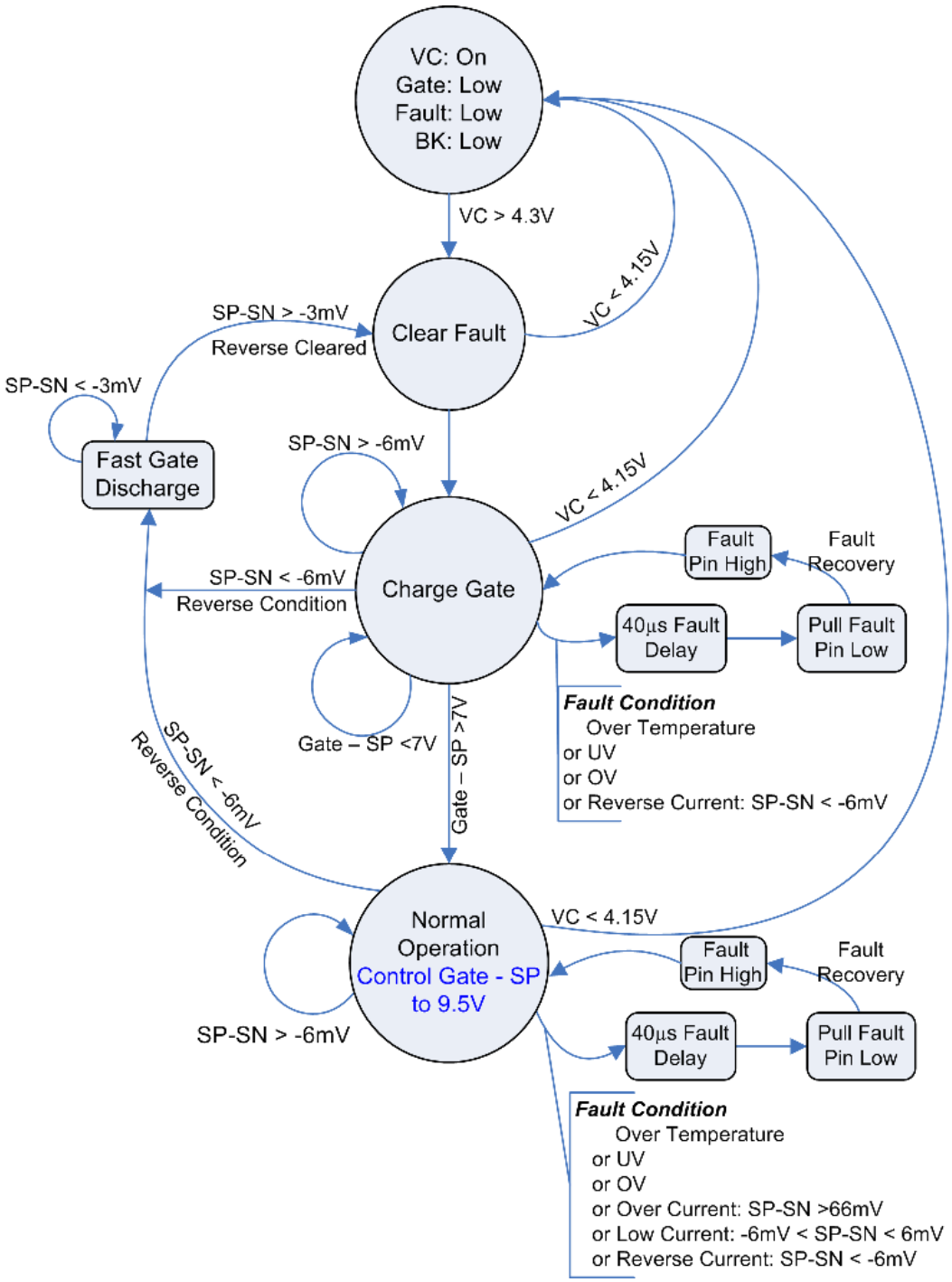


Figure 5: PI2001 State Diagram (Configured in Master Mode)

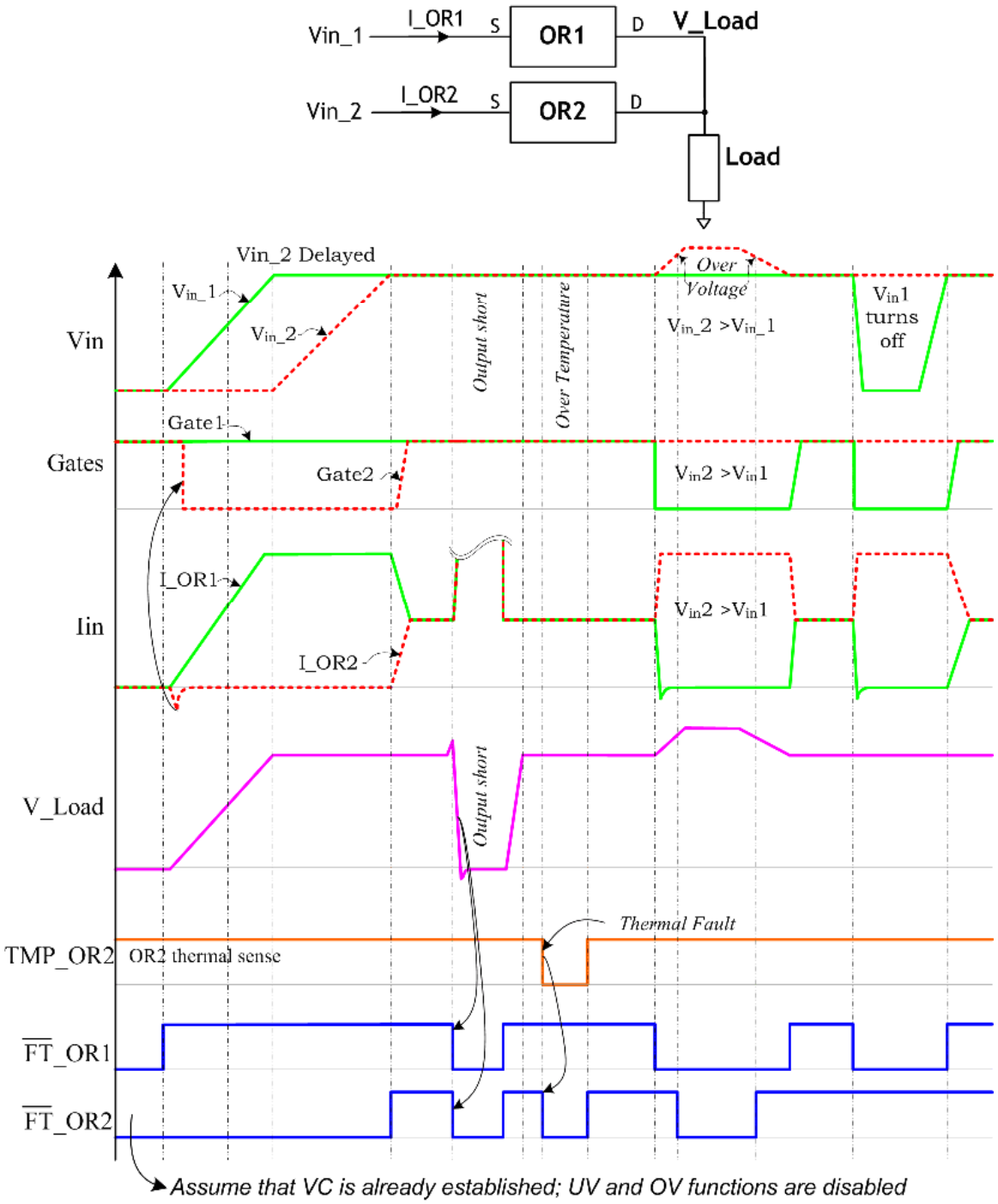


Figure 6: Timing diagram for two PI2001 controllers in an Active ORing application

Typical Characteristics:

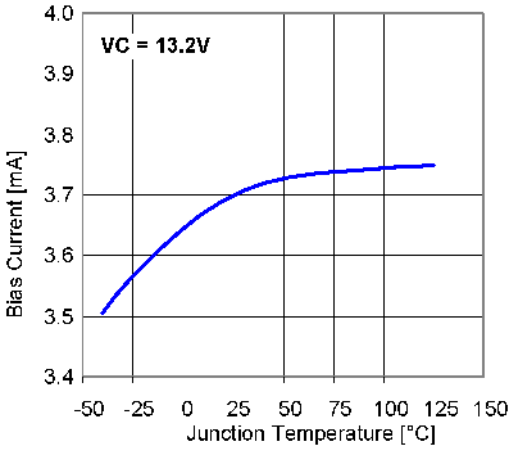


Figure 7: Controller bias current vs. temperature

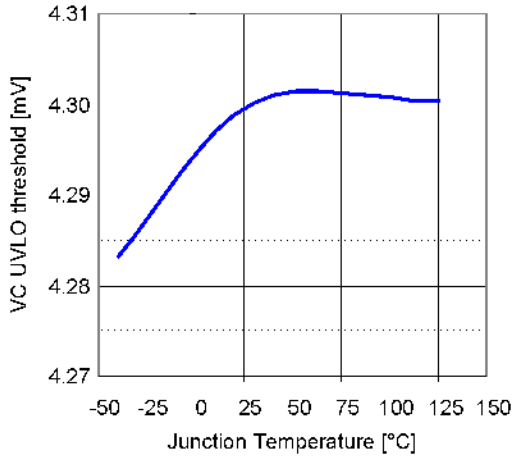


Figure 8: VC UVLO threshold vs. temperature

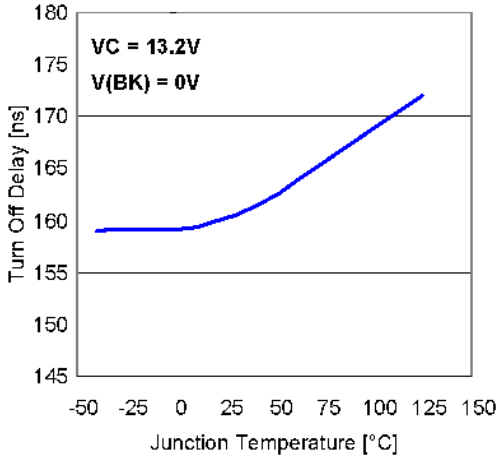


Figure 9: Reverse condition gate turn-off delay time vs. temperature.

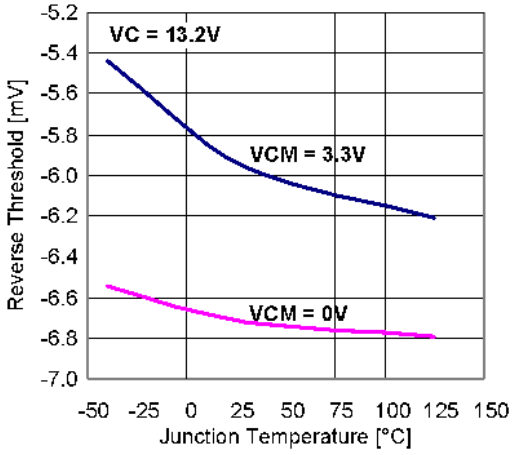


Figure 10: Reverse comparator threshold vs. temperature. ***VCM:*** *Common Mode Voltage*.

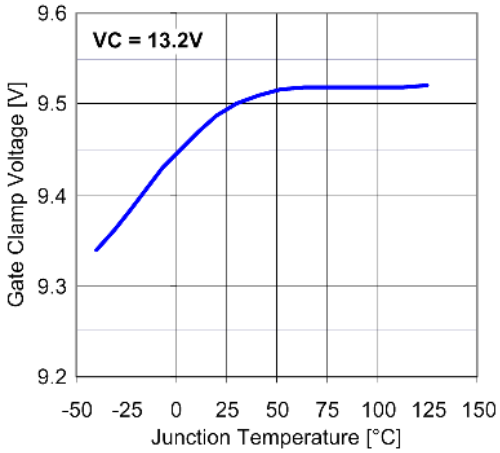


Figure 11: Gate to SP clamp voltage vs. temperature.

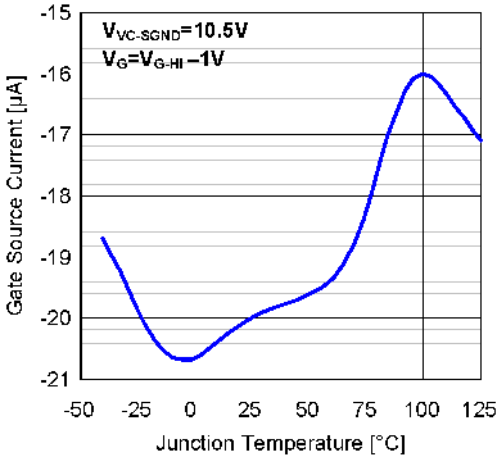


Figure 12: Gate source current vs. temperature

Application Information:

The PI2001 is designed to replace ORing diodes in high current redundant power architectures. Replacing a traditional diode with a PI2001 controller IC and a low on-state resistance N-channel MOSFET will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features. This section describes in detail the procedure to follow when designing with the PI2001 Active ORing controller and N-Channel MOSFETs. Three different Active ORing design examples are presented.

Fault Indication:

$\overline{FT}$ output pin is an open collector and should be pulled up to the logic voltage or to the controller VC via a resistor (10KΩ)

Blanking Timer:

Connect the blanking timer pin (BK) to GND to program the device for the fastest reverse comparator response time of 160ns typical. To increase the blanking time, connect the BK pin to GND via a resistor to avoid the fault response to short reverse current pulses. Refer to Figure 2 in the reverse comparator functional description for resistor values versus the reverse blanking time.

Auxiliary Power Supply (Vaux):

Vaux is an independent power source required to supply power to the PI2001 VC input. The Vaux voltage should be higher than Vin (redundant power source output voltage) by the required gate-to-source voltage (Vgs) to fully enhance the MOSFET, plus 0.5V maximum gate to VC headroom (VHD_{VC-G})

Vaux = Vin + Vgs + VHD_{VC-G}

Where, VHD_{VC-G} is defined as the 0.5V maximum drop from VC in the *Gate Voltage High* (V_G) specification in the Gate Driver section of the Electrical Specification.

For example, if the bus voltage is 3.3V and the MOSFET requires 5.0V of Vgs to fully enhance the MOSFET, then Vaux should be at least 3.3V + 5.0V + 0.5V = 8.8V.

If Vaux is higher than 15V then a bias resistor (Rbias) is required, and should be connected between the PI2001 VC pin and Vaux. The resistor is selected based on the input voltage range.

Minimize the resistor value for low Vaux voltage levels to avoid a voltage drop that may reduce the VC voltage lower than required to drive the gate of the MOSFET. Select the value of Rbias using the following equations:

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}}$$

Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias}$$

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage (15V).

Where:

$Vaux_{\min}$: Vaux minimum voltage

$Vaux_{\max}$: Vaux maximum voltage

VC_{Clamp} : Controller clamp voltage, 15.5V

$IC_{\max}$: Controller maximum bias current (4.2mA)

Slave:

For a high current application where one MOSFET can not handle the total load current, multiple MOSFETs can be paralleled and driven by a single PI2001 controller. Special care has to be taken when multiple MOSFET gates are driven from one gate driver output. The gate driver output capability will be divided by the number of MOSFET gates connected to it and will slow the MOSFET response to a reverse fault. To avoid MOSFET slow response the PI2001 can be configured in a master / slave configuration providing localized gate drive to each paralleled MOSFET.

The PI2001 slave feature allows the user to parallel multiple PI2001s and configure one unit as the master and the rest in slave mode. The slave ($\overline{SL}$) pin of the master unit will act as an output driving the units configured in slave mode. The $\overline{SL}$ pins of the slaved units will act as inputs under the control of the master. In this configuration each MOSFET will have its own localized gate driver which is synchronized by the master controller, thereby improving the response to a reverse current condition. One master controller is capable of driving up to 10 slave inputs.

N-Channel MOSFET Selection:

There are several factors that affect the MOSFET selection including cost, on-state resistance (Rds(on)), current rating, power dissipation, thermal conductivity, drain-to-source breakdown voltage (BVdss), gate-to-source voltage rating (Vgs), and gate threshold voltage ($Vgs_{(TH)}$).

The first step is to select suitable MOSFETs based on the BVdss requirement for the application. The BVdss voltage rating should be higher than the applied Vin voltage plus expected transient voltages. Stray parasitic inductance in the circuit can also contribute to significant transient voltage conditions, particularly

during MOSFET turn-off after a reverse current fault has been detected. In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFET. Depending on the output impedance of the system, the reverse current may reach over 60A in some conditions before the MOSFET is turned off. Such high current conditions will store energy even in a small parasitic element. For example, a 1nH parasitic inductance with 60A reverse current will store 1.8µJ (½Li^2). When the MOSFET is turned off, the stored energy will be released and will produce high negative voltage ringing at the MOSFET source. This event will create a high voltage difference across the drain and source of the MOSFET.

The MOSFET current rating and maximum power dissipation are closely related. Generally the lower the MOSFET Rds(on), the higher the current capability and the lower the resultant power dissipation. This leads to reduced thermal management overhead, but will ultimately be higher cost compared to higher Rds(on) parts. It is important to understand the primary design goal objectives for the application in order to effectively trade off the performance of one MOSFET versus another.

Power dissipation in active ORing circuits is derived from the total source current and the on-state resistance of the selected MOSFET.

MOSFET power dissipation:

$$Pd_{MOSFET} = Is^2 * Rds(on)$$

Where :
Is : Source Current
Rds(on) : MOSFET on-state resistance

Note:
In the calculation use Rds(on) at maximum MOSFET temperature because Rds(on) is temperature dependent. Refer to the normalized Rds(on) curves in the MOSFET manufacturers datasheet. Some MOSFET Rds(on) values may increase by 50% at 125°C compared to values at 25°C.

The Junction Temperature rise is a function of power dissipation and thermal resistance.

$$Trise_{MOSFET} = Rth_{JA} * Pd_{MOSFET} = Rth_{JA} * Is^2 * Rds(on),$$

Where:
Rth_{JA}: Junction-to-Ambient thermal resistance

Rds(on) and PI2001 sensing:

The PI2001 senses the MOSFET source-to-drain voltage drop via the SP and SN pins to determine the status of the current through the MOSFET. When the MOSFET is fully enhanced, its source-to-drain voltage is equal to the MOSFET on-state resistance multiplied by the source current, V_{SD} = Rds(on)*Is. The reverse current threshold is set for -6mV and when the differential voltage between the SP & SN pins is less than -6mV, i.e. SP-SN≤-6mV, the PI2001 detects a reverse current fault condition and pulls the MOSFET gate pin low, thus turning off the MOSFET and preventing further reverse current. The reverse current fault protection disconnects the power source fault condition from the redundant bus, and allows the system to keep running.

The GATE pin output voltage is clamped to 10.5V maximum with respect to the SP pin, which should be tied to the MOSFET source pin, to support any MOSFET with a Vgs rating of ±12V or greater. A Vgs rating ≥12V is very common for industry standard N-Channel MOSFETs.

OV/UV resistor selection:
The UV and OV comparator inputs are used to monitor the input voltage and will indicate a fault condition when this voltage is out of range. The UV and OV pins can be configured in two different ways, either with a divider on each pin, or with a three-resistor divider to the same node, enabling the elimination of one resistor. Under-Voltage is monitored by the UV pin input and Over-Voltage is monitored with the OV pin input.

The Fault pin ($\overline{FT}$) will indicate a fault (active low) when the UV pin is below the threshold or when the OV pin is above the threshold. The UV and OV thresholds are 0.50V typ with 25mV hysteresis and their input current is less than ±1µA. It is important to consider the maximum current that will flow in the resistor divider and maximum error due to UV and OV input current. Set the resistor current to 100µA or higher to maintain 1% accuracy for UV and OV due to the bias current.

The three-resistor voltage divider configuration for both UV and OV to monitor the same voltage node is shown in figure 13:

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

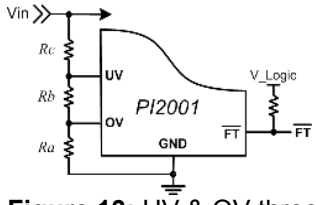


Figure 13: UV & OV three-resistor divider configuration.

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

Set Ra value based on system allowable current I_{Ra} $Ra = \frac{V(OV_{TH})}{I_{Ra}}$

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right)$$

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V_{TH}} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

$V(OV_{TH})$: OV threshold voltage

V(UV) : UV voltage

I_{Ra} : Ra current.

Alternatively, a two-resistor voltage divider configuration can be used and is shown in (Figure 14).

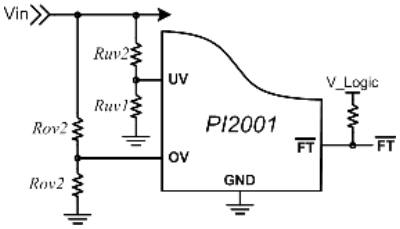


Figure 14: Two-resistor divider configuration

The UV resistor voltage divider can be obtained from the following equations:

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{UV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:

$V(UV_{TH})$: UV threshold voltage

I_{RUV} : $R1_{UV}$ current

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{OV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right)$$

Where:

$V(OV_{TH})$: OV threshold voltage

I_{ROV} : $R1_{OV}$ current

Typical application Example 1:

Requirement:
Redundant Bus Voltage = 3.3V
Load Current = 15A (assume through each redundant path)
Maximum Ambient Temperature = 75°C
Auxiliary Voltage = 12V (11V to 13V)

Solution:

1. A single PI2001 with suitable external MOSFET for each redundant 3.3V power source should be used, configured as shown in the circuit schematic in figure 15
2. **Select a suitable N-Channel MOSFET:** Most industry standard MOSFETs have a Vgs rating of +/-12V or higher. Select an N-Channel MOSFET with a low Rds(on) which is capable of supporting the full load current with some margin, so a MOSFET capable of at least 18A in steady state is reasonable. An exemplary MOSFET having these characteristic is FDS6162N7 from Fairchild.

From FDS6162N7 datasheet:

- N-Channel MOSFET
- V_{DS}= 20V
- I_D = 23A continuous drain current
- $V_{GS(MAX)}$= ± 12V
- $R_{\theta JA}$= 40°C/W
- $R_{DS(on)}$=2.9mΩ typical at I_D=23A, V_{GS}≥4.5V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{2.9m\Omega} = -2.07A$$

Power dissipation:
Rds(on) is 3.5mΩ maximum at 25°C & 4.5Vgs and will increase as the temperature increases. Add 25°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (75°C + 25°C) Rds(on) will increase by 28%.

$Rds(on) = 3.5m\Omega * 1.28 = 4.48m\Omega$ maximum at 100°C

$Trise = Rth_{JA} * Is^2 * Rds(on)$

Maximum Junction temperature

$$T_{J\max} = T_A + Trise$$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.48m\Omega\right) = 115°C$$

Recalculate based on calculated Junction temperature, 115°C.

At 115°C Rds(on) will increase by 32%.

$$Rds(on) = 3.5m\Omega * 1.32 = 4.62m\Omega$$

$$T_{J\max} = 75°C + \left(\frac{40°C}{W} * (15A)^2 * 4.62m\Omega\right) = 116.5°C$$

3. **Vaux:** Make sure Vaux voltage is higher than Vin (power source output) by the voltage required to fully enhance the MOSFET. Minimum required Vaux = Vin + Vgs + 0.5V = 3.3V + 4.5V + 0.5V = 8.3V. Since 8.3V is less than the 11V minimum Aux supply voltage, there is sufficient voltage available to drive the gate of the MOSFET.

4. **SP and SN pins:** Connect the SP pin to the MOSFET source pin and the SN pin to the MOSFET drain pin.

5. **BK pin:** Connect the BK pin to the GND pin to achieve the minimum reverse current response time.

6. $\overline{SL}$ **pin:** Not required, so leave floating.

7. $\overline{FT}$ **pin**: Connect to the logic input and to the logic power supply via a 10KΩ resistor.

8. **Program UV and OV to monitor input voltage:** Program UV at 3.0V and OV at 3.6V

   Use the three-resistor divider configuration:

   $I_{Ra} = 200\mu A$

$$Ra = \frac{V(UV_{TH})}{I_{Ra}} = \frac{500mV}{200\mu A} = 2.5k\Omega$$ or 2.49kΩ 1%

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right) = 2.49k\Omega\left(\frac{3.6V}{3.0V} - 1\right) = 498\Omega$$

or 499Ω 1%

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

$$= (2.49k\Omega + 499\Omega)\left(\frac{3.0V}{500mV} - 1\right) = 14.95k\Omega$$

or 15kΩ 1%

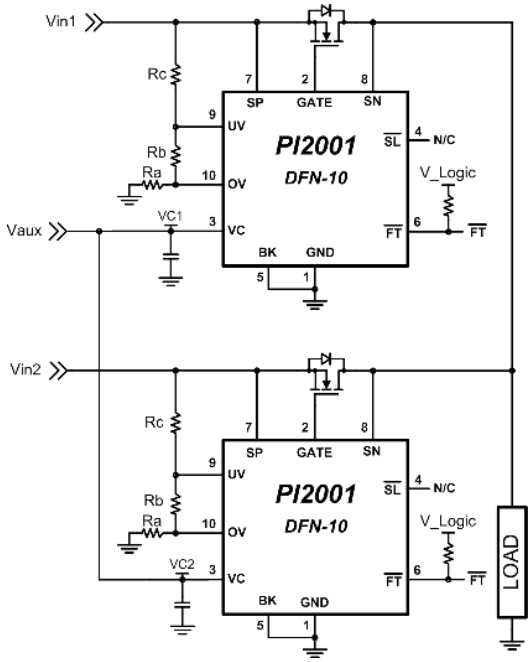


Figure 15: PI2001 in high side Active ORing configuration

Typical application Example 2:

Requirement:
Redundant Bus Voltage = 12V (±10%, 10.8V to 13.2V)
Load Current = 10A (assume through each redundant path)
Maximum Ambient Temperature = 75°C
Auxiliary Voltage = 24V±10% (21.6V to 26.4V) referenced to GND

Solution:

1. A single PI2001 with suitable external MOSFET for each redundant 12V power source should be used, configured in a high-side floating configuration as shown in the circuit schematic in Figure 16. The controller is floated on Vin by connecting the controller ground pin to the input voltage Vin.
2. **Select a suitable N-Channel MOSFET:** Select an N-Channel MOSFET with a voltage rating higher than the 12V input plus any expected transient voltages, with a low Rds(on) that is capable of supporting full load current with margin. For instance, a 30V rated MOSFET with 20A current capability is suitable. An exemplary MOSFET having these characteristic is FDS8812NZ from Fairchild.

From FDS8812NZ datasheet:

- N-Channel MOSFET
- V_{DS}= 30V
- I_D = 20A continuous drain current
- $V_{GS(MAX)}$= ± 20V
- $R_{\theta JA}$= 50°C/W
- $R_{DS(on)}$=3.2mΩ typical at I_D=10A, V_{GS}=8V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{3.2m\Omega} = -1.87A$$

Power dissipation:
Rds(on) is 4.2mΩ maximum at 25°C & 8Vgs and will increase as the temperature increases. Add 25°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (75°C + 25°C) Rds(on) will increase by 28%.

$Rds(on) = 4.2m\Omega * 1.28 = 5.37m\Omega$ maximum at 100°C

$Trise = Rth_{JA} * Is^2 * Rds(on)$

Maximum Junction temperature

$T_{J\max} = T_A + Trise$

$$T_{J\max} = 75°C + \left(\frac{50°C}{W} * (10A)^2 * 5.37m\Omega\right) = 102°C$$

3. **Vaux:** Make sure Vaux voltage is higher than Vin (power source output) by the voltage required to fully enhance the MOSFET. In this case there is sufficient headroom on the Vaux supply to increase the Vgs level for a reduction in power dissipation due to lower Rds(on). If the MOSFET requires 8.0V to achieve lower power dissipation, then

   Vaux = Vin + Vgs + 0.5V = 12V + 8.0V + 0.5V = 20.5V.

   When Vin is off (0V), PI2001 GND pin is at 0V and Vaux is higher than the VC clamp voltage. A bias resistor (Rbias) is needed in series with the VC pin.

Rbias value:

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}} = \frac{21.6V - 15.5V}{4.2mA} = 1.45K\Omega$$

or 1.30KΩ

Rbias resistor power dissipation rating:
Note: Use minimum value for VC_{Clamp} voltage to calculate worst condition power dissipation.

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias} = \frac{(26.4V - 15.0V)^2}{1.30K\Omega} = 100mW$$

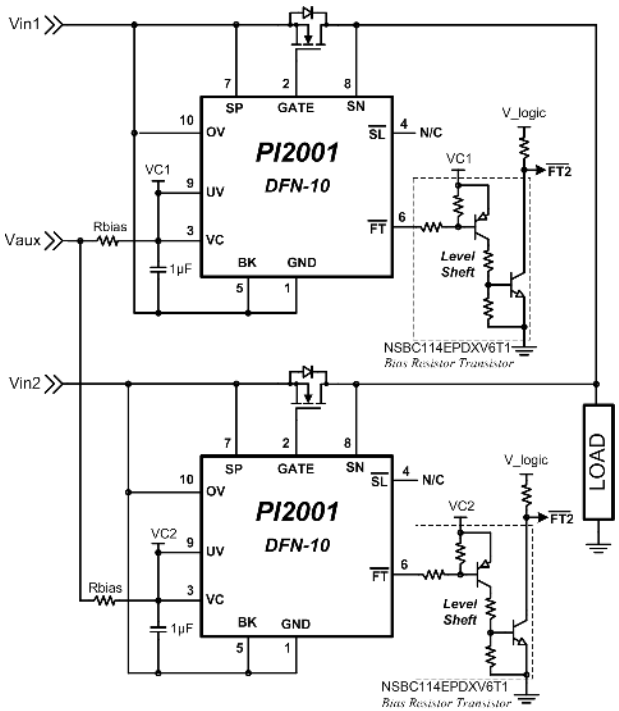


Figure 16: PI2001 in floating application: example 2

4. **SP and SN pins:** Since the PI2001 controller GND pin is connected to the input (Vin) which is also the MOSFET source, connect the SP pin directly to the PI2001 GND pin to reduce the parasitic between the SP pin and the GND pin to avoid negative voltages on the SP pin with respect to GND pin. Connect the SN pin to the MOSFET drain pin.

5. **BK pin:** Connect the BK pin to the GND pin to achieve the minimum reverse current response time.

6. $\overline{SL}$ **pin:** Not required, so leave floating.

7. $\overline{FT}$ **pin**: The $\overline{FT}$ pin output is referenced to the PI2001 GND pin which is connected to Vin. A level shift circuit can be added to make the $\overline{FT}$ pin output referenced to the system ground. The recommended level shift circuit is shown in Figure 16, The level shift circuit uses a Dual Bias Resistor Transistor circuit which is available as a small device that contains two transistors and their bias resistors, part number NSBC114EPDXV6T1.

8. **UV and OV inputs:** In floating applications these pins can not be used to monitor Vin. Connect UV to the VC pin and OV to the GND pin to disable their function.

Typical application Example 3:
Requirement:
Redundant Bus Voltage = -48V (-36V to -60V, 100V for 100ms transient)
Load Current = 5A load (assume through each redundant path)
Maximum Ambient Temperature = 60°C

Solution:

1. A single PI2001 with a suitable MOSFET for each redundant -48V power source should be used and configured as shown in figure 17. The VC is biased from the return line through a bias resistor.

2. **Select a suitable N-Channel MOSFET:** Select the N-Channel MOSFET with voltage rating higher than the input voltage, Vin, plus any expected transient voltages, with a low Rds(on) that is capable of supporting the full load current with margin. For instance, a 100V rated MOSFET with 10A current capability is suitable. An exemplary MOSFET having these characteristic is Si4486EY from Vishay Siliconix.

From Si4486EY datasheet:

- N-Channel MOSFET
- V_{DS}= 100V
- I_D = 23A continuous drain current at 125°C
- $V_{GS(MAX)} = \pm 20V$
- $R_{\theta JA}$= 50°C/W
- $R_{DS(on)}$=20mΩ typical at V_{GS}=10V, T_J=25°C

Reverse current threshold is:

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{20m\Omega} = -300mA$$

Power dissipation:
Rds(on) is 25mΩ maximum at 25°C & 10Vgs and will increase as the temperature increases. Add 40°C to maximum ambient temperature to compensate for the temperature rise due to power dissipation. At 100°C (60°C + 40°C) Rds(on) will increase by 63%.

$Rds(on) = 25m\Omega * 1.63 = 41m\Omega$ maximum at 100°C

Maximum Junction temperature

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 41m\Omega\right) = 111°C$$

Recalculate based on calculated Junction temperature, 115°C.

At 115°C Rds(on) will increase by 72%.

$Rds(on) = 25m\Omega * 1.72 = 43m\Omega$ maximum at 115°C

$$T_{J\max} = 60°C + \left(\frac{50°C}{W} * (5.0A)^2 * 43m\Omega\right) = 113°C$$

Vaux: Connect each controller to the return path with a separate bias resistor, Rbias.

To reduce $Rbias$ power dissipation, VC_{clamp} is selected at 13V which is less than the actual PI2001 clamp voltage (15V typical). 13V is higher than PI2001 maximum gate clamp voltage (10.5V).

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}} = \frac{36V - 13V}{4.2mA} = 5.48K\Omega$$

or 5.49KΩ

$Rbias$ maximum power dissipation is at maximum input voltage and minimum clamp voltage

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clampMIN})^2}{Rbias} = \frac{(60V - 15V)^2}{5.49K\Omega} = 369mW$$

3. **SP and SN pins:** Connect the SP pin to the MOSFET source and controller GND pin, and connect the SN pin to Vin- and the drain of the MOSFET.
4. **BK pin:** Connect the BK pin to the GND pin to achieve the minimum reverse current response time.
5. $\overline{SL}$ **pin:** Not required, so leave floating.
6. $\overline{FT}$ **pin**: Connect the $\overline{FT}$ pin to logic input and to the logic power supply or to the VC pin via a resistor.
7. **UV and OV inputs:** sensing input voltages Vin1- and Vin2- separately in this application the resistor divider has to be connected between Vin1-/Vin2- and return. The PI2001 controller GND pins are referenced to the load side, if the resistor dividers are connected between Return and Vin1-/Vin2- it will produce an error due the voltage drop across the MOSFET and will expose the OV and UV controller inputs to a high current in case of an input short circuit and will damage the controller.

   The voltage across the load can be monitored by one controller or both. The following shows the resistor voltage divider configuration using the three-resistor divider configuration:

Set $I_{Ra} = 100\mu A$

$$Ra = \frac{V(UV_{TH})}{I_{Ra}} = \frac{500mV}{100\mu A} = 5k\Omega$$ or 4.99kΩ 1%

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right) = 4.99k\Omega\left(\frac{65V}{34V} - 1\right) = 4.55K\Omega$$

Or Rb=4.53KΩ

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

$$Rc = (4.99k\Omega + 4.53K\Omega)\left(\frac{34V}{500mV} - 1\right) = 638k\Omega$$

or 634kΩ 1%

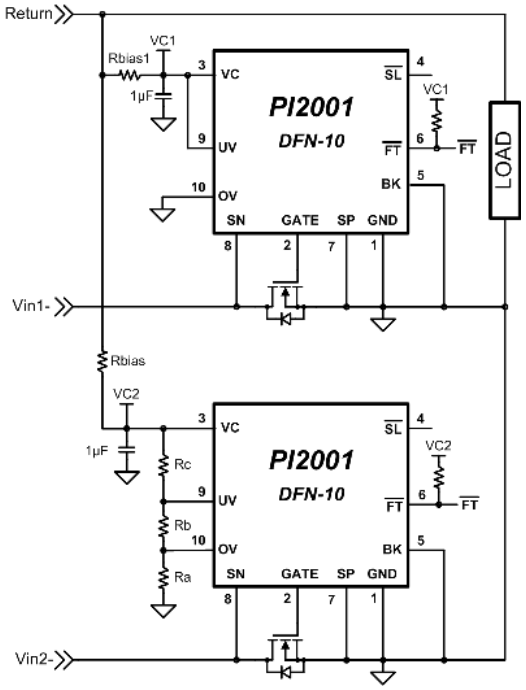


Figure 17: PI2001 in low side -48V application

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for a TDFN PI2001 and SO-8/PowerPak MOSFET is shown in Figure 18:

- It is best to connect the gate of the MOSFET to the GATE pin of the controller with a short and wide trace.
- The GND pin of the controller carries high peak current and it should be returned to the ground plane through a low impedance path.
- Connections from the SP and SN pins to the MOSFET source and drain pins respectively should be as short as possible
- The VC bypass capacitor should be located as close as possible to the VC and GND pins. Place the PI2001 and VC bypass capacitor on the same layer of the board. The VC pin and C_{VC} PCB trace should not contain any vias.
- Connect all MOSFET source pins together with a wide trace to reduce trace parasitics and to accommodate the high current input. Similarly, connect all MOSFET Drain pins together with a wide trace to accommodate the high current output.
- Connect the power source very close to the MOSFET source connection to reduce the effects of stray parasitics. If a short trace is not possible, connect C4 (typically 1µF) as shown in figure 18.

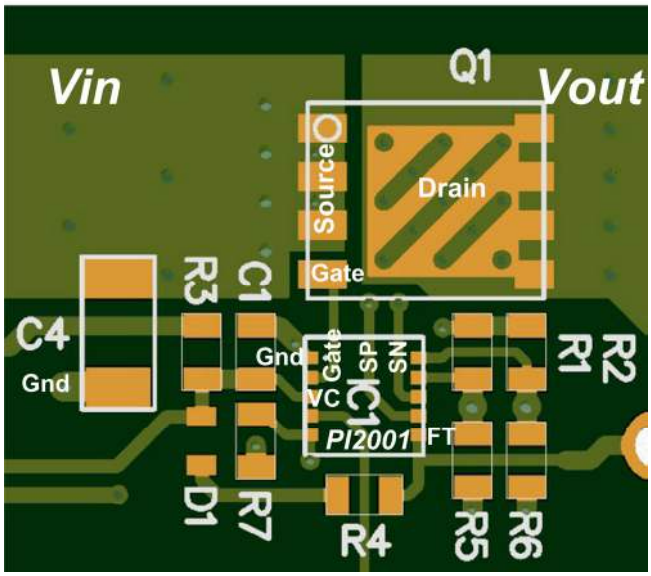
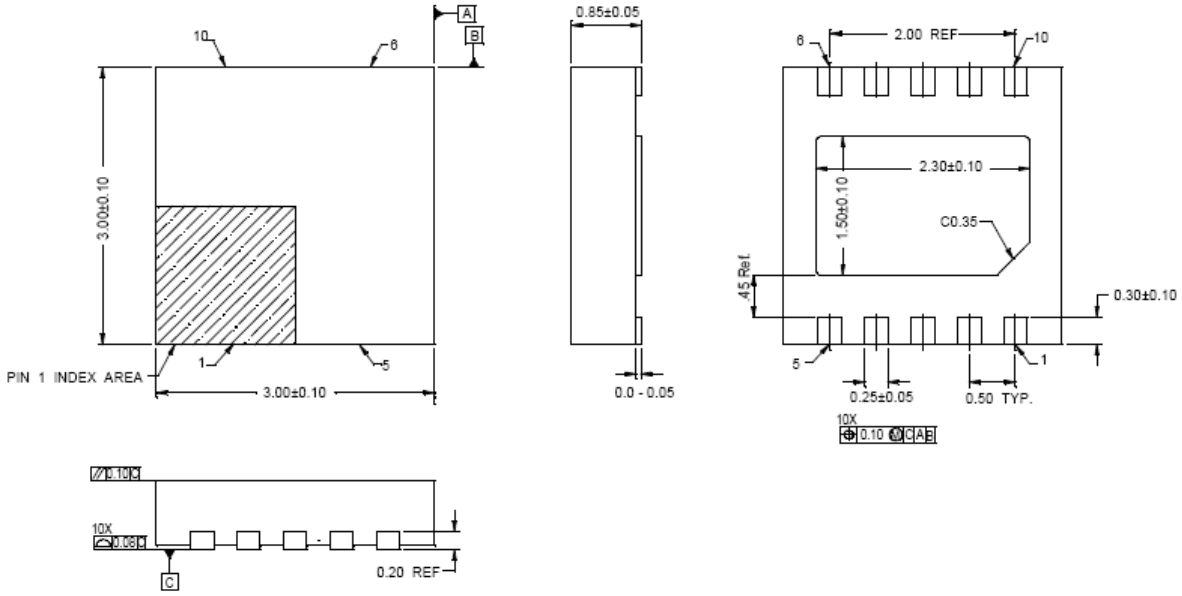


Figure 18: PI2001 and MOSFET layout recommendation

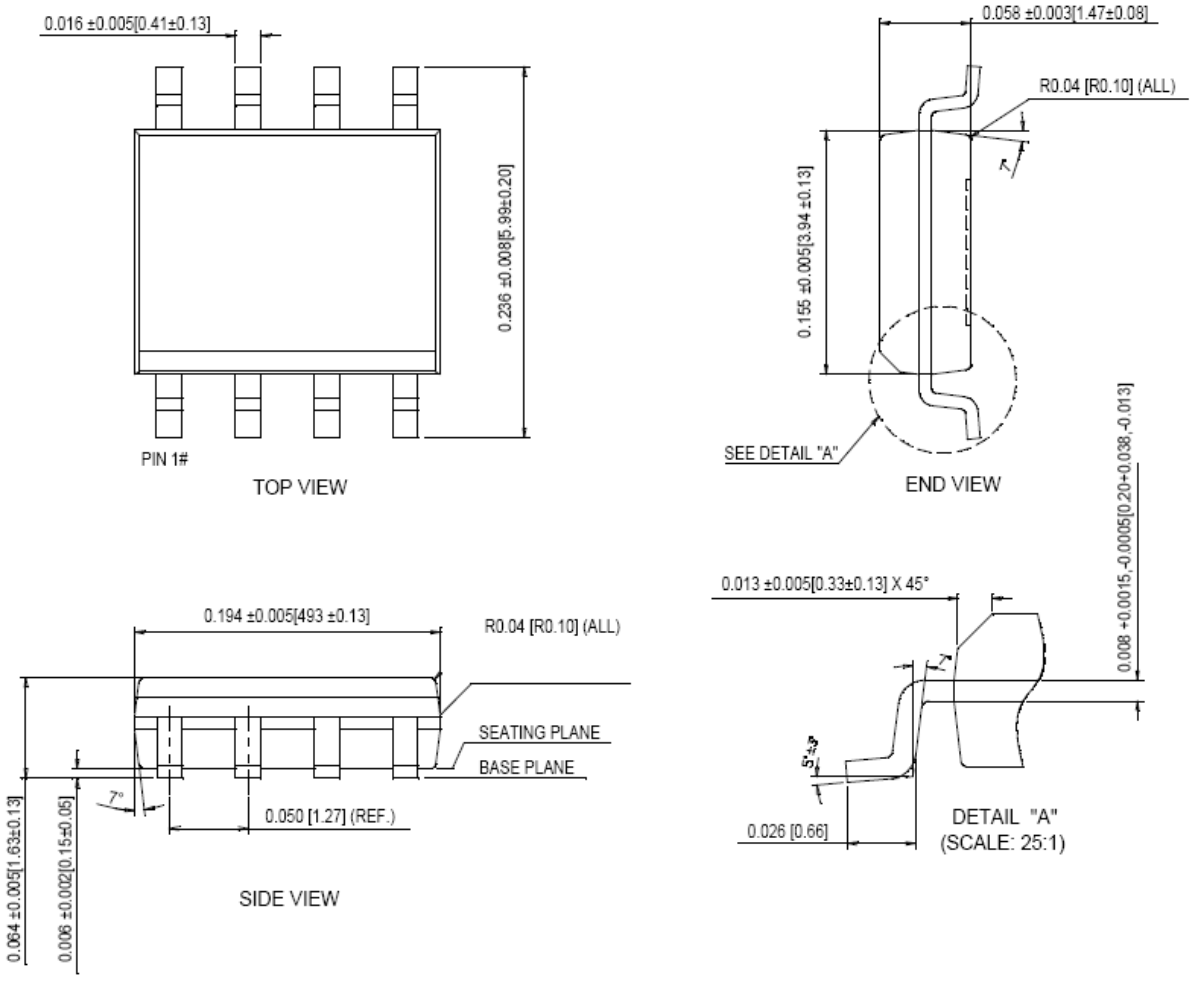
Package Drawing: 10 Lead TDFN



NOTES :

1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity does not exceed .05mm
3. Package is variation of JEDEC MO-229
4. Warpage does not exceed .05mm

Package Drawing: 8 Lead SOIC



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN INCHES [MM]
2. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 [0.15] PER SIDE
3. FORMED LEADS SHALL BE PLANAR WITH REPECT TO ONE ANOTHER WITHIN 0.003 [0.08] AT SEATING PLANE
4. GENERAL ANGLE TOLERANCES TO BE +/-2°
5. GENERAL TOLERANCES TO BE +/- 0.005 [0.13]
6. THIS POD COMPLIES TO MS-012 ISSUE C

Ordering Information

Part Number	Package	Transport Media
PI2001-00-QEIG	3mm x 3mm 10 Lead TDFN	Tape & Reel
PI2001-00-SOIG	8 Lead SOIC	Tape & Reel

Warranty

Vicor products are guaranteed for two years from date of shipment against defects in material or workmanship when in normal use and service. This warranty does not extend to products subjected to misuse, accident, or improper application or maintenance. Vicor shall not be liable for collateral or consequential damage. This warranty is extended to the original purchaser only.

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