A8303 and A8303-1

Single LNB Supply and Control Voltage Regulator

Discontinued Product

These parts are no longer in production The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 28, 2019

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

A8303 and A8303-1

Single LNB Supply and Control Voltage Regulator

FEATURES AND BENEFITS

- Integrated boost MOSFET, current sensing, and compensation
- Stable with low-profile ceramic boost capacitors
- Configurable output settings to meet global requirements
- A8303-1 includes 11.667 V setting to meet Japanese market requirements
- Adjustable LNB output current limit from 250 to 950 mA
  - □ Covers wide array of application requirements
  - □ Minimizes component sizing to fit each application
  - □ For startup, reconfiguration, and continuous output (maximum value depends on PCB thermal design)
- Boost peak current limit scales with LNB current limit setting
- 8 programmable LNB output voltage (DAC) levels
- LNB overcurrent limiter with shutdown timer
- Static LNB current limit reliably starts a wide range of loads
- Tracking boost converter minimizes power dissipation
- LNB transition times configurable by external capacitor

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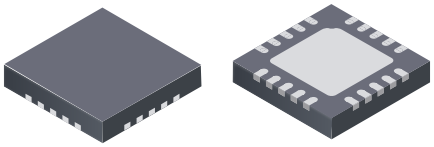
PACKAGE:



20-contact MLP/QFN (suffix ES)
4 mm × 4 mm × 0.75 mm

DESCRIPTION

Intended for analog and digital satellite receivers, these single low noise block converter regulator (LNBR) are monolithic linear and switching voltage regulators, specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable. The A8303 and A8303-1 require few external components, with the boost switch and compensation circuitry integrated inside of the devices. A high switching frequency is chosen to minimize the size of the passive filtering components, further assisting in cost reduction. The high levels of component integration ensure extremely low noise and ripple figures.

The A8303 and A8303-1 have been designed for high efficiency, using the Allegro™ advanced BCD process. The integrated boost switch has been optimized to minimize both switching and static losses. To further enhance efficiency, the voltage drop across the tracking regulator has been minimized.

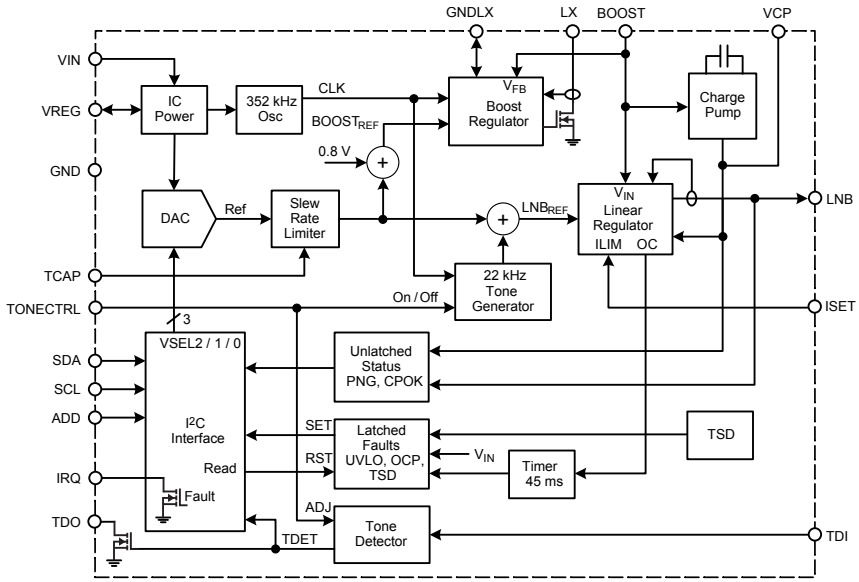
For DiSEqC™ communications, a tone control pin is provided to gate the internally generated 22 kHz tone on-and-off.

A comprehensive set of fault registers are provided, which comply with all the common standards, including: overcurrent, thermal shutdown, undervoltage, and power not good.

Furthermore, design methodology and structure ensure the highest level of robustness against transients and component failures. The devices use a 2-wire bidirectional serial interface, compatible with the I²C™ standard, that operates up to 400 kHz.

The A8303 and A8303-1 are supplied in a lead (Pb) free package.

Functional Block Diagram



FEATURES AND BENEFITS (continued)

- Push-pull LNB output stage maintains 13→18 V and 18→13 V transition times, even with highly capacitive loads
- Built-in 22 kHz tone oscillator facilitates DiSEqC™ tone encoding, even at no-load
- Tone generation does not require additional external components
- Diagnostic features: PNG, TDET
- Dynamic tone detect amplitude and frequency transmit/receive thresholds
- Extensive protection features: UVLO, OCP, TSD, CPOK
- 2-wire I²C-compatible interface

SELECTION GUIDE

Part Number	Output Voltage Settings	Packing [1]	Description
A8303SESTR-T	Refer to Table 3a	7 in. reel, 1500 pieces/reel 12 mm carrier tape	ES package [2], MLP/QFN surface mount 4 mm × 4 mm × 0.75 mm nominal height
A8303SESTR-T-1	Refer to Table 3b		

[1] Contact Allegro for additional packing options.

[2] Leadframe plating 100% matte tin.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Rating	Unit
Load Supply Voltage, VIN pin	V_{IN}		30	V
Output Current [3]	I_{OUT}		Internally Limited	A
Output Voltage: BOOST pin			–0.3 to 43	V
Output Voltage: LNB pin		Surge [4]	–1.0 to 43	V
Output Voltage: LX pin			–0.3 to 30	V
Output Voltage: VCP pin			–0.3 to 48	V
Logic Input Voltage			–0.3 to 5.5	V
Logic Output Voltage			–0.3 to 5.5	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[3] Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.

[4] See application schematics 3 and 4 on pages 24 and 25.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [5]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	37	°C/W

[5] Additional thermal information available on the Allegro website.

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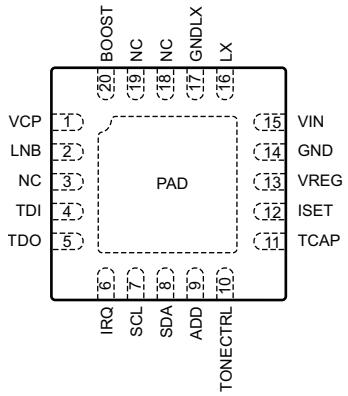
Pinout Diagram



Terminal List Table

Name	Number	Function
ADD	9	Address select
BOOST	20	Tracking supply voltage to linear regulator
GND	14	Signal ground
GNDLX	17	Boost switch ground
IRQ	6	Interrupt request
ISET	12	Output current limit set via external resistor
LNB	2	Output voltage to satellite dish
LX	16	Inductor drive point
NC	3,18,19	No connection
PAD	Pad	Exposed pad; connect to the ground plane, for thermal dissipation
SCL	7	I²C™-compatible clock input
SDA	8	I²C™-compatible data input/output
TCAP	11	Capacitor for setting the rise and fall time of the LNB output
TDI	4	Connect to output for 22 kHz tone verification function
TDO	5	Open-drain logic output that transitions low when a 22 kHz tone is present at TDI
TONECTRL	10	Gates the 22 kHz tone on-and-off
VCP	1	Gate supply voltage
VIN	15	Supply input voltage
VREG	13	Analog supply

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted [2], unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
GENERAL							
Output Voltage Accuracy	V_{OUT}	V_{IN} = 12 V, I_{OUT} = 50 mA, see tables 3a and 3b for DAC settings	•	–2	–	2	%
Load Regulation	$\Delta V_{OUT(Load)}$	V_{IN} = 12 V, V_{OUT} = 13.667 V, ΔI_{OUT} = 50 to 700 mA	•	–	75	120	mV
		V_{IN} = 12 V, V_{OUT} = 19.000 V, ΔI_{OUT} = 50 to 700 mA	•	–	85	150	mV
Line Regulation	$\Delta V_{OUT(Line)}$	V_{IN} = 10 to 16 V, V_{OUT} = 13.667 V, I_{OUT} = 50 mA	•	–10	0	10	mV
		V_{IN} = 10 to 16 V, V_{OUT} = 19.000 V, I_{OUT} = 50 mA	•	–10	0	10	mV
Supply Current	$I_{IN(OFF)}$	ENB = 0, V_{IN} = 12 V		–	4	–	mA
	$I_{IN(ON)}$	ENB = 1, V_{IN} = 12 V, V_{OUT} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 0		–	11	–	mA
		ENB = 1, V_{IN} = 12 V, V_{OUT} = 19 V, I_{LOAD} = 0 mA, TONECTRL = 1		–	17	–	mA
Boost Switch On Resistance	$R_{DS(on)}$ BOOST	I_{SW} = 450 mA		–	300	–	mΩ
Switching Frequency	f_{SW}			320	352	384	kHz
Linear Regulator Voltage Drop	ΔV_{REG}	$V_{BOOST} – V_{LNB}$, no tone signal, I_{LOAD} = 700 mA		600	800	1000	mV
TCAP Pin Current	I_{TCAP}	TCAP capacitor (C12) charging		–13	–10	–7	µA
		TCAP capacitor (C12) discharging		7	10	13	µA
Output Voltage Rise Time [3]	$t_{r(VLNB)}$	For V_{LNB} 13.667 to 19.667 V; C_{12} = 100 nF, I_{LOAD} = 700 mA		–	10	–	ms
Output Voltage Pull-Down Time [3]	$t_{f(VLNB)}$	For V_{LNB} 19.667 to 13.667 V; C_{LOAD} = 100 µF, I_{LOAD} = 0 mA		–	25	–	ms
LNB Sink Current [3]	I_{RLNB}	ENB = 0, V_{LNB} = 21 V, Boost capacitor fully charged		–	2	4	mA
		ENB = 1, $VSEL_{2,1,0}$ = 001 (13.667 V), V_{LNB} = 21 V, TONECTRL = 0 or 1		–	9	15	mA
		ENB = 1, $VSEL_{2,1,0}$ = 101 (19.000 V), V_{LNB} = 21 V, TONECTRL = 0 or 1		–	9	15	mA
		ENB = 1, $VSEL_{2,1,0}$ = 110 (19.667 V), 18.5 V < V_{LNB} <21 V, TONECTRL = 0		–	30	40	mA
LNB Off Current	$I_{LNB(Off)}$	V_{IN} = 16 V		–	–	10	µA

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted [2], unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
GENERAL (continued)							
Ripple and Noise on LNB Output [4]	$V_{rip,n(pp)}$	20 MHz BWL; reference circuit shown in Application Information section; contact Allegro for additional information on application circuit board design		–	15	–	mV_{PP}
VREG Voltage	V_{VREG}	V_{IN} = 10 V		4.97	5.25	5.53	V
ISET Voltage	V_{ISET}	V_{IN} = 10 V		3.4	3.5	3.6	V
TCAP Voltage	V_{TCAP}	V_{IN} = 10 V, V_{OUT} = 13.667 V		–	2.28	–	V
		V_{IN} = 10 V, V_{OUT} = 19.000 V		–	3.17	–	V
PROTECTION CIRCUITRY							
Output Overcurrent Limit [5]	$I_{OUT(MAX)}$	R_{SET} = 100 kΩ	•	250	300	350	mA
		R_{SET} = 37.4 kΩ	•	720	800	880	mA
Overcurrent Disable Time	t_{DIS}			–	45	–	ms
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling		8.05	8.35	8.65	V
VIN Turn On Threshold	$V_{IN(th)}$	V_{IN} rising		8.40	8.70	9.00	V
Undervoltage Hysteresis	$V_{UVLOHYS}$			–	350	–	mV
Boost MOSFET Current Limit	$I_{BOOST(MAX)}$	R_{SET} = 100 kΩ		–	1680	–	mA
		R_{SET} = 37.4 kΩ		–	4030	–	mA
Thermal Shutdown Threshold [3]	T_J			–	165	–	°C
Thermal Shutdown Hysteresis [3]	ΔT_J			–	20	–	°C
Power Not Good (Low)	PNG_{LOSET}	With respect to V_{LNB} setting; V_{LNB} low, PNG set to 1		88	91	94	%
	$PNG_{LORESET}$	With respect to V_{LNB} setting; V_{LNB} low, PNG reset to 0		92	95	98	%
Power Not Good (Low) Hysteresis	PNG_{LOHYS}	With respect to V_{LNB} setting		–	4	–	%
Power Not Good (High)	PNG_{HISET}	With respect to V_{LNB} setting; V_{LNB} high, PNG set to 1		106	109	112	%
	$PNG_{HIRESET}$	With respect to V_{LNB} setting; V_{LNB} high, PNG reset to 0		102	105	108	%
Power Not Good (High) Hysteresis	PNG_{HIHYS}	With respect to V_{LNB} setting		–	4	–	%
TONE							
Amplitude (A8303)	$V_{TONE(PP)}$	I_{LNB} = 0 to 700 mA, C_{LNB} = 750 nF	•	400	650	900	mV_{PP}
Amplitude (A8303-1)	$V_{TONE(PP)}$	I_{LNB} = 0 to 700 mA, C_{LNB} = 330 nF	•	400	650	800	mV_{PP}
Frequency	f_{TONE}	I_{LNB} = 0 to 700 mA, C_{LNB} = 750 nF or 330 nF	•	20	22	24	kHz
Duty Cycle	DC_{TONE}			40	50	60	%
Rise Time	$t_{R(TONE)}$			5	10	15	µs
Fall Time	$t_{F(TONE)}$			5	10	15	µs

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid at T_A = 25°C, V_{IN} = 10 to 16 V, • as noted [2], unless noted otherwise

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
TONE DETECTION							
Amplitude	$V_{TDX(PP)}$	TONECTRL = 1		400	650	900	mV_{PP}
	$V_{TDR(PP)}$	TONECTRL = 0; 22 kHz sine wave		250	650	900	mV_{PP}
Reject Amplitude, Low	$V_{TD(XMT)L}$	TONECTRL = 1		–	–	250	mV_{PP}
	$V_{TD(RCV)L}$	TONECTRL = 0; 22 kHz sine wave		–	–	100	mV_{PP}
Reject Amplitude, High	$V_{TD(XMT)H}$	TONECTRL = 1		–	–	1100	mV_{PP}
	$V_{TD(RCV)H}$	TONECTRL = 0; 22 kHz sine wave		–	–	1100	mV_{PP}
Frequency Capture	$f_{TD(RCV)}$	TONECTRL = 0; 650 mV_{PP} sine wave		17	22	27	kHz
	$f_{TD(XMT)}$	TONECTRL = 1; 650 mV_{PP} sine wave		20	22	24	kHz
Frequency Reject, Low	$f_{TD(RCV)L}$	TONECTRL = 0; 650 mV_{PP} sine wave		12	14	–	kHz
	$f_{TD(XMT)L}$	TONECTRL = 1; 650 mV_{PP} sine wave		15	17	–	kHz
Frequency Reject, High	$f_{TD(RCV)H}$	TONECTRL = 0; 650 mV_{PP} sine wave		–	34	37	kHz
	$f_{TD(XMT)H}$	TONECTRL = 1; 650 mV_{PP} sine wave		–	30	33	kHz
Detection Delay	t_{DET}	650 mV_{PP}, 22 kHz sine wave		–	1.5	3	cycle
TDI Input Impedance	Z_{TDI}			–	8.6	–	kΩ
TDO Output Voltage	$V_{TDO(L)}$	Tone present, I_{LOAD} = 3 mA		–	–	0.4	V
TDO Output Leakage	I_{TDO}	Tone absent, 0 V < V_{TDO} < 5 V		–	–	10	µA
TONE CONTROL (TONECTRL)							
Logic Input	V_H			2.0	–	–	V
	V_L			–	–	0.8	V
Input Leakage				–1	–	1	µA
I²C™-COMPATIBLE INTERFACE							
Logic Input (SDA,SCL) Low Level	$V_{SCL(L)}$			–	–	0.8	V
Logic Input (SDA,SCL) High Level	$V_{SCL(H)}$			2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$			–	150	–	mV
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 5 V		–1	<±1.0	1	µA
Logic Output Voltage SDA and IRQ	$V_{OUT(L)}$	I_{LOAD} = 3 mA		–	–	0.4	V
Logic Output Leakage SDA and IRQ	V_{LKG}	V_{OUT} = 0 to 5 V		–	–	10	µA
SCL Clock Frequency	f_{CLK}			–	–	400	kHz
I²C™ ADDRESS SETTING							
ADD Voltage for Address 0001,000	Address1			0	–	0.7	V
ADD Voltage for Address 0001,001	Address2			1.3	–	1.7	V
ADD Voltage for Address 0001,010	Address3			2.3	–	2.7	V
ADD Voltage for Address 0001,011	Address4			3.3	–	5.0	V

[1] Operation at 16 V may be limited by power loss in the linear regulator.
[2] Indicates specifications guaranteed from 0 ≤ T_J ≤ 125°C_{MIN}.
[3] Guaranteed by worst case process simulations and system characterization. Not production tested.
[4] LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the Application Schematic and PCB layout recommendations. Not production tested.
[5] Current from the LNB output may be limited by the choice of Boost components.

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FUNCTIONAL DESCRIPTION

Protection

The A8303 and A8303-1 have a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

Boost Converter/Linear Regulator

The A8303 and A8303-1 solution contains a tracking current-mode boost converter and linear regulator. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOST}, is greater than the output voltage, V_{LNB}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8303 and A8303-1 is not exceeded.

The boost converter operates at 352 kHz typical: 16 times the internal 22 kHz tone frequency. All the loop compensation, current sensing, and slope compensation functions are provided internally.

The A8303 and A8303-1 have internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against short circuits. When the LNB output is shorted, the LNB output current is limited, and if the overcurrent condition lasts for more than 45 ms, the LNB output will be disabled. If this occurs, the A8303 and A8303-1 output must be reenabled for normal operation. The system should provide sufficient time between successive restarts to limit internal power dissipation; 1 to 2 seconds is recommended

At extremely light load or no load, if the BOOST voltage tries to exceed the BOOST target voltage, the boost converter operates with minimum on time. BOOST settling voltage depends on supply voltage, boost inductance, minimum on time, switching frequency, output power and power loss in boost inductor, capacitor and A8303 and A8303-1. If the BOOST voltage settles below pulse skipping threshold (23.7 V), the boost converter continues to operate with minimum on time. If BOOST voltage tries to exceed 23.7 V, pulse skipping occurs, and pulse skipping stops when the BOOST voltage drops to 23.4 V.

In the case that two or more set top box LNB outputs are connected together by the customer (e.g., with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (e.g., 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8303 and A8303-1 output will auto-recover to their programmed levels.

Charge Pump. Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

LNB and BOOST Current Limits. The LNB output current limit, $I_{OUT(MAX)}$ can be set by connecting a resistor (RSET) from the ISET pin to GND as shown in the applications schematic. The LNB current limit can be set from 300 to 800 mA, corresponding to an R_{SET} value of 100 to 37.4 kΩ, respectively. If the LNB current limit is exceeded for more than the Overcurrent Disable Time (t_{DIS}) then the A8303 and A8303-1 will be shut down and the OCP bit set, as shown in figure 1. The LNB output current limit can be set as high as 950 mA (R_{SET} = 31.6 kΩ) but care should be taken not to exceed the thermal limit of the package or thermal shutdown (TSD) will occur. The typical LNB output current limit can be set according to the following equation:

$$I_{OUT(MAX)} = 29{,}925 / R_{SET} \ ,$$

where $I_{OUT(MAX)}$ is in mA and R_{SET} is in kΩ. If the voltage at the ISET pin is 0 V (that is, shorted to GND), $I_{OUT(MAX)}$ will be clamped to a moderately high value (approximately 1.5 A). Care should be taken to ensure that ISET is not inadvertently grounded. If no resistor is connected to the ISET pin (that is, if ISET is open-circuit), $I_{OUT(MAX)}$ will be set to approximately 0 A and the A8303 and A8303-1 will not support any load (OCP will occur prematurely).

The BOOST pulse-by-pulse current limit, $I_{BOOST(MAX)}$, is automatically scaled along with the LNB output current limit. The typical BOOST current limit is set according to the following equation:

$$I_{BOOST(MAX)} = 4.7 \times I_{OUT(MAX)} + 270 \text{ mA} \ ,$$

where both $I_{BOOST(MAX)}$ and $I_{OUT(MAX)}$ are in mA.

Automatically scaling the BOOST current limit allows the designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

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Slew Rate Control. During either start-up, or when the output voltage at the LNB pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAP pin to GND (C12 in the Applications Schematic). Note that during start-up, the BOOST pin is pre-charged to the input voltage minus a diode voltage drop. As a result, the slew rate control for the BOOST pin occurs from this voltage.

The value of C12 can be calculated using the following formula:

$$C_{12} = (I_{TCAP} \times 6) / SR \ ,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAP} is the TCAP pin current specified in the Electrical Characteristics table. The recommended value for C_{12}, 100 nF, should provide satisfactory operation for most applications.

The minimum value of C_{12} is 10 nF. There is no theoretical maximum value of C_{12} however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of C_{12} .

Pull-Down Rate Control. In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), the output linear stage provides approximately 45 mA of pull-down capability. This ensures that the LNB output voltage is ramped from 18 to 13 V in a reasonable amount of time. When the tone is on (TONECTRL = 1), the output linear stage must increase its pull-down capability to approximately 100 mA. This ensures that the tone signal meets all specifications, even with no load on the on the LNB output.

ODT (Overcurrent Disable Time)

If the LNB output current exceeds the set output current, for more than 45 ms, then the LNB output will be disabled and the OCP bit will be set. See figure 1.

Short Circuit Handling

If the LNB output is shorted to ground, the LNB output current will be clamped to $I_{OUT(MAX)}$. If the short circuit condition lasts for more than 45 ms, the A8303 and A8303-1 will be disabled and the OCP bit will be set.

Auto-Restart

After a short circuit condition occurs, the host controller should periodically reenable the A8303 and A8303-1 to check if the short circuit has been removed. Consecutive startup attempts should allow 1 to 2 seconds of delay between restarts.

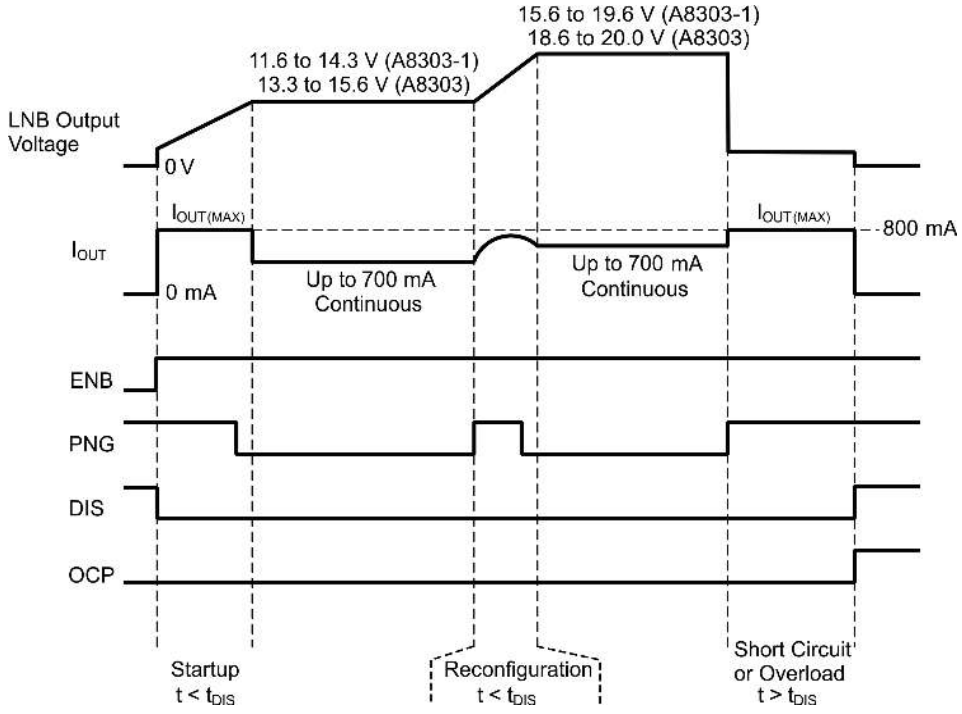

Figure 1. Startup, Reconfiguration, and Short Circuit operation using R_{SET} = 37.4 kΩ, and a capacitive load

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In-Rush Current

At start-up or during an LNB reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8303 and A8303-1. This current increase can be as high as the set output current, for as long as required, up to a maximum of 45 ms.

Tone Generation

A 22 kHz tone is generated internally, and can be controlled on and off via the TONECTRL pin as shown in figure 2. Note this tone can be generated under no-load conditions, and does not require the use of an external DiSEqC filter.

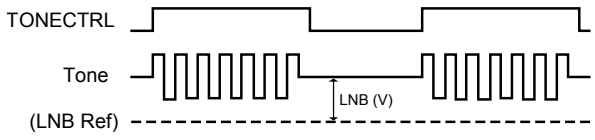

Figure 2. Internal tone, gated by TONECTRL pin

Tone Detection

A 22 kHz tone detector is provided in the A8303 and A8303-1. The detector extracts the 22 kHz signal from the AC-coupled TDI pin and provides it as an open-drain logic output at the TDO pin. Also, when a tone is present, the TDET bit in the Status register is set high and can be seen via the I^2C interface. The tone detection delay is typically shorter than 1.5 cycles.

The tone detector dynamically adjusts its amplitude and frequency thresholds depending on whether the A8303 and A8303-1 are transmitting or receiving a tone signal. If TONECTRL is a logic high, the A8303 and A8303-1 are transmitting and the tone detect amplitude threshold is relatively high and the acceptable frequency range is tight. This guarantees a high quality tone signal is always generated by the A8303 and A8303-1. On the other hand, if TONECTRL is a logic low, the A8303 and A8303-1 are receiving and the tone detect amplitude threshold is reduced and the acceptable frequency range is increased slightly. This guarantees the A8303 and A8303-1 have maximum sensitivity to remotely generated tone signals that may be degraded by long lengths of coaxial cable. The Electrical Characteristics table of this datasheet documents the guaranteed specifications of the tone detector and how they are adjusted by TONECTRL. To help in the understanding, typical tone detector operation is shown graphically in figures 3a and 3b. The shaded areas in figure 3a indicate the accept range of the detector when TONECTRL is a logic high (transmit) and a logic low (receive). The shaded areas in figure 3b indicate the reject range of the detector when TONECTRL is a logic high (transmit) and a logic low (receive).

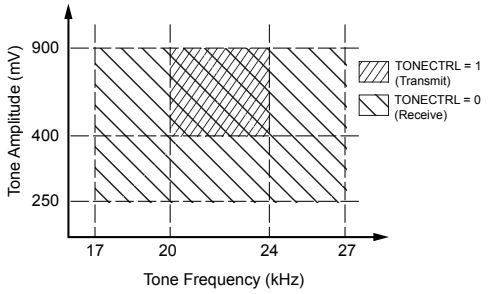

Figure 3a. Accept Ranges of Tone Detection feature

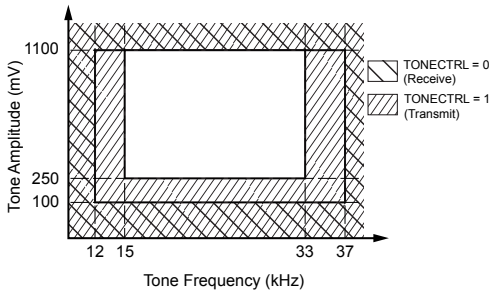

Figure 3b. Reject Ranges of Tone Detection feature

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Component Selection

BOOST INDUCTOR

The A8303 and A8303-1 are designed to operate with a boost inductor value of 15 µH +30%/–40% with a DCR less than 75 mΩ. The error amplifier loop compensation, current sense gain, and PWM slope compensation were chosen for this value of inductor. The boost inductor must be able to support the peak currents required to maintain the maximum LNB output current without saturating. Figure 4 can be used to determine the peak current in the inductor given the LNB load current. The "typical" curve uses V_{IN} = 12 V, V_{OUT} = 19 V, L = 15 µH, and f = 352 kHz, while the "maximum" curve assumes V_{IN} = 9 V, V_{OUT} = 20 V, L = 12 µH, and f = 282 kHz.

The system will have reduced gain and phase margins, if the boost inductor is higher than 22 µH. Figure 6 shows a Bode plot of the boost loop with 3 × 10 µF of boost capacitance and 33, 22, 18, 15, and 10 µH of boost inductance. Although this plot assumes many of the system variables are "worst case" (10.8 V_{IN}, 20 V_{OUT}, +2% DAC tolerance, 1V of ΔV_{REG}, 1.1 A load, and 320 kHz), these conditions could certainly occur in an application. This plot shows that, as the boost inductance increases, the 0 dB crossover frequency remains relatively constant but the phase and gain margins are reduced. With 22 µH, the phase margin is 32° and with 33 µH the phase margin is only 10°.

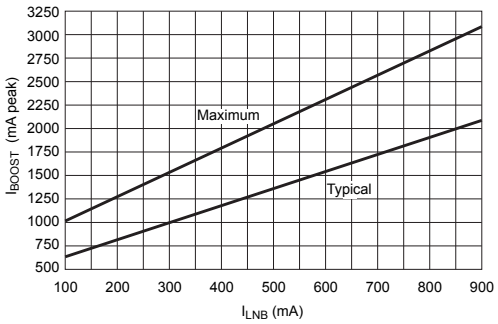

Figure 4. Boost inductor peak current versus I_{LNB}

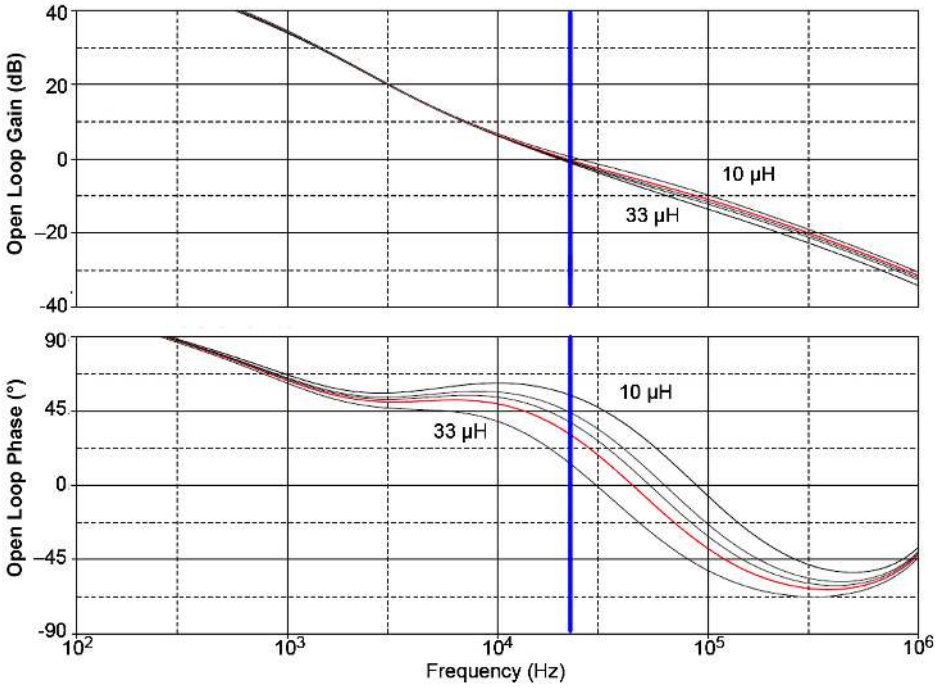

Figure 6. Gain and Phase Margin of the boost loop at various inductance levels

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BOOST CAPACITORS

The A8303 and A8303-1 are designed to operate with two or three, high-quality ceramic capacitors on the boost node. Allegro recommends capacitors that are rated at least 35 V, ±10%, X7R, 1210 size. Physically smaller capacitors, like 0603 and 0805, with lower temperature ratings, like X5R and Z5U, should be avoided. Figure 5 can be used to determine the necessary rms current rating of the boost capacitor given the LNB load current. The "typical" curve uses V_{IN} = 12 V, V_{OUT} = 19 V, L = 15 µH, and f = 352 kHz while the "maximum" curve assumes V_{IN} = 9 V, V_{OUT} = 20 V, L = 12 µH, and f = 282 kHz.

The nominal boost capacitance should total 18.8 to 30 µF. Allegro recommends either four 4.7 µF or three 10 µF capacitors, with the characteristics shown in table 1. If tolerance, temperature, and DC bias effects are considered, the capacitance must total at least 13 µF. The DC bias effect is very significant on ceramic capacitors with lower voltage ratings, smaller packages, or wider temperature characteristics. For example, a 10 µF, 25 V, 1206, X5R capacitor can lose 85% of its value at 20 VDC bias. If the total boost capacitance becomes less than 12 µF, the converter will have reduced gain and phase margins. If the total boost capacitance becomes less than 7.5 µF, then the converter will very likely be unstable.

Figure 7 shows a Bode plot of the boost loop with 15 µH of boost inductance and 20, 15, 10, 7.5, and 5 µF of boost capacitance. Although this plot assumes many of the system variables are "worst case" (10.8 V_{IN}, 20 V_{OUT}, +2% DAC tolerance, 1 V of ΔV_{REG}, 1.1 A load, and 320 kHz), these conditions could certainly occur in an application. This plot shows that, as the boost capacitance decreases, the 0 dB crossover frequency increases and the phase and gain margins are reduced. At 7.5 µF the phase margin is only 6° and at 5 µF this system is unstable.

Two possible ceramic based capacitor solutions have been presented. Other capacitor combinations are certainly possible, such as a very low ESR electrolytic capacitor in parallel with several microfarads of ceramic capacitance. However, there are two critical requirements that must be satisfied: 1) the zero formed by the electrolytic capacitor and its ESR should be at least 1 decade higher than the 0 dB crossover of the boost loop (typically around 25 kHz), and 2) the ceramic capacitors must eliminate the high frequency switching spikes/edges in the boost voltage, or the LNB output noise will be too high.

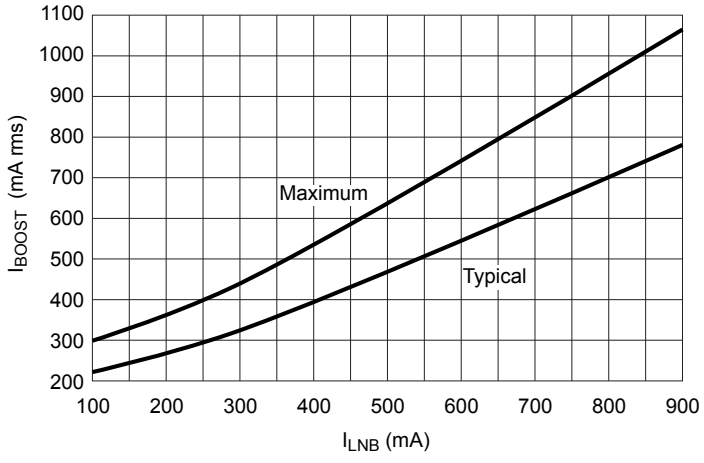

Figure 5. Boost capacitor rms current versus I_{LNB}

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Table 1. Recommended Boost Capacitor Characteristics

Quantity of Capacitors	Value (µF)	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size	Total Capacitance at –10% and 20 VDC Bias (µF)
4	4.7	±10	50	X7R	1210	14.0
3	10	±10	35	X7R	1210	18.6

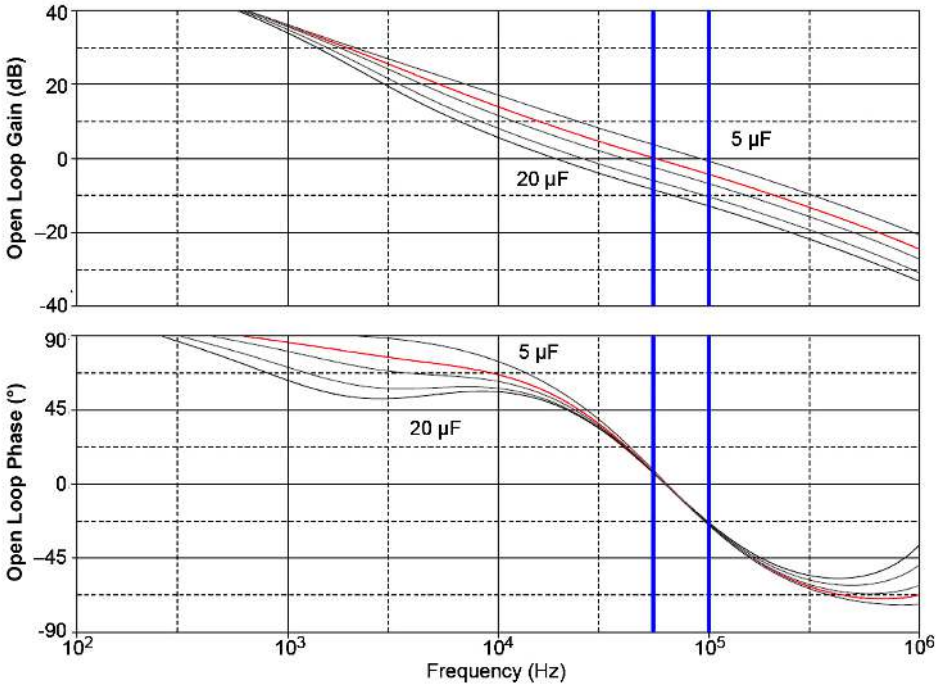

Figure 7. Gain and Phase Margin of the boost loop at various capacitance values

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BOOST FILTERING AND LNB NOISE

The LNB output noise depends on the amount of high-frequency noise at the BOOST pin. To minimize the high-frequency noise at the BOOST pin, the ceramic capacitors should be placed as close as possible to the BOOST pin.

SURGE COMPONENTS

The circuit shown in schematic 1 includes external diodes for surge protection. The Applications Information section includes D2, D3, and D4 component recommendations in table 6. This configuration and these components have successfully passed surge tests up to ±1000 V/500 A, with a 1.2/50 µs − 8/20 µs combination wave.

Recently, set-top box suppliers have increased their surge specifications to require "surge to failure of the TVS" or ±4000 V, whichever occurs first. These increased surge voltages produce significantly more current in the both the external circuitry and the A8303 and A8303-1. Allegro surge testing has shown that the SMDJ20A and LNBTVS6-221 usually fail at approximately 43 V, so all the LNBR output components (ceramic capacitors, diodes, etc.) should support at least 50 V.

To protect at these higher voltage/current levels three modifications must be made:

- For increased positive surge, the shunting diode from the LNB pin to the BOOST pin (D3, 3 A/40 V) will no longer be able to protect the body diode of the output stage. This diode must be increased to a 3 A/50 V device and be located so that it is in series with the BOOST pin as shown in schematics 3 and 4. In this position D3 will block surge current to the majority of the boost capacitance, but the 1 µF ceramic capacitor will still filter the high frequency switching noise.
- For increased negative surge, the relatively small clamping diode (D2) from LNB to ground will no longer be sufficient. This diode must be increased from a 1 A/40 V, SOD123 to a 3 A/50 V, SMA device.
- For a DiSEqC 1.0 application, a 0.47 Ω/1%/0.25 W series resistor also must be added as shown in the application drawings. The 0.47 Ω resistor could be reduced if there is enough equivalent resistance in any series output components such as jumpers, inductors, or PCB traces.

Every application will have its own surge requirements and the surge solution can be changed. However, Allegro strongly recommends incorporating a form of surge protection to prevent any pin of the A8303 and A8303-1 from exceeding its Absolute Maximum voltage ratings shown in this datasheet.

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I²C™-Compatible Interface

The I²C™ interface is used to access the internal Control and Status registers of the A8303 and A8303-1. This is a serial interface that uses two lines, serial clock (SCL) and serial data (SDA), connected to a positive supply voltage via a current source or a pull-up resistor. Data is exchanged between a microcontroller (master) and the A8303 and A8303-1 (slave). The master always generates the SCL signal. Either the master or the slave can generate the SDA signal. The SDA and SCL lines from the A8303 and A8303-1 are open-drain signals so multiple devices may be connected to the I²C™ bus. When the bus is free, both the SDA and the SCL lines are high.

SDA and SCL Signals. SDA can only be changed while SCL is low. SDA must be stable while SCL is high. However, an exception is made when the I²C™ Start or Stop condition is encountered. See the I²C™ Communication section for further details.

Acknowledge (AK) Bit. The Acknowledge (AK) bit indicates a "good transmission" and can be used two ways. First, if the slave has successfully received eight bits of either an address or control data, it will pull the SDA line low (AK = 0) for the ninth SCL pulse to signal "good transmission" to the master. Second, if the master has successfully received eight bits of status data from the A8303 and A8303-1, it will pull the SDA line low for the ninth SCL pulse to signal "good transmission" to the slave. The receiver (either the master or the slave) should set the AK bit high (AK = 1 or NAK) for the ninth SCL pulse if eight bits of data are not received successfully.

AK Bit During a Write Sequence. When the master sends control data (writes) to the A8303 and A8303-1 there are three instances where AK bits are toggled by the A8303 and A8303-1. First, the A8303 and A8303-1 use the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 0 for write). Second, the A8303 and A8303-1 use the AK bit to indicate reception of a valid eight-bit Control register address. Third, the A8303 and A8303-1 use the AK bit to indicate reception of eight bits of control data. This protocol is shown in figure 8(A).

AK Bit During a Read Sequence. When the master reads status data from the A8303 and A8303-1 there are four instances where AK bits are sent–three sent by the A8303 and A8303-1 and one sent by the master. First, the A8303 and A8303-1 use the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 0 for write). Second, the A8303 and A8303-1 use the AK bit to indicate reception of a valid eight-bit status register address. Third, the A8303 and A8303-1 use the AK bit to indicate reception of a valid seven-bit chip address plus a read/write bit (R/W = 1 for read). Finally, the master uses the AK bit to indicate receiving eight bits of status data from the A8303 and A8303-1. This protocol is shown in figure 8(B).

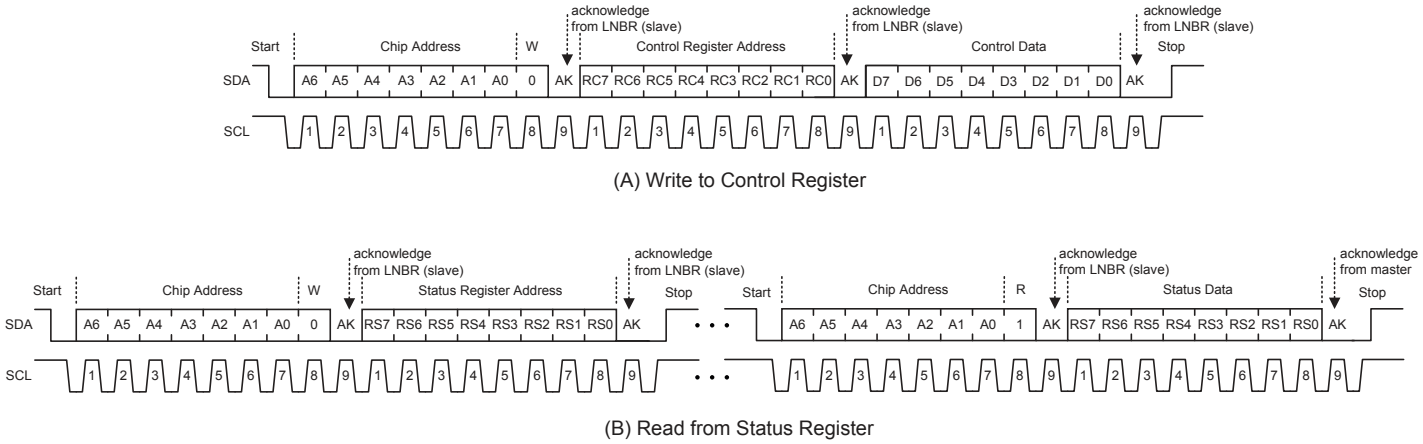

Figure 8. I²C™ Interface Read and Write Sequences. (A) for the I²C™ Write cycle and (B) for the I²C™ Read cycle

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I²C™ Communications

I²C™ Start and Stop Conditions. The I²C™ Start condition is defined by a negative edge on the SDA line while SCL is highConversely, the Stop condition is defined by a positive edge on the SDA line while SCL is high. The Start and Stop conditions are shown in figure 8. It is possible for the Start or Stop condition to occur at any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the A8303 and A8303-1 will respond by resetting the data transfer sequence.

I²C™ Write Cycle Description. Writing to the A8303 and A8303-1 Control register requires transmission of a total of 27 bits–three 8-bit bytes of data plus an Acknowledge bit after each byte. Writing to the A8303 and A8303-1 Control register is shown in figure 8(A). Writing to the A8303 and A8303-1 Control register requires a chip address with R/W = 0, a Control register address, and the control data, as follows:

- The Chip Address cycle consists of a total of nine bits—seven bits of chip address (A6 to A0) plus one read/write bit (R/W = 0) to indicate a write from the master followed by an Acknowledge bit (AK = 0 for reception of a valid chip address) from the slave. The chip address must be transmitted MSB (A6) first. The first five bits of the A8303 and A8303-1 chip address (A6 to A2) are fixed as 00010. The remaining two bits (A1 and A0) are used to select one of four possible A8303 and A8303-1 chip addresses. The DC voltage on the ADD pin programs the chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.
- The Control Register Address cycle consists of a total of nine bits—eight bits of control register address (RC7 to RC0) from the master followed by an Acknowledge bit from the slave. The Control register address must be transmitted MSB (RC7) first. The A8303 and A8303-1 only have one Control register each, so the Control register address is fixed as 00000000.
- The Control Data cycle consists of a total of nine bits—eight bits of control data (D7 to D0) from the master followed by an Acknowledge bit from the slave. The control data must be transmitted MSB first (D7). The Control register bits are identified in the Control Registers section of this datasheet.

I²C™ Read Cycle Description. Reading from the A8303 and A8303-1 Status register requires transmission of a total of 36 bits–four 8-bit bytes of data plus an Acknowledge bit after each byte. Reading the A8303 and A8303-1 Status register requires a chip address with R/W = 0, a Status register address, an I²C™ Stop condition, an I²C™ Start condition, a “repeated” chip address with R/W=1, and finally the status data from the A8303 and A8303-1. Reading from the A8303 and A8303-1 Status register is shown in figure 8(B).

- This 9-bit Chip Address cycle is identical to the Chip Address cycle previously described for the Write Control register sequence. It consists of A6 to A0, plus one read/write bit (R/W = 0) from the master, followed by an Acknowledge bit from the slave and finally an I²C™ Stop condition.
- The Status Register Address cycle consists of a total of nine bits–eight bits of Status register address (RS7 to RS0) from the master, followed by an Acknowledge bit from the slave. The Status register address must be transmitted MSB (RS7) first. The A8303 and A8303-1 only have one Status register, so the Status register address is fixed at 00000000.
- The “Repeated” Chip Address cycle begins with an I²C™ Start condition followed by a 9-bit cycle identical to the Chip Address cycle previously described for the Write Control Register sequence. It consists of A6 to A0, plus one read/write bit (R/W = 1) from the master, followed by an Acknowledge bit from the slave.
- The Status Data cycle consists of a total of nine bits–eight bits of status data (RD7 to RD0) from the slave, followed by an Acknowledge bit from the master. The status data is transmitted MSB (RD7) first. The Status register bits are identified in the Status Register section of this data sheet.

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Interrupt (IRQ) and Fault Clearing

The A8303 and A8303-1 provide an interrupt request pin (IRQ), which is an open-drain, active low output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I²C™ compatible devices to request attention from the master controller.

The IRQ output becomes active (logic low) when the A8303 and A8303-1 recognize a fault condition. The fault conditions that will force IRQ active include undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD). The UVLO, OCP, and TSD faults are latched in the Status register and will not be unlatched until the A8303 and A8303-1 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and figure 9 for further details.

The A8303 and A8303-1 IRQ response to $V_{IN(UVLO)}$ is controlled by the I²C address setting. The A8303 and A8303-1 have two methods to control the IRQ for UVLO fault:

- The first method uses the I²C address setting (Address 2, Address 3, or Address 4). In this method while V_{IN} is below 8.70 V (typ), the A8303 and A8303-1 are disabled and the I²C port is inactive. After V_{IN} rises above 8.70 V (typ), the I²C port becomes active and the IRQ pin is pulled low. An I²C Read cycle is required to report and clear the UVLO fault and set the IRQ pin to a logic high before the A8303 and A8303-1 can be enabled. If a brown-out occurs, such that V_{IN} drops below 8.35 V (typ), the A8303 and A8303-1 will be disabled and the I²C port will become inactive (note that the IRQ pin will remain high during this time because the A8303 and A8303-1 are disabled). After V_{IN} rises above 8.70 V (typ) the I²C port reactivates and the IRQ pin is pulled low to report that a brown-out had occurred. An I²C Read cycle is required to report and clear the UVLO fault before the A8303 and A8303-1 can be re-enabled. A detailed timing diagram is shown in figure 10(A).
- The second method uses I²C address setting (Address 1). In this method the I²C port is active when V_{IN} is above the I²C UVLO (6 V when V_{IN} is rising). IRQ transitions low when V_{IN} goes above I²C UVLO (6 V, V_{IN} rising), and the I²C Read cycle resets IRQ to logic high even if V_{IN} is below UVLO. Even though IRQ is cleared below UVLO, one more Read cycle is required after V_{IN} goes above UVLO, to re-enable the A8303 and A8303-1. While V_{IN} is falling, IRQ transitions low when V_{IN} goes below UVLO, and the I²C Read cycle resets IRQ to logic high. A detailed timing diagram is shown in figure 10(B).

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read the status register of each to determine which device is requesting attention. As shown in figure 9, the A8303 and A8303-1 latch all conditions in the Status register and set the IRQ to logic low when a UVLO, OCP, or TSD event occurs. The IRQ bit is reset to logic high and the Status register is unlatched when the master acknowledges the status data from the A8303 and A8303-1 (an AK bit must be received from the master).

The disable (DIS) and Power Not Good (PNG) conditions do not cause an interrupt and are not latched in the Status register.

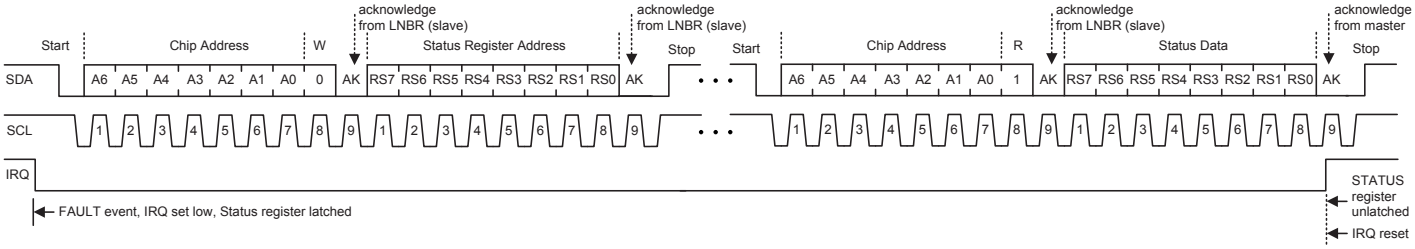

Figure 9. Fault, IRQ, and Status Register Timing. When a UVLO, OCP, or TSD event occurs, the IRQ bit is set low and the Status register is latched. The IRQ bit is reset to high when the A8303 and A8303-1 acknowledges it is being read. The Status register is unlatched when the master acknowledges the status data from the A8303 and A8303-1.

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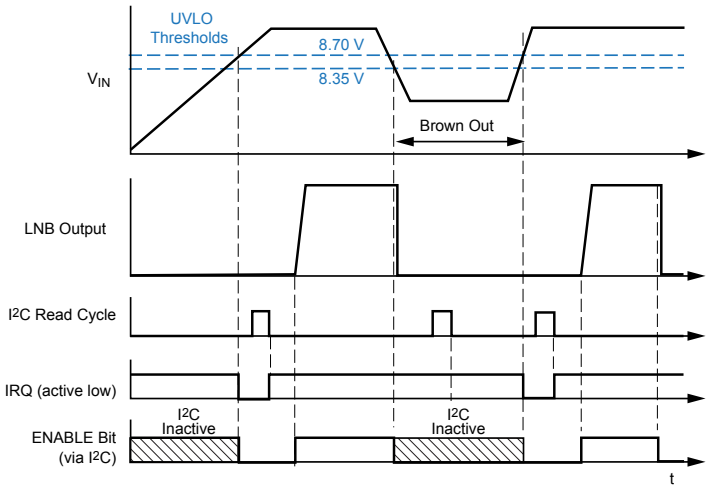
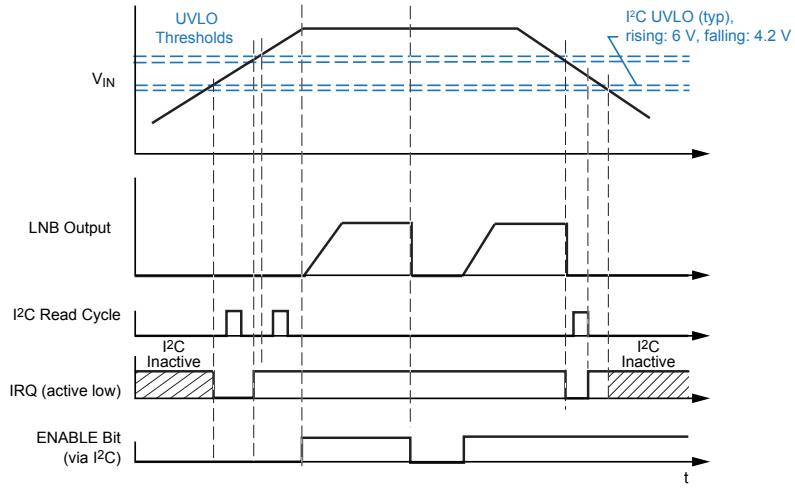


10(A). IRQ and Fault Clearing in Response to Undervoltage at VIN (UVLO), with I²C address set to (Address 2, Address 3, or Address 4). In this method, while V_{IN} is below 8.70 V (typ), the A8303 and A8303-1 are disabled and the I²C port is inactive. After V_{IN} rises above 8.70 V (typ), the I²C port becomes active and the IRQ pin is pulled low. An I²C Read cycle is required, to report and clear the UVLO fault and set the IRQ pin to a logic high, before the A8303 and A8303-1 can be enabled. If a brown-out occurs, such that V_{IN} drops below 8.35 V (typ), the A8303 and A8303-1 will be disabled and the I²C port will become inactive (note that the IRQ pin will remain high during this time because the A8303 and A8303-1 are disabled). After V_{IN} rises above 8.70 V (typ) the I²C port reactivates and the IRQ pin is pulled low to report that a brown-out had occurred. An I²C Read cycle is required to report and clear the UVLO fault before the A8303 and A8303-1 can be re-enabled.



10(B). IRQ and Fault Clearing in Response to Undervoltage at VIN (UVLO), with I²C address set to (Address 1). In this method, the I²C port is active when V_{IN} is above I²C UVLO (6 V when V_{IN} is rising). IRQ transitions low when V_{IN} goes above I²C UVLO (6 V, V_{IN} rising), and the I²C Read cycle resets IRQ to logic high even if V_{IN} is below UVLO. Even though IRQ is cleared below UVLO, one more Read cycle is required after V_{IN} goes above UVLO, to re-enable the A8303 and A8303-1. While V_{IN} is falling, IRQ transitions low when V_{IN} goes below UVLO, and the I²C Read cycle resets IRQ to logic high.

Figure 10. IRQ and Fault Clearing in Response to Undervoltage at VIN (UVLO), showing the alternate methods, set by selection of I²C address

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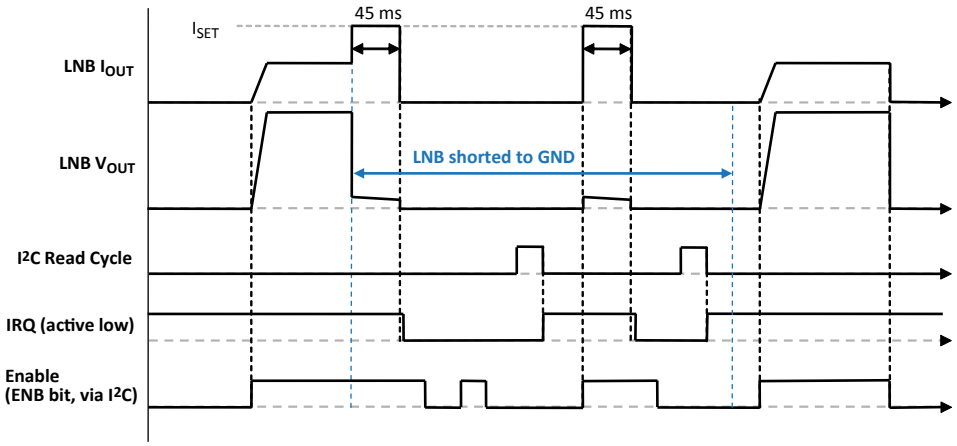

Figure 11. IRQ and Fault Clearing in Response to Overcurrent (OCP). If the LNB output is grounded for more than 45 ms, the LNB output will be shut off, an overcurrent fault (OCP) will be latched in the Status Register, and the IRQ pin will transition low. After an OCP fault, the LNB output does not respond to the Enable (ENB) bit until an I²C Read cycle is executed to report and clear the OCP fault. After a successful I²C Read, the IRQ pin transitions high and the A8303 and A8303-1 can be re-enabled, provided the LNB output is no longer grounded.

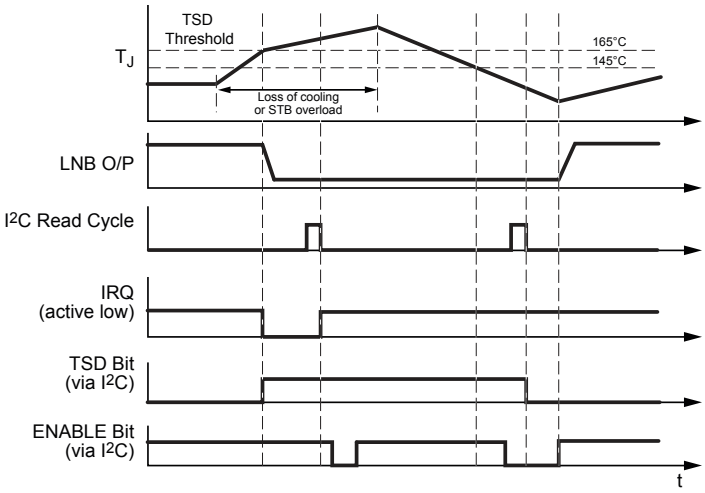

Figure 12. IRQ and Fault Clearing in Response to Thermal Shutdown (TSD). If the LNB junction temperature rises above 165°C (typ), the LNB output will be shut off, a thermal shutdown fault (TSD) will be latched in the Status Register, and the IRQ pin will transition low. After a TSD fault, the LNB output does not respond to the Enable (ENB) bit until an I²C Read cycle is executed to report and clear the TSD fault. After a successful I²C Read, the IRQ pin transitions high and the A8303 and A8303-1 can be re-enabled, provided the junction temperature is below 145°C (typ).

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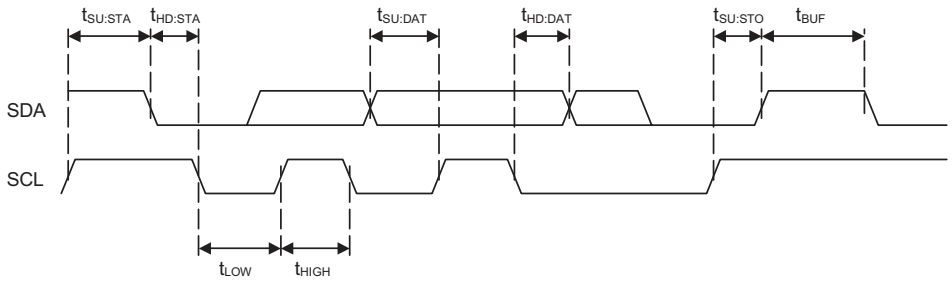
I²C™-Compatible Interface Timing Diagram



I²C™-Compatible Timing Requirements

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Bus Free Time Between Stop/Start	t_{BUF}	1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	0.6	–	–	µs
SCL Low Time	t_{LOW}	1.3	–	–	µs
SCL High Time	t_{HIGH}	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	100	–	–	ns
Data Hold Time*	$t_{HD:DAT}$	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	0.6	–	–	µs
Output Fall Time ($V_{fI2COut(H)}$ to $V_{fI2COut(L)}$)	$t_{fI2COut}$	–	–	250	ns

*For $t_{HD:DAT}$(min), the master device must provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the SCL signal falling edge.

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Control Registers (I²C™-Compatible Write Register)

All main functions of the A8303 and A8303-1 are controlled through the I²C™ compatible interface via the 8-bit Control register. Table 2 shows the functionality and bit definitions of the Control register. At power-up, the Control register is initialized to all 0s.

Table 2. Control Register Definition

Bit	Name	Function	Description
0	VSEL0	LNB output voltage control See Table 3a for A8303 output voltage selections See Table 3b for A8303-1 output voltage selections	The available voltages provide levels for all the common standards plus the ability to add line compensation. VSEL0 is the LSB and VSEL2 is the MSB to the internal DAC.
1	VSEL1		
2	VSEL2		
3	ENB	0: Disable LNB Output 1: Enable LNB Output	Turns the LNB output on or off.
4	–	Set to 0	Unused
5	–		
6	–		
7	–		

Table 3a. A8303 Output Voltage Selection

VSEL2	VSEL1	VSEL0	LNB (V)
0	0	0	13.333
0	0	1	13.667
0	1	0	14.333
0	1	1	15.667
1	0	0	18.667
1	0	1	19.000
1	1	0	19.667
1	1	1	20.000

Table 3b. A8303-1 Output Voltage Selection

VSEL2	VSEL1	VSEL0	LNB (V)
1	1	1	11.667
0	0	0	13.333
0	0	1	13.667
0	1	0	14.333
0	1	1	15.667
1	0	0	18.667
1	0	1	19.000
1	1	0	19.667

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Status Registers (I²C™-Compatible Read Register)

The main fault conditions: overcurrent (OCP), and thermal shutdown (TSD) are all indicated by setting the relevant bits in the Status register. For these two fault cases, after the bit is set, it remains latched until the I²C™ master has successfully read the A8303 and A8303-1, assuming the fault has been resolved.

The undervoltage lockout (UVLO) bit indicates either V_{IN} is below V_{UVLO}, or V_{REG} is out of regulation. UVLO disables the LNB output and forces IRQ low. UVLO is a latched fault, and can only be cleared by performing an I²C™ READ cycle.

The Disable bit (DIS) indicates the status of the LNB output. The DIS is set when either a fault occurs (UVLO, OCP, TSD, or CPOK) or when the LNB output is turned off using the Enable bit (ENB) via the I²C™ interface. The DIS bit is latched and is only reset when there are no faults and the A8303 and A8303-1 output is turned back on using the Enable (ENB) bit via the I²C™ interface.

The Power Not Good (PNG), Charge Pump OK (CPOK), and Tone Detect (TDET) bits are set based on the conditions sensed at the LNB output, VCP, and Tone Detect Input (TDI) pins, respectively. These bits are not latched and, unlike the other fault bits, may become reset without an I²C™ read sequence. The PNG, CPOK, and TDET bits are continuously updated.

There are three methods to detect when the Status register changes: responding to the interrupt request (IRQ) pin going low, continuously polling the Status register via the I²C™ interface, or detecting a fault condition external to the A8303 and A8303-1 and performing a diagnostic poll of the A8303 and A8303-1. In any case, the master should read and re-read the Status register until the status changes.

Table 4. Status Register Description and IRQ Operation

Bit	Name	Function	Latched?	Reset Condition	Effect on IRQ Pin
0	DIS	LNB output disabled	Yes	LNB enabled and no faults	None
1	CPOK	Charge pump OK	No	$V_{CP} > V_{BOOST} + 5V$	None
2	OCP	Overcurrent	Yes	I²C™ READ and $I_{LOAD} < I_{SET}$	IRQ set low
3	TRIMS	Trim bits locked	Yes	None	None
4	PNG	Power Not Good	No	LNB voltage within range	None
5	TDET	Tone detect	No	Tone removed from LNB pin	None
6	TSD	Thermal shutdown	Yes	I²C™ READ and $T_J < 145°C$	IRQ set low
7	UVLO	VIN or VREG undervoltage	Yes	I²C™ READ and $V_{IN} > 9.0$ V	IRQ set low

Table 5. Status Register Bit Descriptions

Bit	Name	Description
0	DIS	The DIS bit is set to 1 when the A8303 and A8303-1 are disabled, (ENB = 0) or there is a fault: UVLO, OCP, CPOK, or TSD.
1	CPOK	If this bit is set low, the internal charge pump is not operating correctly (VCP). If the charge pump voltage is too low, the LNB output is disabled and the DIS bit is set.
2	OCP	This bit will be set to a 1 if the LNB output current exceeds the overcurrent threshold ($I_{OUT(MAX)}$) for more than the overcurrent disable time (t_{DIS}). If the OCP bit is set to 1, then the DIS bit is also set to 1.
3	TRIMS	Factory use only.
4	PNG	Set to 1 when the A8303 and A8303-1 are enabled and the LNB output voltage is either too low or too high (nominally ±9% from the LNB DAC setting). Set to 0 when the A8303 and A8303-1 are enabled and the LNB voltage is within the acceptable range (nominally ±5% from the LNB DAC setting).
5	TDET	The TDET bit is set to 1 if a tone is detected at the TDI pin that is within the specified voltage and frequency ranges. If TONECTRL = 1, the tone is being transmitted by the A8303 and A8303-1 and the tone detect low threshold is determined by $V_{TD(XMT)L}$. If TONECTRL I = 0, it is assumed the tone is being received from an external source and the tone detect low threshold is determined by $V_{TD(RCV)L}$.
6	TSD	The TSD bit is set to 1 if the A8303 and A8303-1 have detected an overtemperature condition. If the TSD bit is set to 1, then the DIS bit is also set to 1.
7	UVLO	The UVLO bit is set to 1 if either the voltage at the VIN pin or the voltage at the VREG pin is too low. If the UVLO bit is set to 1, then the DIS bit is also set to 1.

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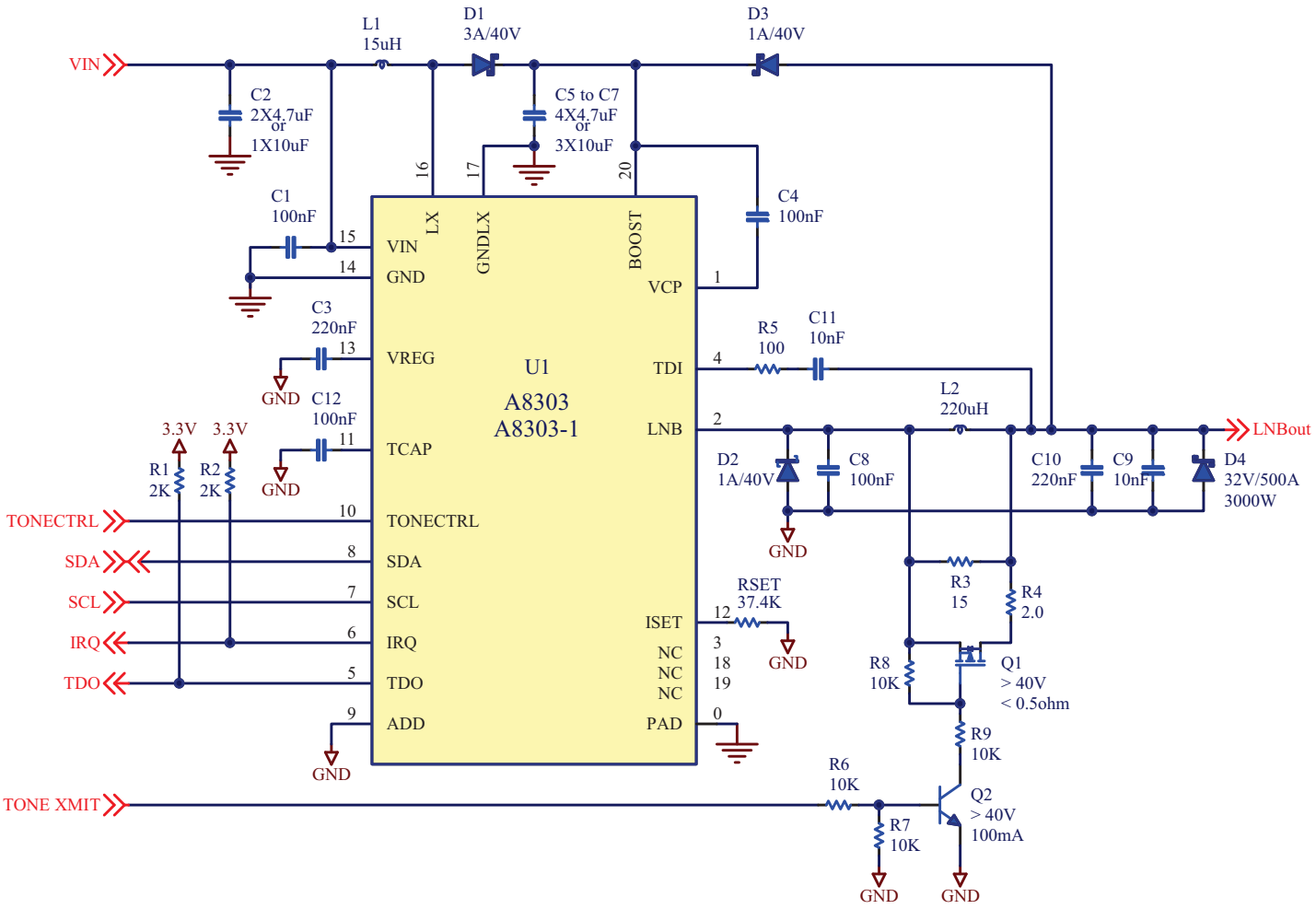
APPLICATION INFORMATION



See next page for bill of materials

Schematic 1. DiSEqC 2.0 Applications, 12 V_{IN} ±10%, 700 mA I_{OUT}, surge of ±1000 V, 2 Ω, 1.2/50 µs – 8/20 µs combination wave

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Table 6. Component Selection Table

Component	Characteristics	Recommended Devices
C1, C4, C8, C12	100 nF, 50 V, X5R or X7R, 0603	
C2	2X: 4.7 µF or 1X 10 µF, 25 V, X5R or X7R, 1206	
C3	220 nF, 10 V (min.) , X5R or X7R, 0603	
C5, C6, C7	4X: 4.7 µF, ±10%, 50 V, X7R, 1210 or 3X: 10 µF, ±10%, 35 V, X7R, 1210	4.7 µF: Murata: GRM32ER71H475KA88 Taiyo Yuden: UMK325B7475KM AVX: 12105C475KAT2A 10 µF: Murata: GRM32ER7YA106K
C9, C11	10 nF, 50 V, X5R or X7R, 0603	
C10	220 nF, 50 V, X5R or X7R, 0603	
D1	Schottky diode, 3 A, 40 V, SMA	Sanken: SFPB-74 Vishay: B340A-E3/5AT Diodes, Inc.: B340A-13-F Central Semiconductor: CMSH3-40MA
D2, D3	Schottky diode, 1 A, 40 V, SOD-123	Diodes, Inc.: B140HW-7 Central Semiconductor: CMMSH1-40
D4	TVS, 20 VRM, 32 VCL at 500 A, 3000 W	Littelfuse: SMDJ20A ST: LNBTVS6-221S
L1	15 µH, ±20%, I_{SAT} ≥ 3.1 A, DCR < 75 mΩ	Cooper Bussmann: DR1040-150-R TDK: VLF10045T-150M3R5 Sumida: CDRH10D43FBNP-150M
L2	220 µH, ±20%, I_{SAT} ≥ 800 mA, DCR < 0.8 Ω	Cooper Bussmann: DR1040-221-R TDK: VLF10045T-221MR90
Q1	MOSFET, P-channel, 50 V, < 0.5 Ω, SOT-23	Vishay: SI2309DS-T1-E3 Diodes, Inc.: ZXMP6A13FTA
Q2	Transistor, NPN, 50 V, 100 mA, SOT-323	Diodes, Inc.: BC846AW-7-F NXP: BC846W ON Semiconductor: BC846AWT1G
R1, R2	Resistor, 2 kΩ, 1%, 0402 or 0603	
R3	Resistor, 15 Ω, 1%, 0402 or 0603	
R4	Resistor, 2.0 Ω, 1%, 0402 or 0603	
R5	Resistor, 100 Ω, 1%, 0402 or 0603	
R6, R7, R8, R9	Resistor, 10 kΩ, 1%, 0402 or 0603	
RSET	Resistor, 37.4 kΩ, 1%, 0402 or 0603	

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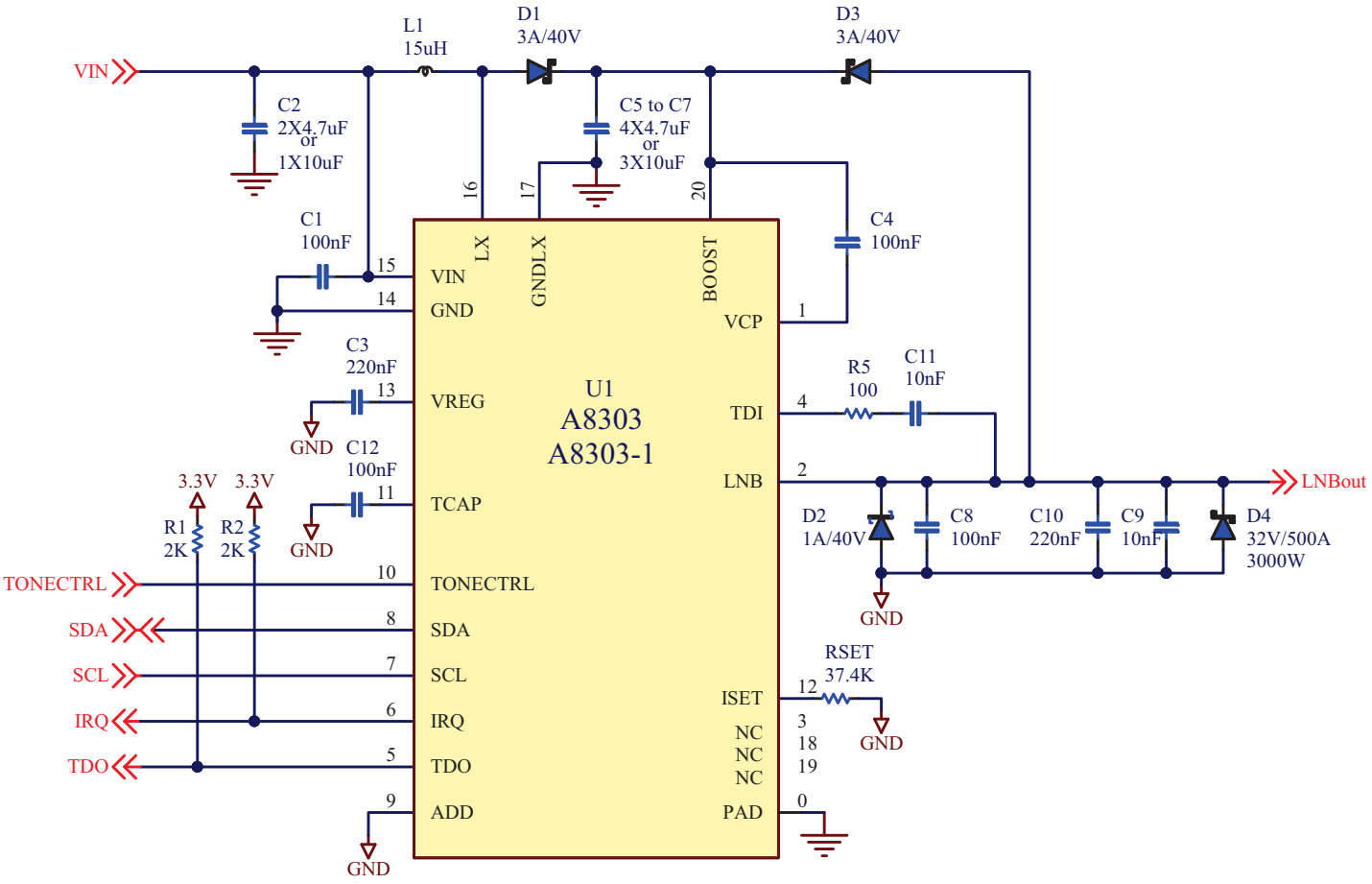

Schematic 2. DiSEqC 1.0 Applications, 12 V_{IN} ±10%, 700 mA I_{OUT}, surge of ±1000 V, 2 Ω, 1.2/50 µs – 8/20 µs combination wave

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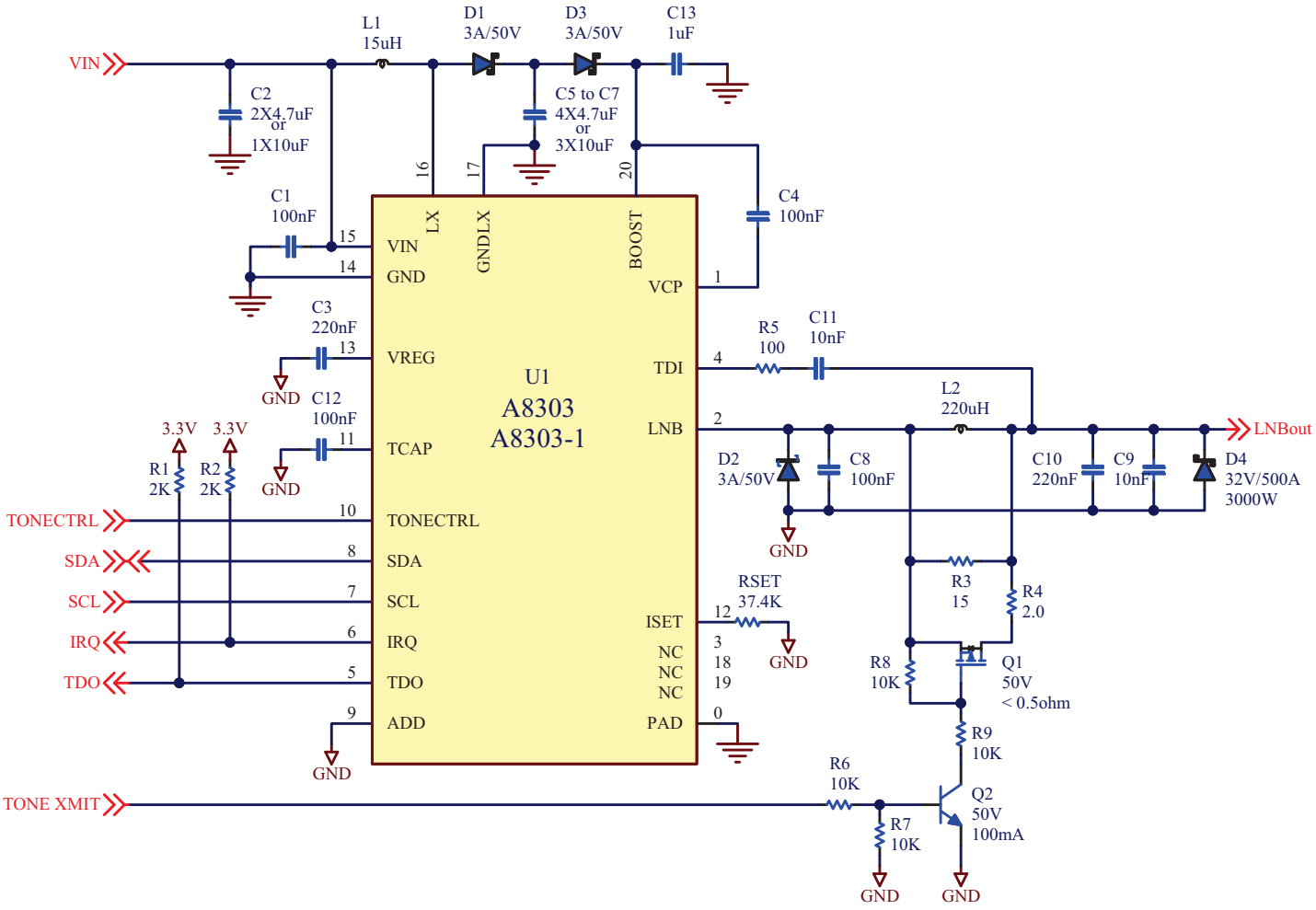

Schematic 3. DiSEqC 2.0 Applications for increased surge requirements ±1000 V, 2 Ω, 1.2/50 µs – 8/20 µs combination wave, and “stress to TVS failure” (or ±4000 V) test

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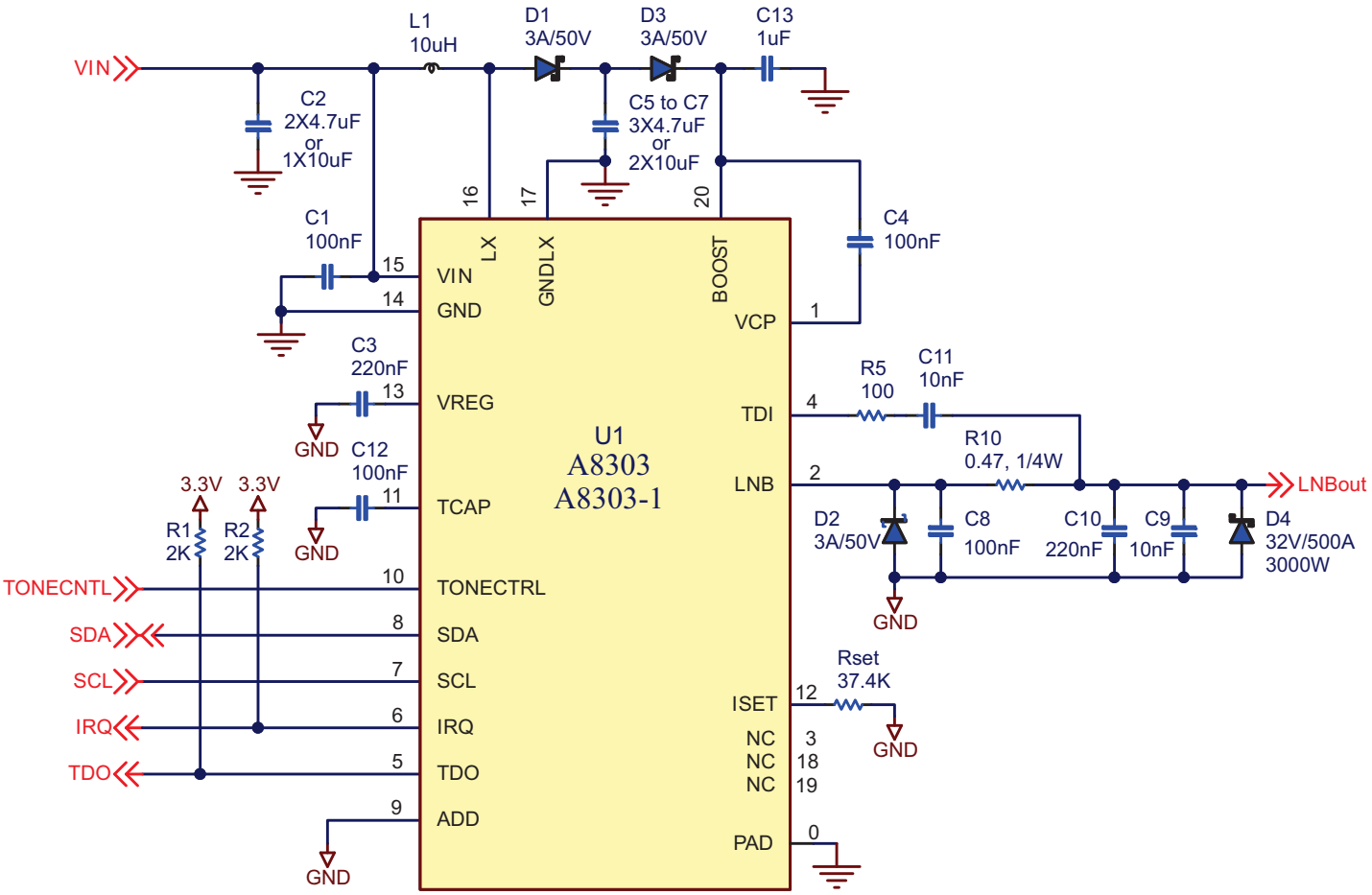

Schematic 4. DiSEqC 1.0 Applications for increased surge requirements ±1000 V, 2 Ω, 1.2/50 µs – 8/20 µs combination wave, and “stress to TVS failure” (or ±4000 V) test

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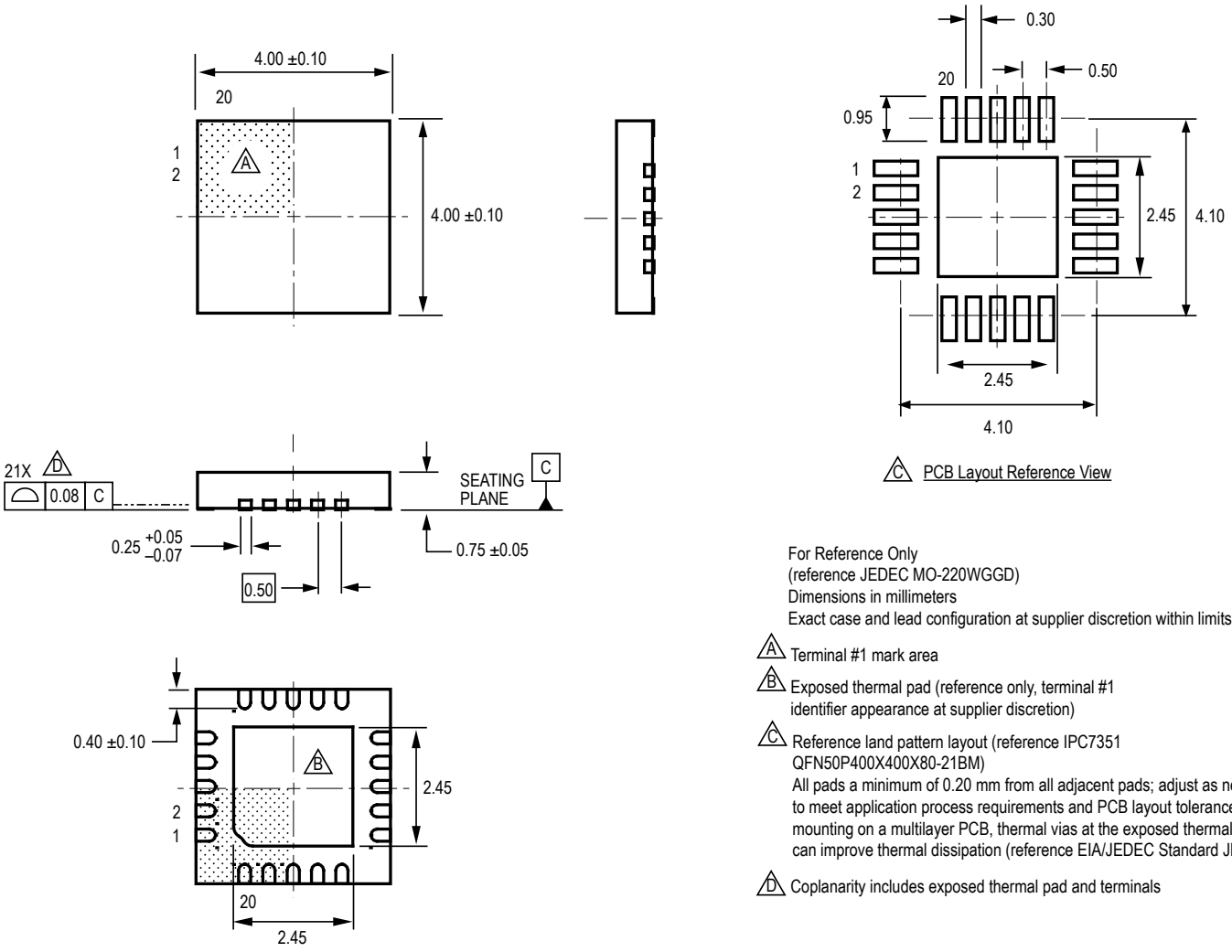
PACKAGE OUTLINE DRAWING



For Reference Only
(reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package ES 20-Pin MLP/QFN

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Revision History

Number	Date	Description
5	January 11, 2016	Corrected Terminal List Table (page 3)
6	July 22, 2016	Updated Component Selection Table (page 22)
7	January 11, 2018	Minor editorial updates
8	January 22, 2019	Minor editorial updates
9	February 8, 2019	Product status changed to Pre-End-of-Life
10	July 1, 2019	Product status changed to Last Time Buy
11	July 14, 2020	Product status changed to Discontinued

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