

This IC incorporates a general purpose analog circuit in a small package.

The S-89713 Series is an auto-zero operation, zero-drift operational amplifier that has input and output of low input offset voltage and Rail-to-Rail. The S-89713 Series is suitable for applications requiring less offset voltage.

The S-89713 Series is a dual operational amplifier (with 2 circuits).

## ■ Features

- Low input offset voltage:  $V_{IO} = 10 \mu\text{V max. (Ta = +25}^\circ\text{C)}$
- Operation power supply voltage range:  $V_{DD} = 2.65 \text{ V to } 5.50 \text{ V}$
- Low current consumption:  $I_{DD} = 165 \mu\text{A typ. (Per circuit, Ta = +25}^\circ\text{C)}$   
 $I_{DD} = 330 \mu\text{A typ. (2 circuits, Ta = +25}^\circ\text{C)}$
- Internal phase compensation: No external parts required
- Rail-to-Rail input and output
- Operation temperature range:  $T_a = -40^\circ\text{C to } +85^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free

## ■ Applications

- Various sensor interfaces
- High-accuracy current detection
- Strain gauge amplifier
- Game
- Various electric devices

## ■ Packages

- TMSOP-8
- SNT-8A

■ Block Diagram

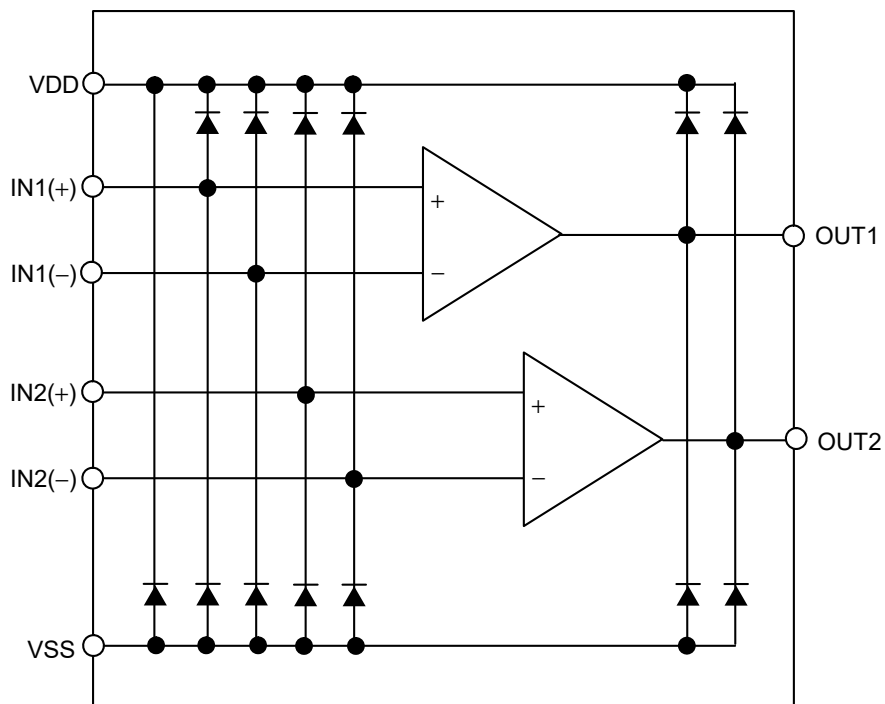
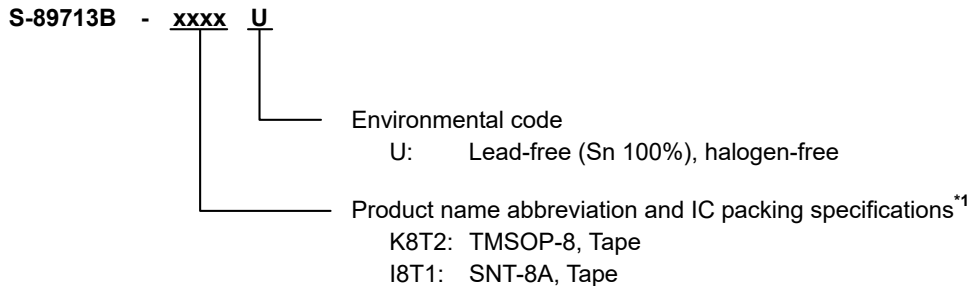


Figure 1

■ **Product Name Structure**

Users can select the package type for the S-89713 Series. Refer to "1. **Product name**" regarding the contents of product name, "2. **Packages**" regarding the package drawings and "3. **Product name list**" regarding the product type.

1. **Product name**



\*1. Refer to the tape drawing.

2. **Packages**

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	—
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

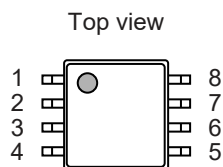
3. **Product name list**

Table 2

Product Name	Package
S-89713B-K8T2U	TMSOP-8
S-89713B-I8T1U	SNT-8A

■ **Pin Configurations**

**1. TMSOP-8**

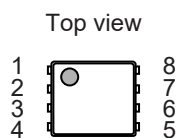


**Figure 2**

**Table 3**

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(-)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(-)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

**2. SNT-8A**



**Figure 3**

**Table 4**

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(-)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(-)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit	
Power supply voltage	V <sub>DD</sub>	V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 7.0	V	
Input voltage	V <sub>IN(+)</sub> , V <sub>IN(-)</sub>	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V	
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3	V	
Differential input voltage	V <sub>IND</sub>	±5.5	V	
Output pin current	I <sub>SOURCE</sub>	10.0	mA	
	I <sub>SINK</sub>	10.0	mA	
Power dissipation	TMSOP-8	P <sub>D</sub>	650*1	mW
	SNT-8A		450*1	mW
Operation ambient temperature	T <sub>opr</sub>	-40 to +85	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	

\*1. When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name: JEDEC STANDARD51-7

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

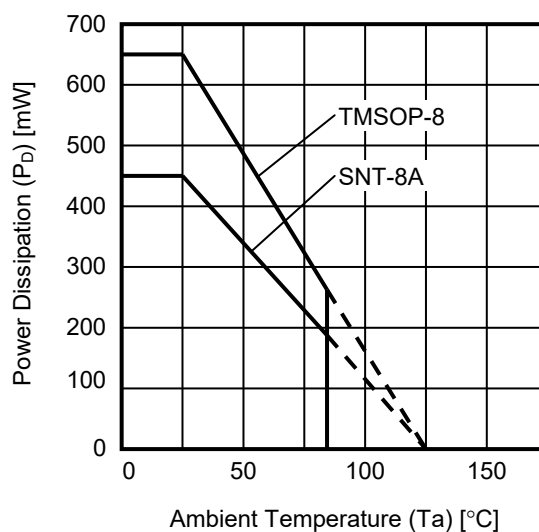


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

**Table 6**

**DC Electrical Characteristics** ( $V_{DD} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation power supply voltage range	$V_{DD}$	–	2.65	3.00	5.50	V	–
Current consumption (for 2 circuits)	$I_{DD}$	$V_{CMR} = V_{OUT} = V_{DD} / 2$	–	330	380	$\mu\text{A}$	5
Input offset voltage	$V_{IO}$	$V_{CMR} = V_{DD} / 2$	–10	$\pm 1$	+10	$\mu\text{V}$	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta T_a}$	$V_{CMR} = V_{DD} / 2$	–	$\pm 0.1$	–	$\mu\text{V}/^\circ\text{C}$	1
Input offset current	$I_{IO}$	–	–	$\pm 140$	–	pA	–
Input bias current	$I_{BIAS}$	–	–	$\pm 70$	–	pA	–
Common-mode input voltage range	$V_{CMR}$	–	$V_{SS} - 0.1$	–	$V_{DD} + 0.1$	V	2
Voltage gain (open loop)	$A_{VOL}$	$V_{SS} + 0.1\text{ V} \leq V_{OUT} \leq V_{DD} - 0.1\text{ V}$ , $V_{CMR} = V_{DD} / 2$ , $R_L = 10\text{ k}\Omega$	110	130	–	dB	8
Maximum output swing voltage	$V_{OH}$	$R_L = 10\text{ k}\Omega$	2.9	–	–	V	3
	$V_{OL}$	$R_L = 10\text{ k}\Omega$	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{SS} - 0.1\text{ V} \leq V_{CMR} \leq V_{DD} + 0.1\text{ V}$	106	130	–	dB	2
Power supply voltage rejection ratio	PSRR	$V_{DD} = 2.65\text{ V to } 5.50\text{ V}$	106	120	–	dB	1
Source current	$I_{SOURCE}$	$V_{OUT} = V_{DD} - 0.1\text{ V}$	1.3	1.6	–	mA	6
Sink current	$I_{SINK}$	$V_{OUT} = 0.1\text{ V}$	1.6	2.0	–	mA	7

**Table 7**

**AC Electrical Characteristics** ( $V_{DD} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Slew rate	SR	$R_L = 1.0\text{ M}\Omega$ , $C_L = 15\text{ pF}$ (Refer to <b>Figure 13</b> )	–	0.16	–	$\text{V}/\mu\text{s}$
Gain-bandwidth product	GBP	$C_L = 0\text{ pF}$	–	240	–	kHz

■ Test Circuits (Per circuit)

1. Power supply voltage rejection ratio, input offset voltage

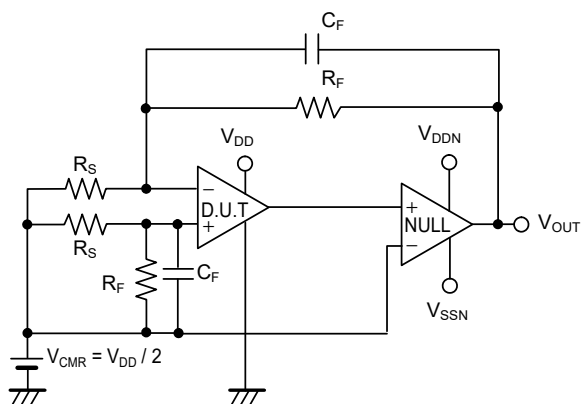


Figure 5 Test Circuit 1

• Power supply voltage rejection ratio (PSRR)

The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with  $V_{OUT}$  measured at each  $V_{DD}$ .

Test conditions:

$$V_{DD} = 2.65 \text{ V: } V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}$$

$$V_{DD} = 5.5 \text{ V: } V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}$$

$$PSRR = 20 \log \left( \left| \frac{V_{DD1} - V_{DD2}}{\left( V_{OUT1} - \frac{V_{DD1}}{2} \right) - \left( V_{OUT2} - \frac{V_{DD2}}{2} \right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• Input offset voltage ( $V_{IO}$ )

$$V_{IO} = \left( V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

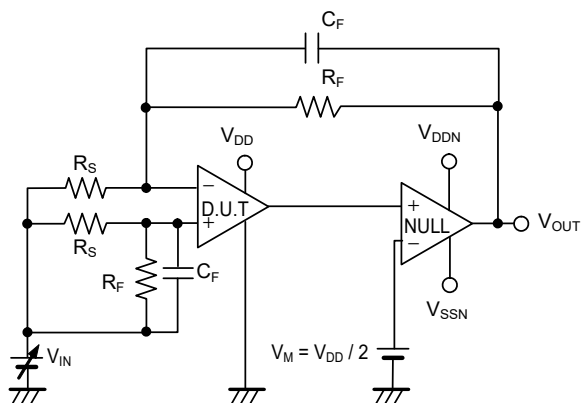


Figure 6 Test Circuit 2

• Common-mode input signal rejection ratio (CMRR)

The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with  $V_{OUT}$  measured at each  $V_{IN}$ .

Test conditions:

$$V_{IN} = V_{CMR \text{ Max.}}: V_{IN} = V_{IN1}, V_{OUT} = V_{OUT1}$$

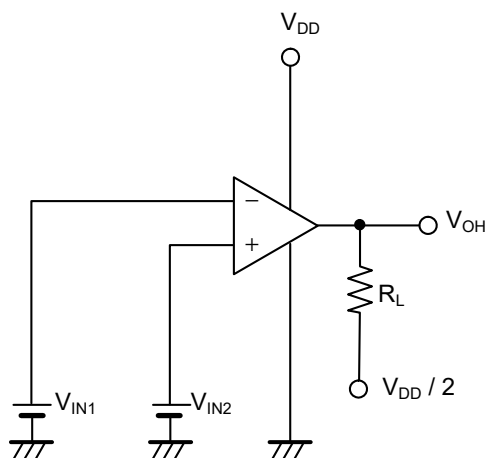
$$V_{IN} = V_{CMR \text{ Min.}}: V_{IN} = V_{IN2}, V_{OUT} = V_{OUT2}$$

$$CMRR = 20 \log \left( \left| \frac{V_{IN1} - V_{IN2}}{\left( V_{OUT1} - V_{IN1} \right) - \left( V_{OUT2} - V_{IN2} \right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

• Common-mode input voltage range ( $V_{CMR}$ )

The common-mode input voltage range is the range of  $V_{IN}$  in which  $V_{OUT}$  satisfies the common-mode input signal rejection ratio specifications.

**3. Maximum output swing voltage**



**Figure 7 Test Circuit 3**

• **Maximum output swing voltage ( $V_{OH}$ )**

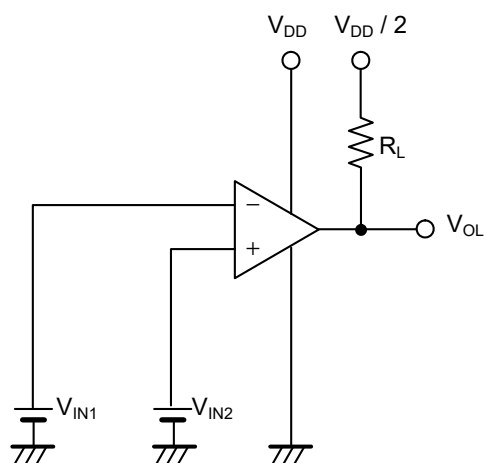
Test conditions:

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$R_L = 10 \text{ k}\Omega$$

**4. Maximum output swing voltage**



**Figure 8 Test Circuit 4**

• **Maximum output swing voltage ( $V_{OL}$ )**

Test conditions:

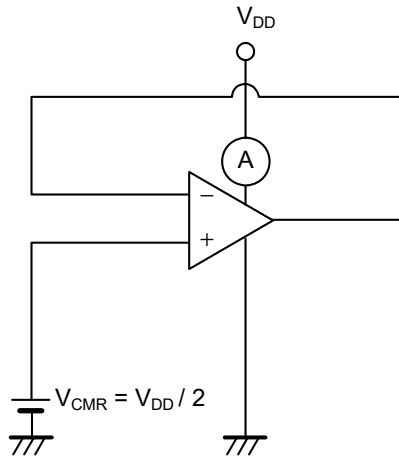
$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$R_L = 10 \text{ k}\Omega$$



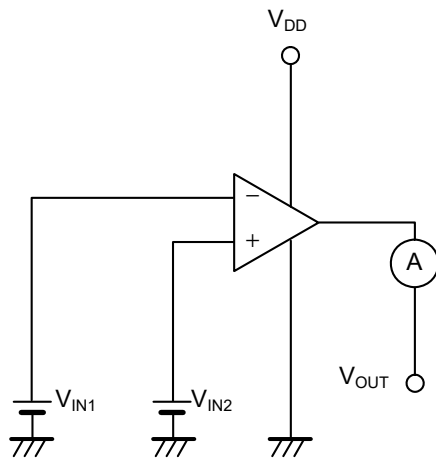
**5. Current consumption**



**Figure 9 Test Circuit 5**

- Current consumption ( $I_{DD}$ )

**6. Source current**



**Figure 10 Test Circuit 6**

- Source current ( $I_{SOURCE}$ )

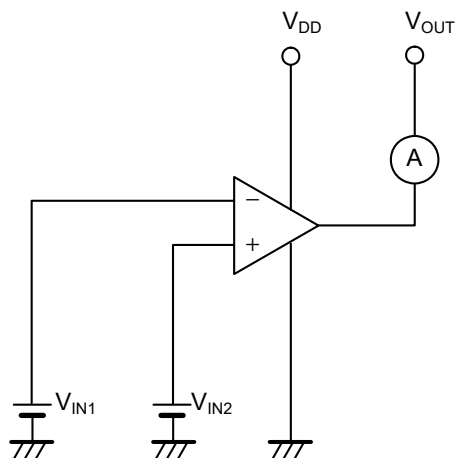
Test conditions:

$$V_{OUT} = V_{DD} - 0.1 \text{ V}$$

$$V_{IN1} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

**7. Sink current**



**Figure 11 Test Circuit 7**

- Sink current ( $I_{SINK}$ )

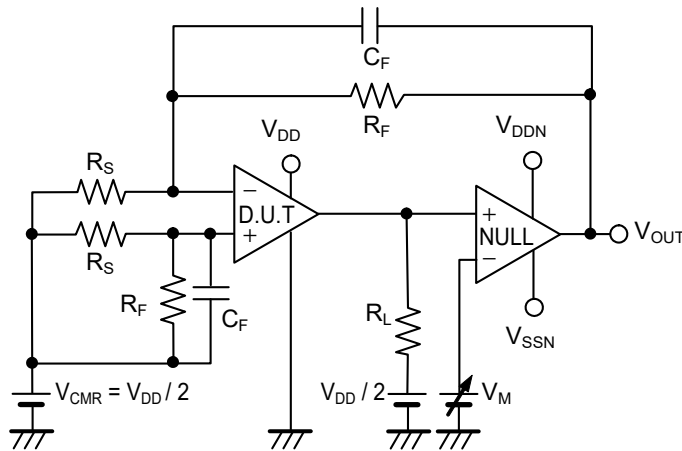
Test conditions:

$$V_{OUT} = 0.1 \text{ V}$$

$$V_{IN1} = \frac{V_{DD}}{2} + 0.1 \text{ V}$$

$$V_{IN2} = \frac{V_{DD}}{2} - 0.1 \text{ V}$$

**8. Voltage gain**



**Figure 12 Test Circuit 8**

• **Voltage gain (open loop) ( $A_{VOL}$ )**

The voltage gain ( $A_{VOL}$ ) can be calculated by the following expression, with  $V_{OUT}$  measured at each  $V_M$ .

Test conditions:

$$V_M = V_{DD} - 0.1 \text{ V: } V_M = V_{M1}, V_{OUT} = V_{OUT1}$$

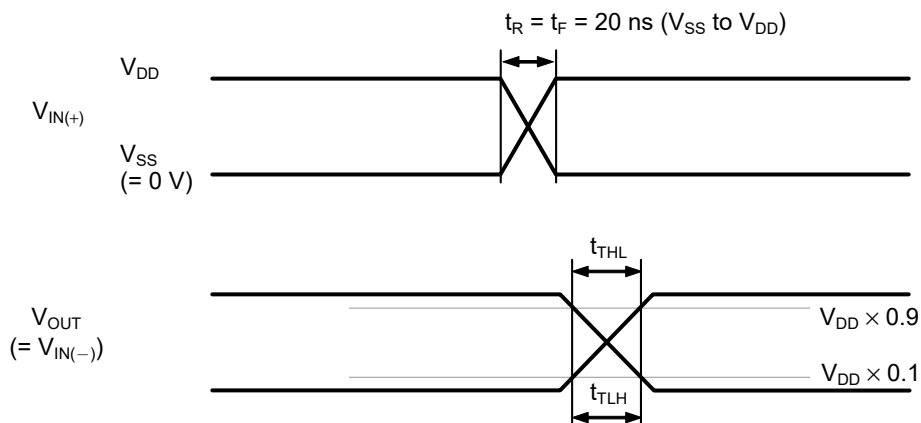
$$V_M = 0.1 \text{ V: } V_M = V_{M2}, V_{OUT} = V_{OUT2}$$

$$A_{VOL} = 20 \log \left( \left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

$$R_L = 10 \text{ k}\Omega$$

**9. Slew rate**

Measured by the voltage follower circuit.



**Figure 13**

• **Slew rate (SR)**

When falling

$$SR = \frac{V_{DD} \times 0.8}{t_{THL}}$$

When rising

$$SR = \frac{V_{DD} \times 0.8}{t_{TLH}}$$

■ Usage Example

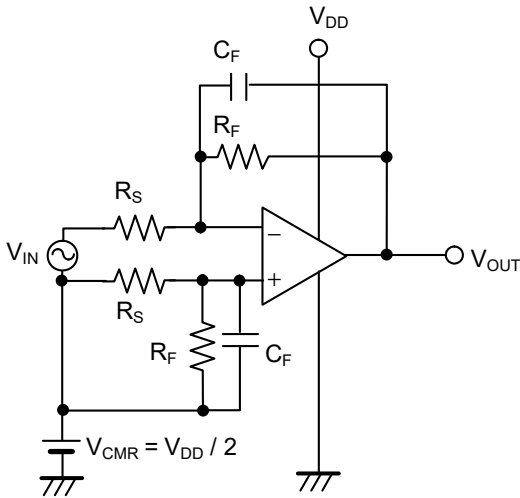


Figure 14 Differential Amplifier Circuit

[Example of Gain = 1000 times]

$R_S = 1 \text{ k}\Omega$   
 $R_F = 1 \text{ M}\Omega$   
 $C_F = 1000 \text{ pF}$

[Example of Gain = 100 times]

$R_S = 1 \text{ k}\Omega$   
 $R_F = 100 \text{ k}\Omega$   
 $C_F = 1000 \text{ pF}$

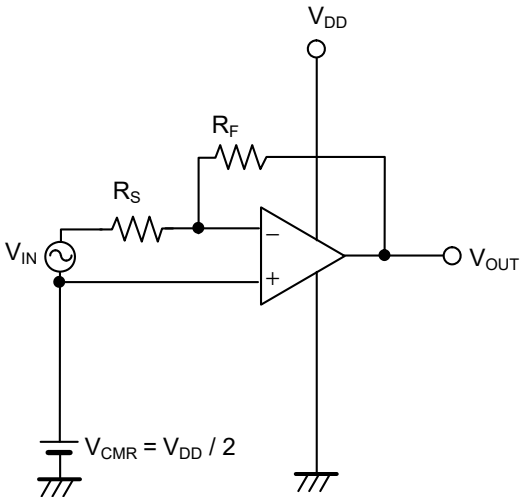


Figure 15 Inverting Amplifier Circuit

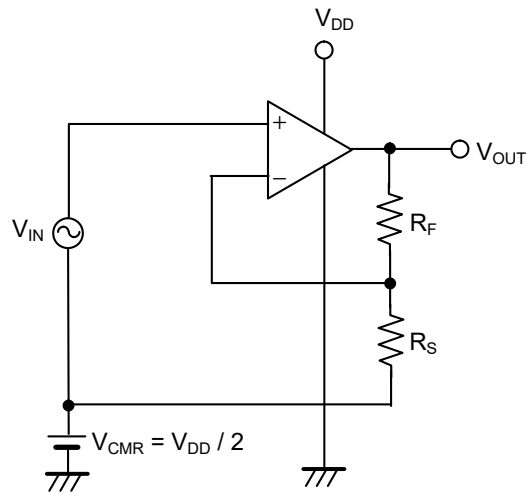


Figure 16 Non-inverting Amplifier Circuit

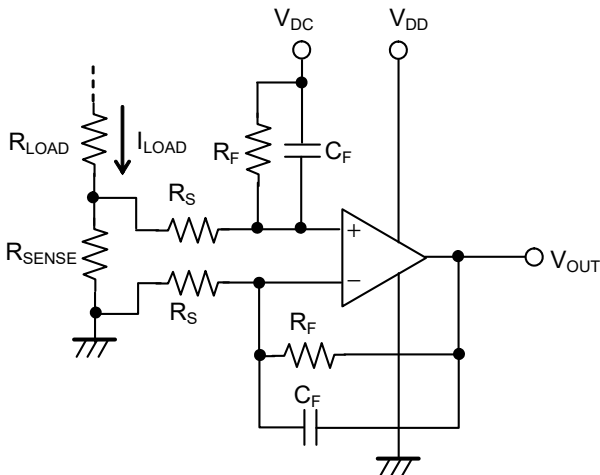


Figure 17 Low-side Current Detection Circuit

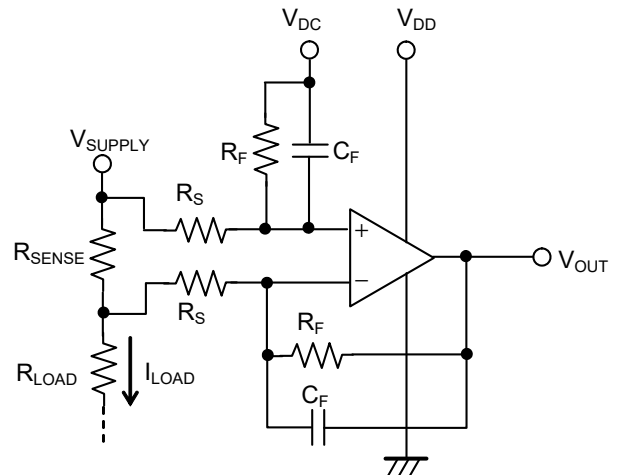
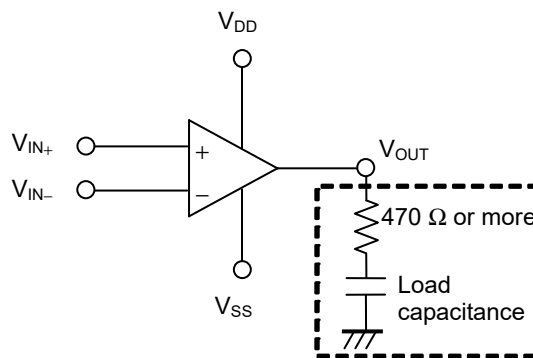


Figure 18 High-side Current Detection Circuit

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform through evaluation using the actual application to set the constant.

■ **Precautions**

- During the operation of an operational amplifier circuit, when  $V_{OUT} \leq V_{SS} + 100 \text{ mV}$  or  $V_{OUT} \geq V_{DD} - 100 \text{ mV}$ , the signal becomes difficult to be output, and the output voltage ( $V_{OUT}$ ) may become  $V_{SS}$  or  $V_{DD}$ . If this happens, supply an appropriate input signal to the operational amplifier so that  $V_{OUT}$  is within the range of  $V_{SS} + 100 \text{ mV}$  to  $V_{DD} - 100 \text{ mV}$ . Contact our sales representatives if you have any questions for use in the above operation conditions.
- Generally an operational amplifier may cause oscillation depending on the selection of external parts. Perform thorough evaluation using the actual application to set the constant.
- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
- Use this IC with the output current of 10 mA or less.
- When using the voltage follower circuit (Gain = 1 time), connect a resistor of 470  $\Omega$  or more for the stable operation, as shown in **Figure 19**. The operation may be unstable depending on the value of the load capacitance connected to the output pin, even when the voltage follower circuit is not used. Use the product under thorough evaluation.

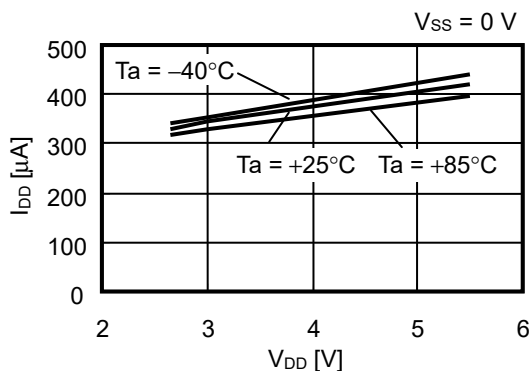


**Figure 19**

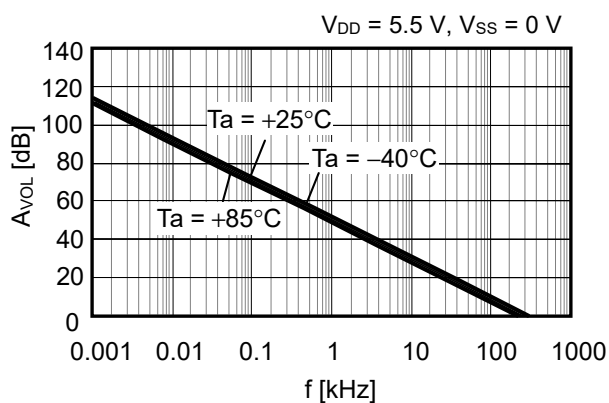
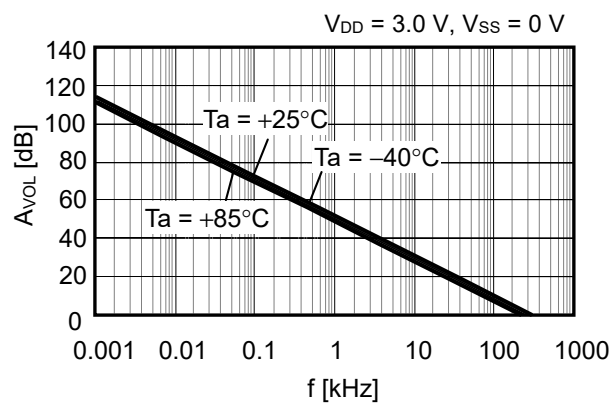
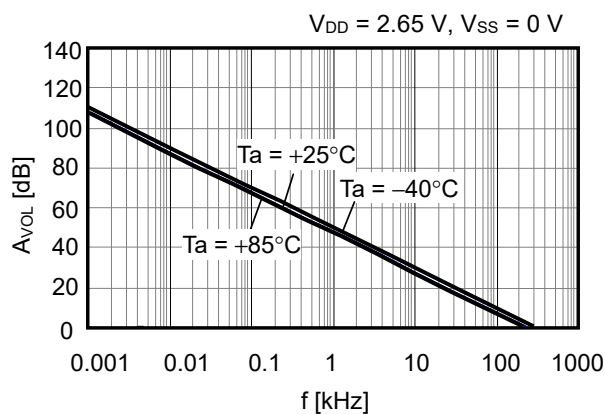
**Caution** The above connection diagram and constant will not guarantee successful operation. Perform through evaluation using the actual application to set the constant.

■ Characteristics (Typical Data)

1. Current consumption ( $I_{DD}$ ) (2 circuits) vs. Power supply voltage ( $V_{DD}$ )

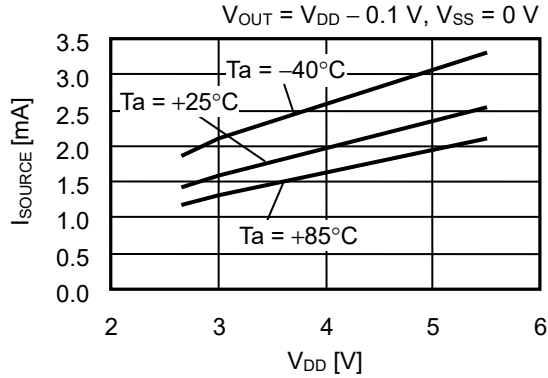


2. Voltage gain ( $A_{VOL}$ ) vs. Frequency ( $f$ )

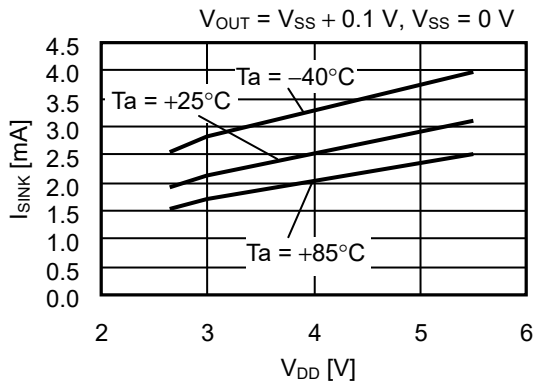


**3. Output current**

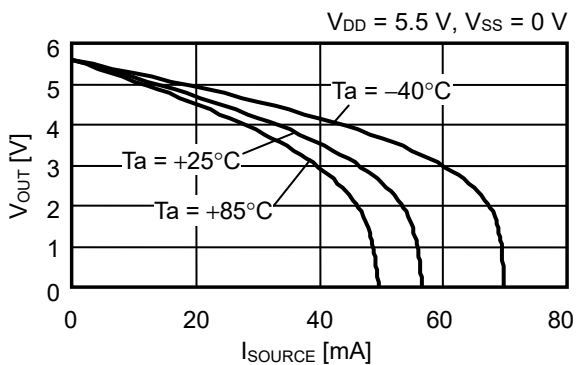
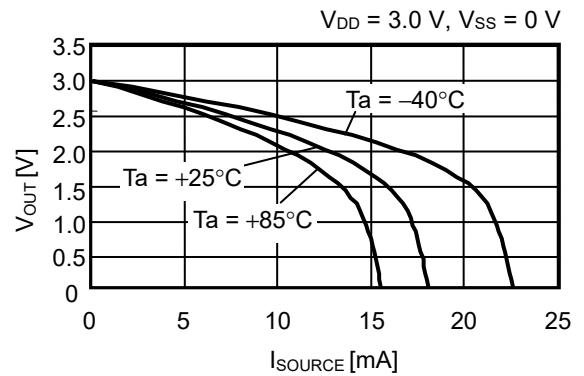
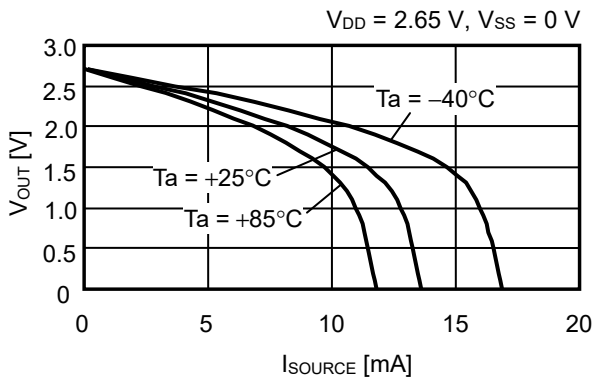
**3.1 Source current ( $I_{SOURCE}$ ) vs. Power supply voltage ( $V_{DD}$ )**



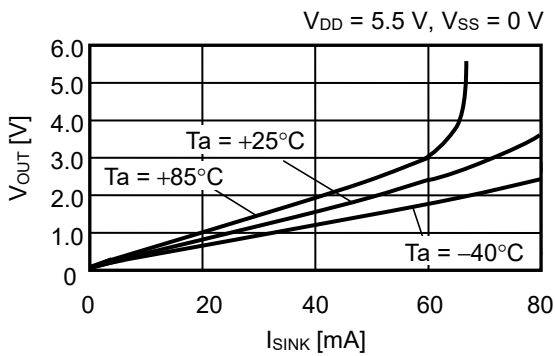
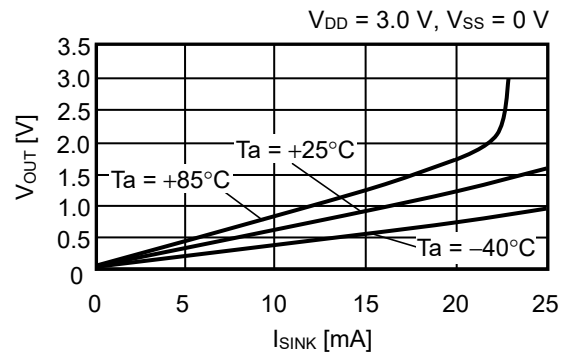
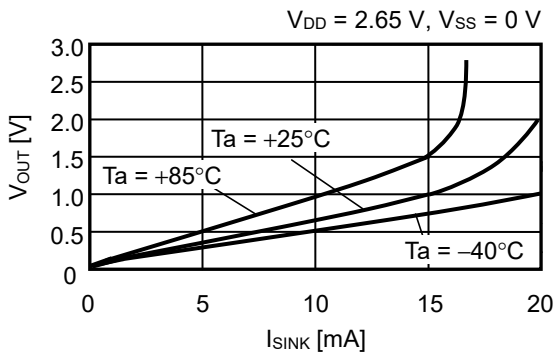
**3.2 Sink current ( $I_{SINK}$ ) vs. Power supply voltage ( $V_{DD}$ )**



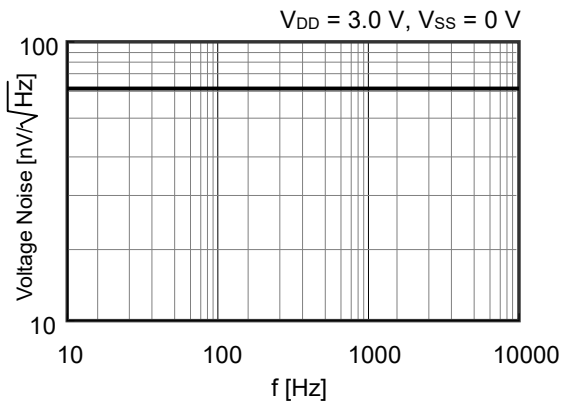
**3.3 Output voltage ( $V_{OUT}$ ) vs. Source current ( $I_{SOURCE}$ )**



3.4 Output voltage ( $V_{OUT}$ ) vs. Sink current ( $I_{SINK}$ )

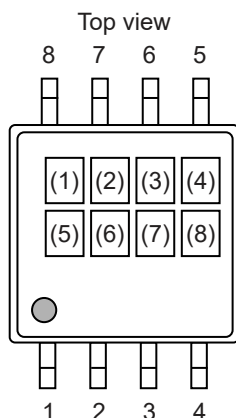


4. Input-referred noise voltage vs. Frequency (f)



■ **Marking Specifications**

**1. TMSOP-8**

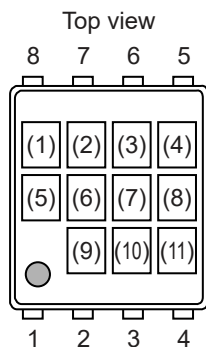


- (1): Blank
- (2) to (4): Product code (Refer to **Product name vs. Product code**)
- (5): Blank
- (6) to (8): Lot number

**Product name vs. Product code**

Product Name	Product Code		
	(2)	(3)	(4)
S-89713B-K8T2U	Z	Y	C

**2. SNT-8A**

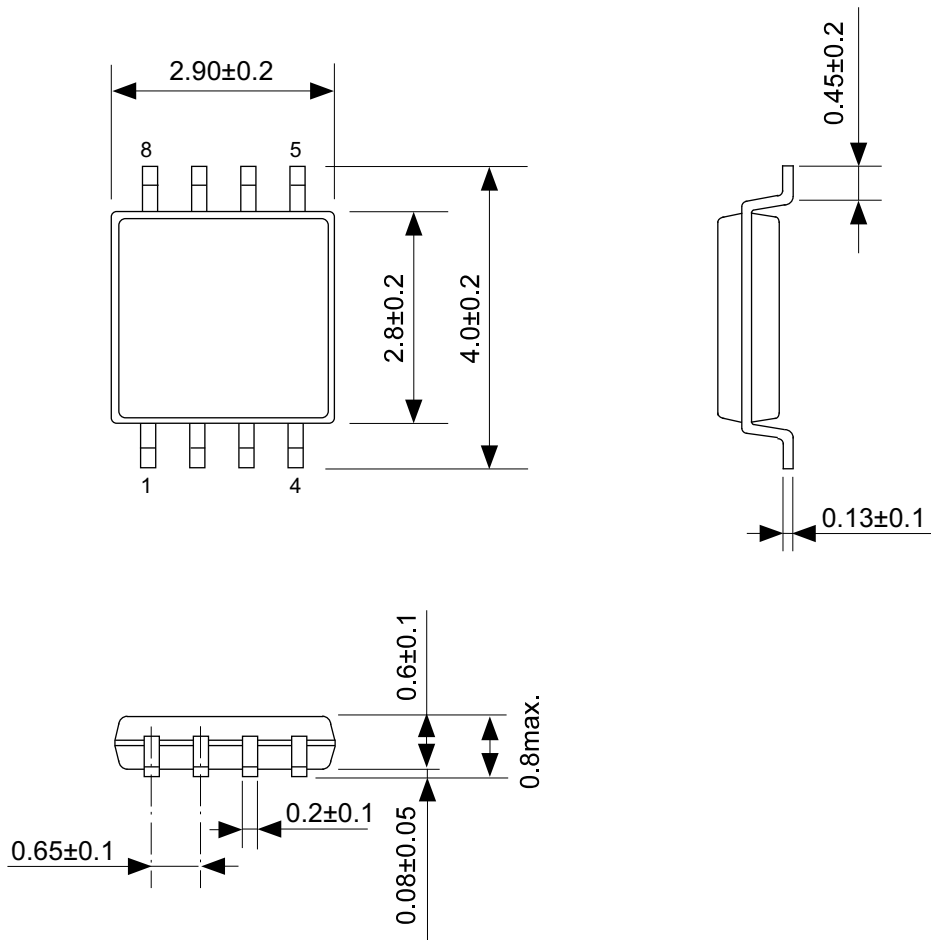


- (1): Blank
- (2) to (4): Product code (Refer to **Product name vs. Product code**)
- (5), (6): Blank
- (7) to (11): Lot number


**Product name vs. Product code**

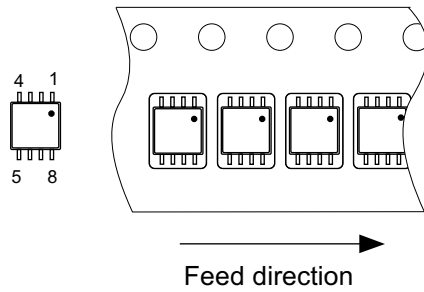
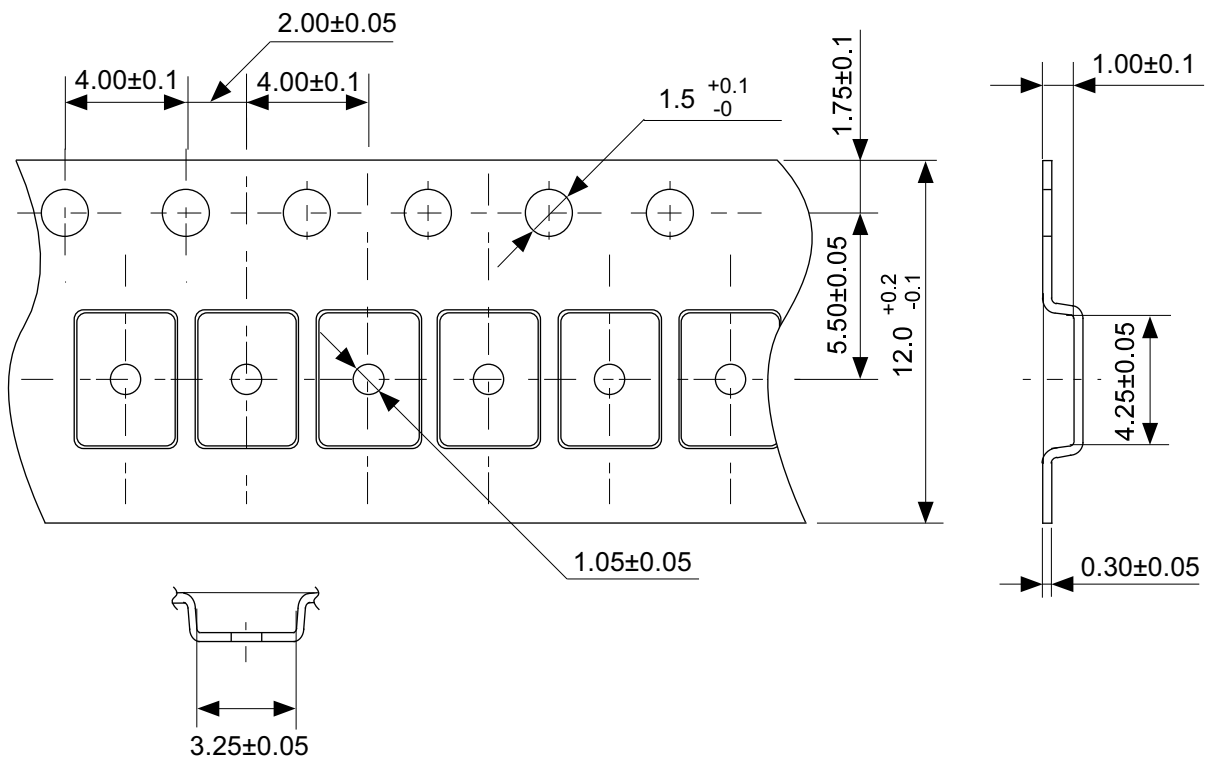
Product Name	Product Code		
	(2)	(3)	(4)
S-89713B-I8T1U	Z	Y	C





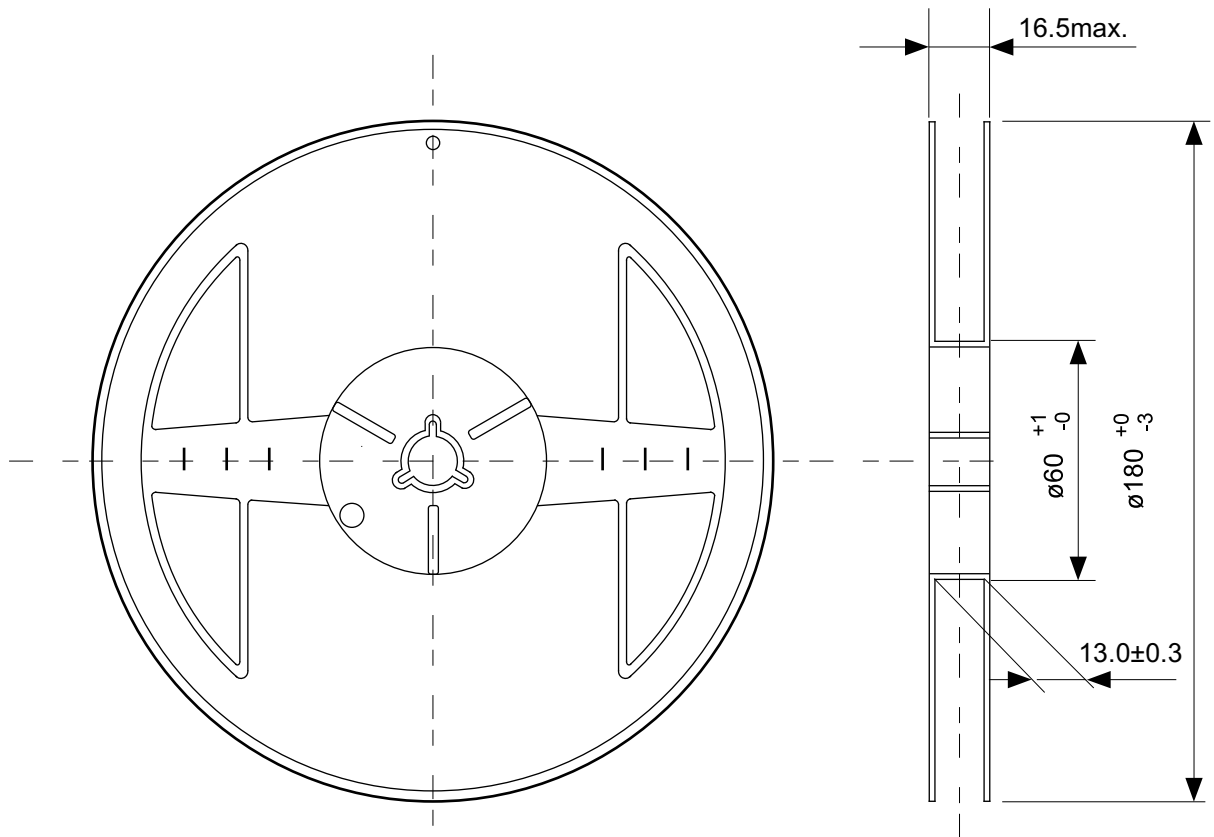
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

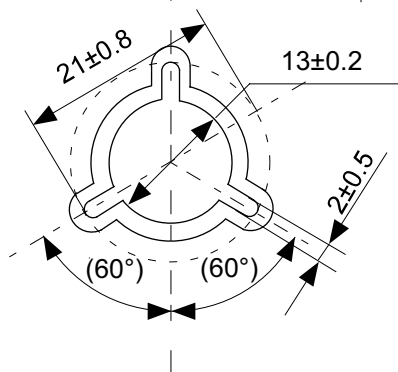


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

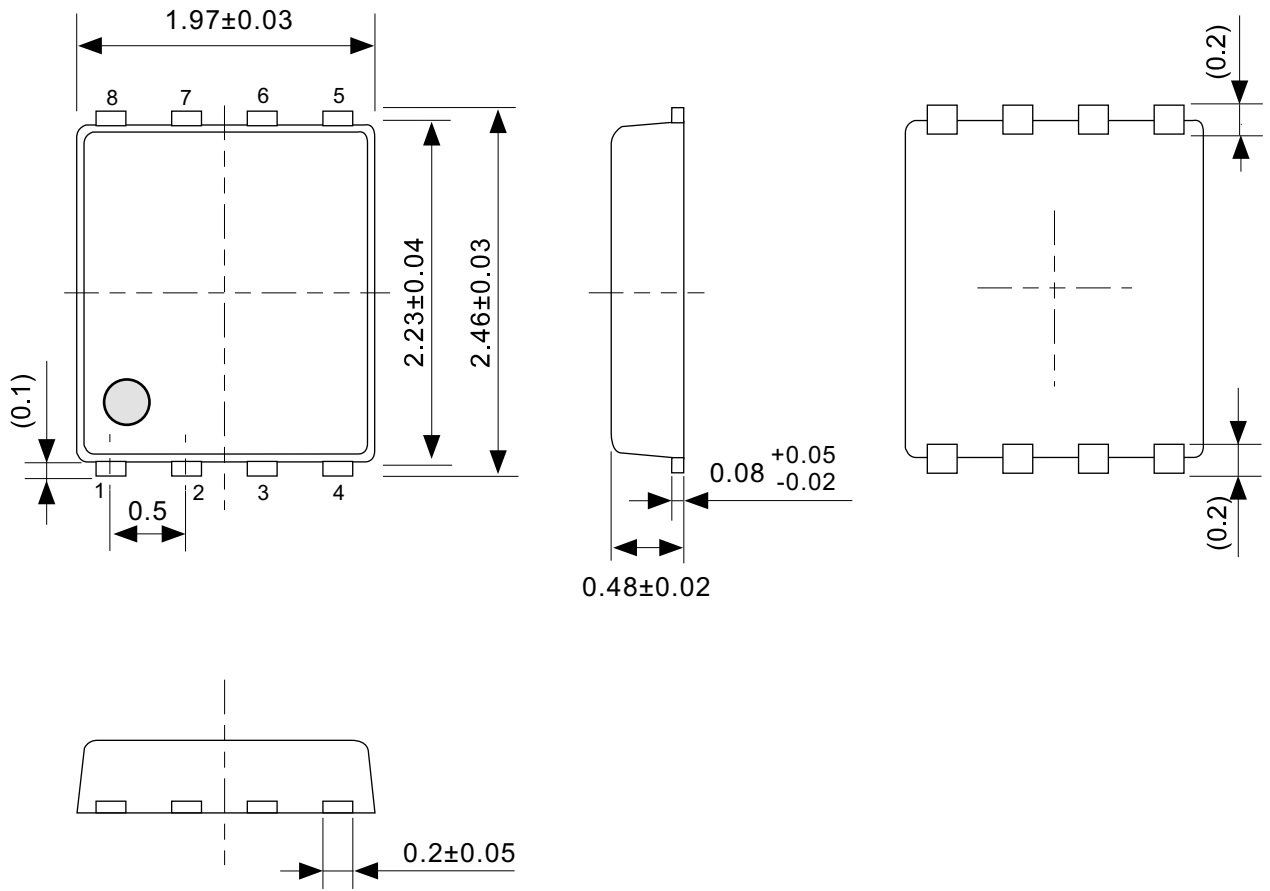


Enlarged drawing in the central part



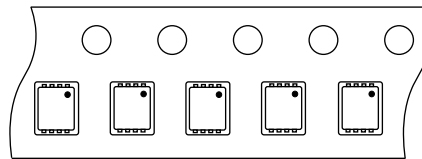
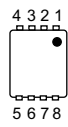
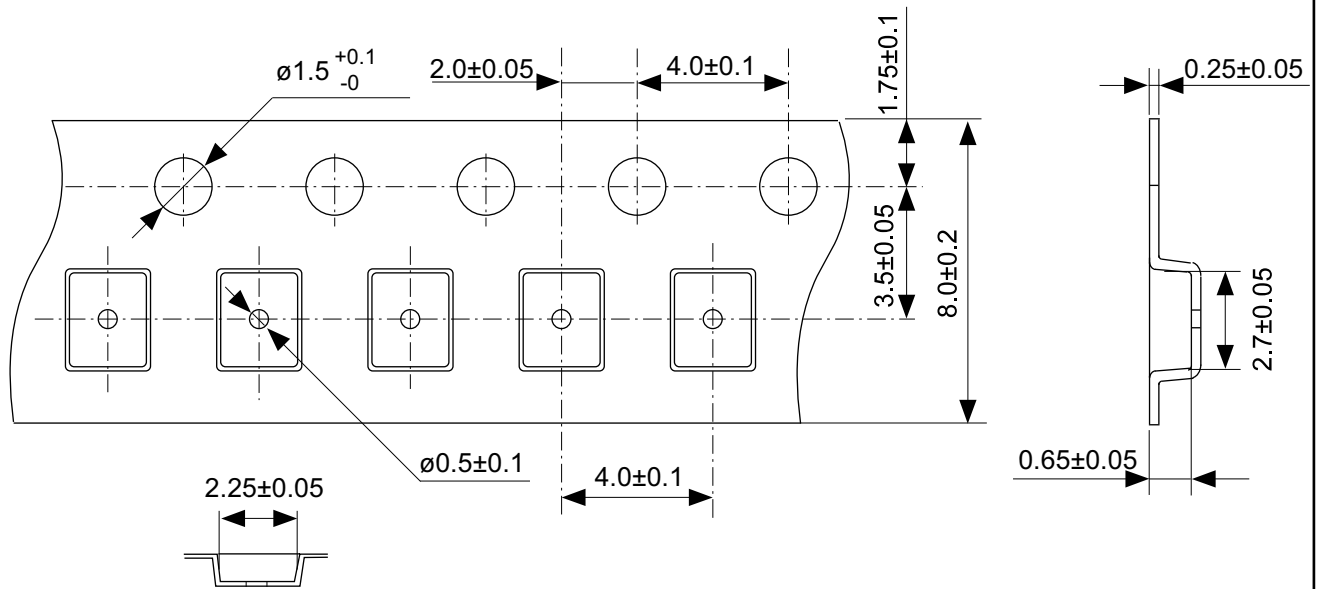
No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
<b>ABLIC Inc.</b>			



No. PH008-A-P-SD-2.1

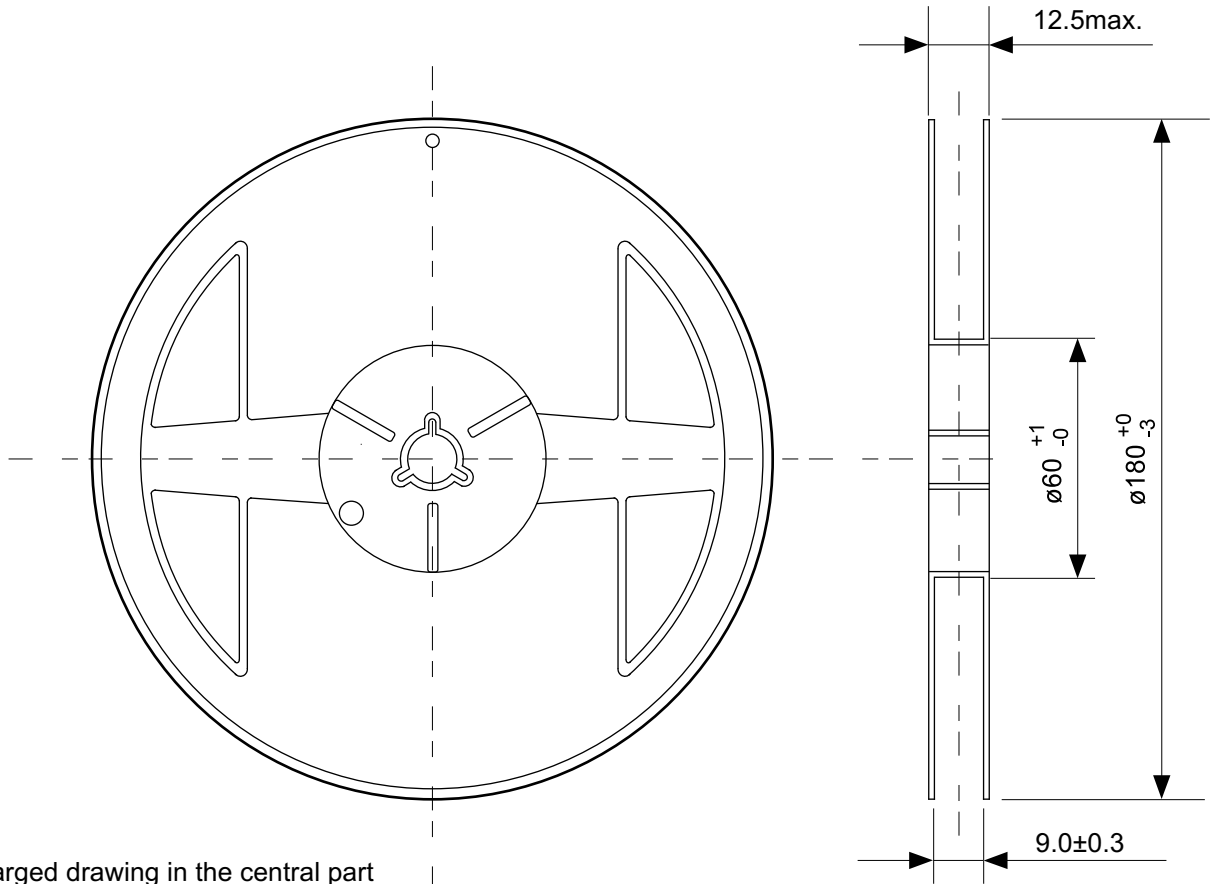
TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



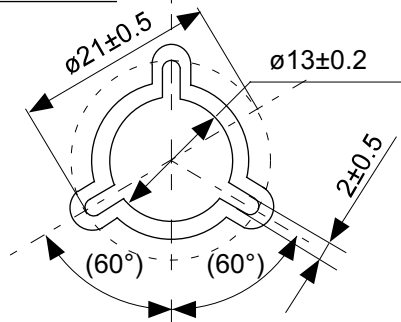
→  
Feed direction

No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

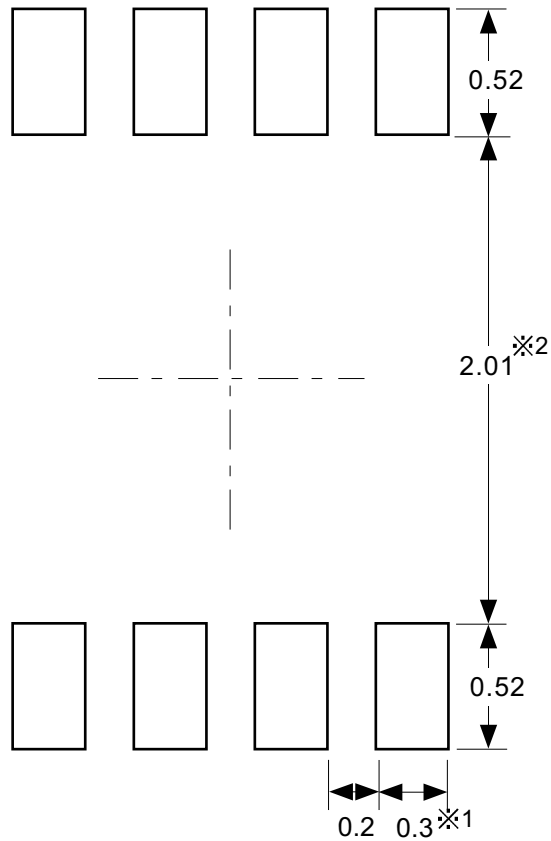


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
<b>ABLIC Inc.</b>			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).  
 ※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

- 注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
  2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
  3. マスク開口サイズと開口位置はランドパターンと合わせてください。
  4. 詳細は“SNTパッケージ活用の手引き”を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).  
 ※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

- Caution**
1. Do not do silkscreen printing and solder printing under the mold resin of the package.
  2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
  3. Match the mask aperture size and aperture position with the land pattern.
  4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).  
 ※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

- 注意
1. 请勿在树脂型封装的下面印刷丝网、焊锡。
  2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
  3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
  4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

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2.4-2019.07