

MOSFET – Dual N-Channel and Dual P-Channel, POWERTRENCH[®], GreenBridge™ Series of High-Efficiency Bridge Rectifiers

N-Channel: 100 V, 6 A, 110 mΩ
P-Channel: -80 V, -6 A, 190 mΩ

FDMQ8203

General Description

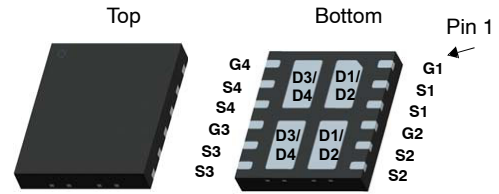
This quad mosfet solution provides ten-fold improvement in power dissipation over diode bridge.

Features

- Q1/Q4: N-Channel
 - ◆ Max $R_{DS(on)}$ = 110 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$
 - ◆ Max $R_{DS(on)}$ = 175 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 2.4\text{ A}$
- Q2/Q3: P-Channel
 - ◆ Max $R_{DS(on)}$ = 190 mΩ at $V_{GS} = -10\text{ V}$, $I_D = -2.3\text{ A}$
 - ◆ Max $R_{DS(on)}$ = 235 mΩ at $V_{GS} = -4.5\text{ V}$, $I_D = -2.1\text{ A}$

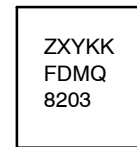
Applications

- High-Efficiency Bridge Rectifiers
- Substantial Efficiency Benefit in PD Solutions
- These Device is Pb-Free, Halide Free and is RoHS Compliant



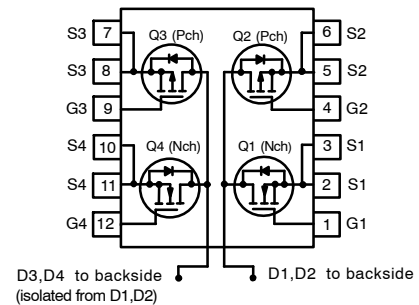
WDFN12 5x4.5, 0.8P
CASE 511CS

MARKING DIAGRAM



FDMQ8203 = Specific Device Code
Z = Assembly Plant Code
XY = Date Code
KK = Lot Run Traceability Code

N-Channel / P-Channel



ORDERING INFORMATION

Device	Package	Shipping [†]
FDMQ8203	MLP 4.5x5 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDMQ8203

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Q1/Q4	Q2/Q3	Unit	
V_{DS}	Drain to Source Voltage	100	-80	V	
V_{GS}	Gate to Source Voltage	± 20	± 20	V	
I_D	Drain Current	- Continuous (Package Limited) $T_C = 25^\circ\text{C}$	6	-6	A
		- Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	10	-10	
		- Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	3.4	-2.6	
		- Pulsed	12	-10	
P_D	Power Dissipation for Single Operation	$T_C = 25^\circ\text{C}$		W	
	Power Dissipation for Dual Operation	$T_A = 25^\circ\text{C}$ (Note 1a)			
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	160	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$ $I_D = -250 \mu\text{A}, V_{GS} = 0$	Q1/Q4 Q2/Q3	100 -80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C $I_D = -250 \mu\text{A}$, Referenced to 25°C	Q1/Q4 Q2/Q3	- -	72 -79	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = -64 \text{ V}, V_{GS} = 0 \text{ V}$	Q1/Q4 Q2/Q3	- -	-	1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1/Q4 Q2/Q3	- -	-	± 100 ± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	Q1/Q4 Q2/Q3	2 -1	3 -1.6	4 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C $I_D = -250 \mu\text{A}$, Referenced to 25°C	Q1/Q4 Q2/Q3	- -	-8 5	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$ $V_{GS} = 6 \text{ V}, I_D = 2.4 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}, T_J = 125^\circ\text{C}$	Q1/Q4	- - -	85 118 147	110 175 191	$\text{m}\Omega$
		$V_{GS} = -10 \text{ V}, I_D = -2.3 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -2.1 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -2.3 \text{ A}, T_J = 125^\circ\text{C}$	Q2/Q3	- - -	161 188 273	190 235 323	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$ $V_{DS} = -10 \text{ V}, I_D = -2.3 \text{ A}$	Q1/Q4 Q2/Q3	- -	6 6	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	Q1/Q4 $V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	Q1/Q4 Q2/Q3	- -	158 639	210 850	pF
C_{oss}	Output Capacitance	Q2/Q3 $V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	Q1/Q4 Q2/Q3	- -	41 46	55 65	pF
C_{rss}	Reverse Transfer Capacitance		Q1/Q4 Q2/Q3	- -	2.6 24	5 40	pF

FDMQ8203

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit	
SWITCHING CHARACTERISTICS (Note 2)								
t _{d(on)}	Turn-On Delay Time	Q1/Q4 V _{DD} = 50 V, I _D = 3 A, V _{GS} = 10 V, R _{GEN} = 6 Ω Q2/Q3 V _{DD} = -40 V, I _D = -2.3 A, V _{GS} = -10 V, R _{GEN} = 6 Ω	Q1/Q4	-	3.8	10	ns	
t _r	Rise Time		Q2/Q3	-	4.7	10	ns	
t _{d(off)}	Turn-Off Delay Time		Q1/Q4	-	1.3	10	ns	
t _f	Fall Time		Q2/Q3	-	2.8	10	ns	
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V V _{GS} = 0 V to -10 V V _{GS} = 0 V to 5 V V _{GS} = 0 V to -4.5 V	Q1/Q4: V _{DD} = 50 V, I _D = 3 A	Q1/Q4	-	2.9	5	nC
Q _g	Total Gate Charge		Q2/Q3: V _{DD} = -40 V, I _D = -2.3 A	Q2/Q3	-	13	19	nC
Q _{gs}	Gate-Source Gate Charge		Q1/Q4	-	1.6	3	nC	
Q _{gd}	Gate to Drain "Miller" Charge		Q2/Q3	-	6.4	10	nC	
				Q1/Q4	-	0.8	-	nC
				Q2/Q3	-	1.6	-	nC
				Q1/Q4	-	0.8	-	nC
				Q2/Q3	-	2.6	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drine Diode Forward Voltage	V _{GS} = 0 V, I _S = 3 A (Note 2) V _{GS} = 0 V, I _S = -2.3 A (Note 2)	Q1/Q4 Q2/Q3	-	0.86 -0.82	1.3 -1.3	V
t _{rr}	Reverse Recovery Time	Q1/Q4: I _F = 3 A, di/dt = 100 A/μs Q2/Q3: I _F = -2.3 A, di/dt = 100 A/μs	Q1/Q4 Q2/Q3	-	32 26	52 42	ns
Q _{rr}	Reverse Recovery Charge		Q1/Q4 Q2/Q3	-	21 26	34 42	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



- 50°C/W when mounted on a 1 in² pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.



- 160°C/W when mounted on a minimum pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS (N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

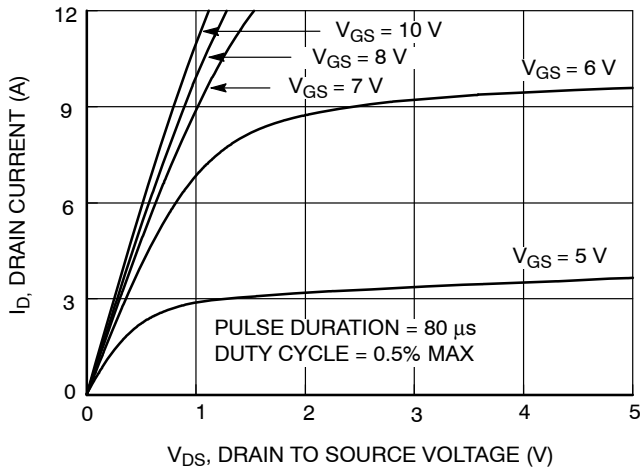


Figure 1. On Region Characteristics

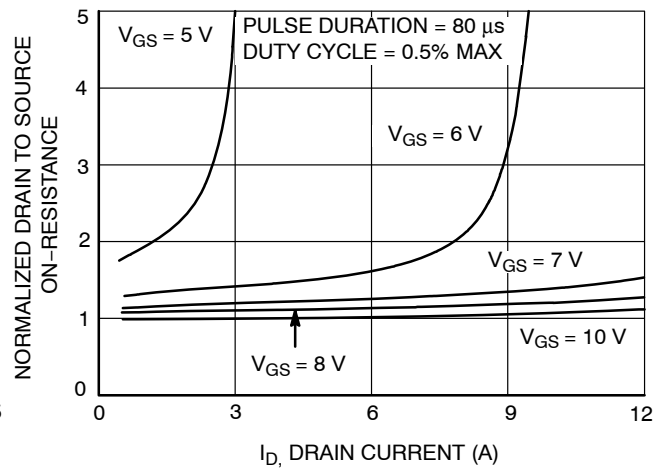


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

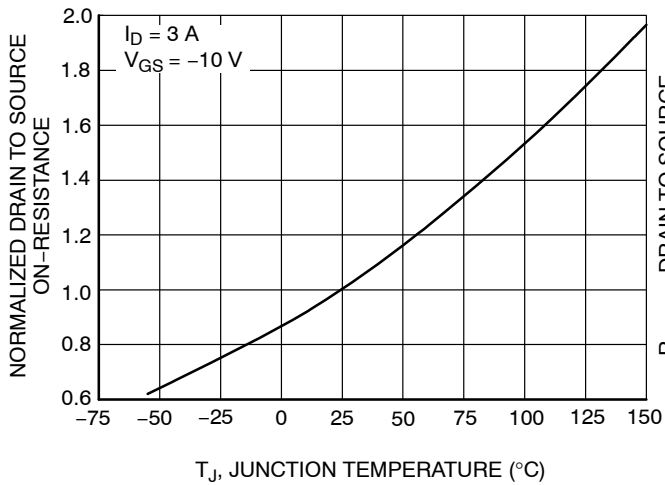


Figure 3. Normalized On Resistance vs Junction Temperature

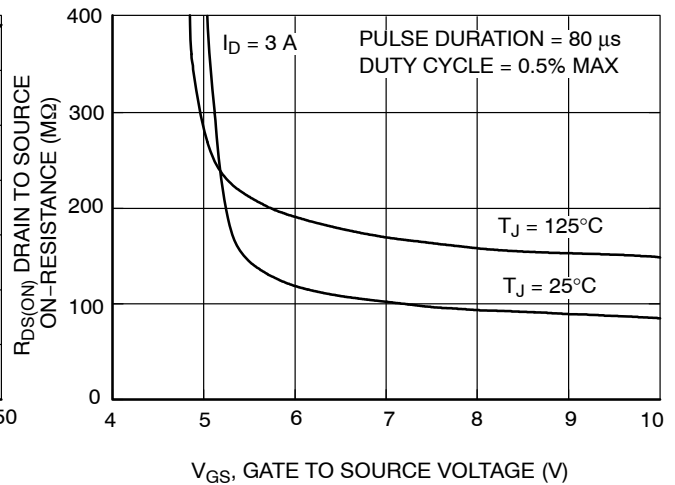


Figure 4. On-Resistance vs Gate to Source Voltage

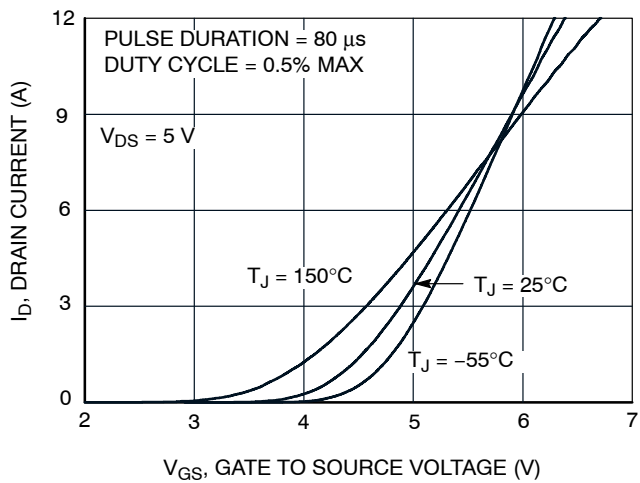


Figure 5. Transfer Characteristics

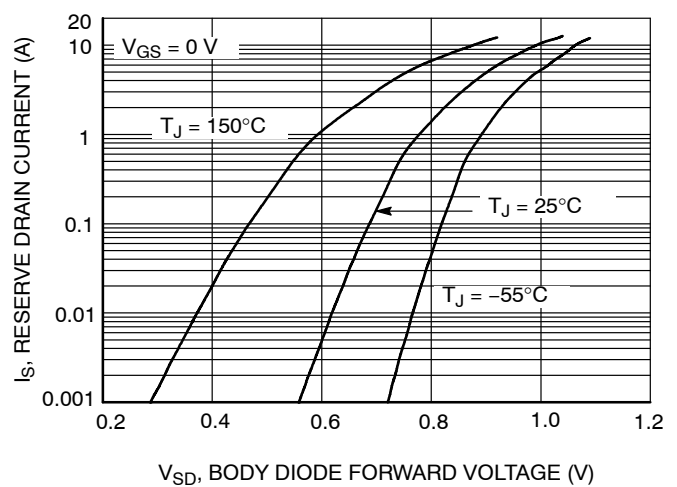


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

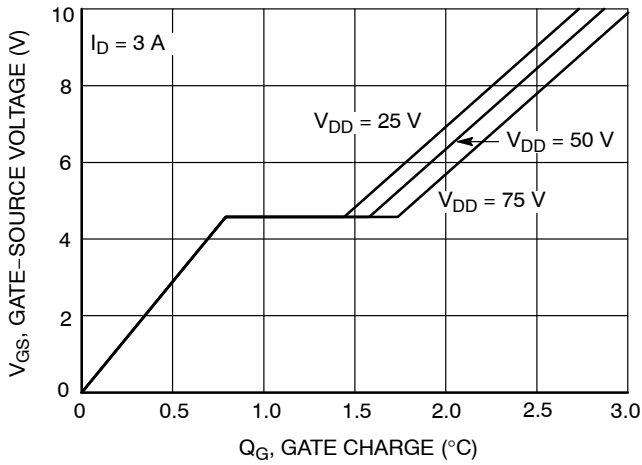


Figure 7. Gate Charge Characteristics

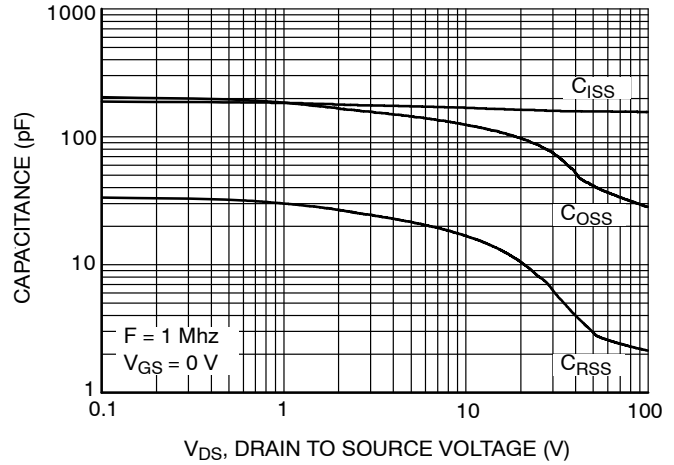


Figure 8. Capacitance vs Drain to Source Voltage

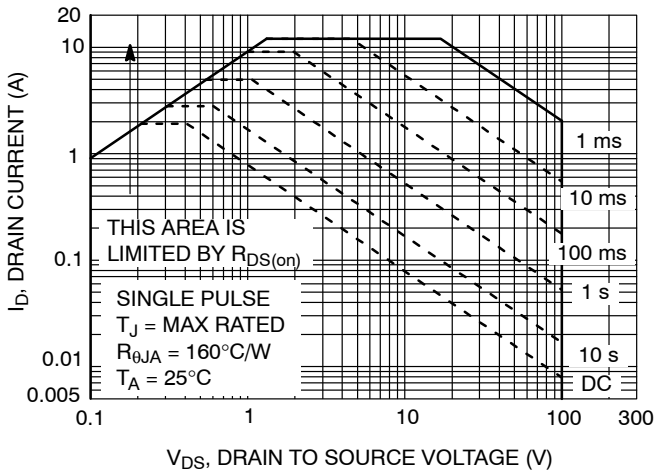


Figure 9. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS (P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

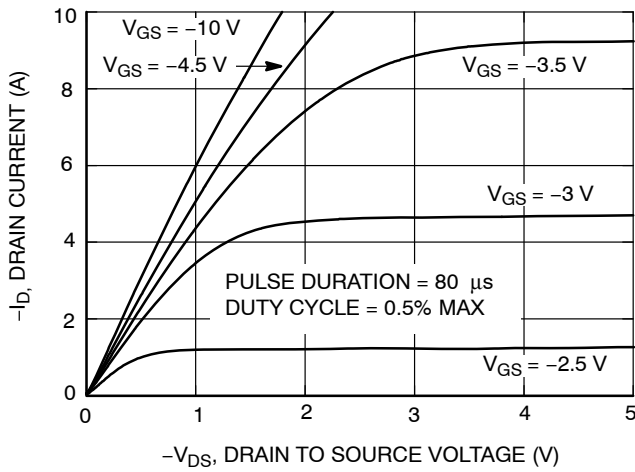


Figure 10. On-Region Characteristics

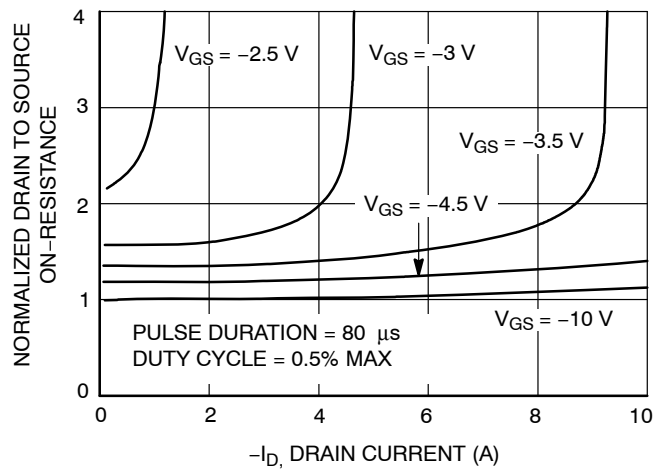


Figure 11. Normalized On-Resistance vs Drain Current and Gate Voltage

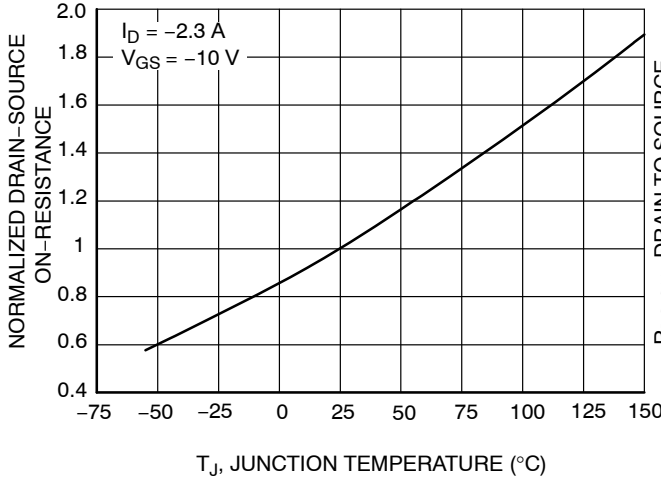


Figure 12. Normalized On-Resistance vs Junction Temperature

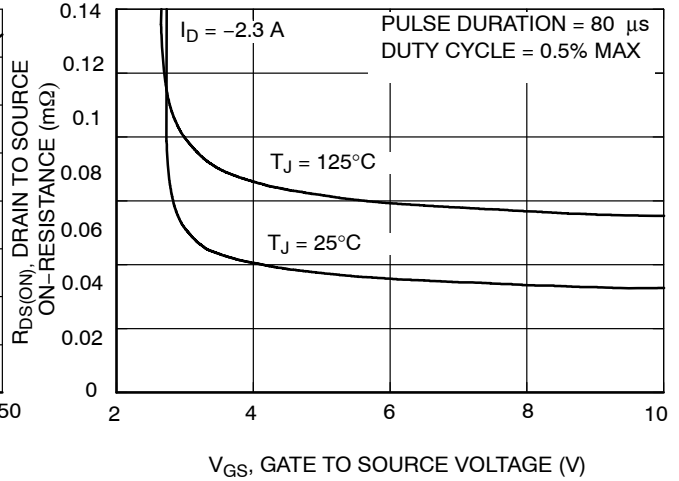


Figure 13. On-Resistance vs Gate to Source Voltage

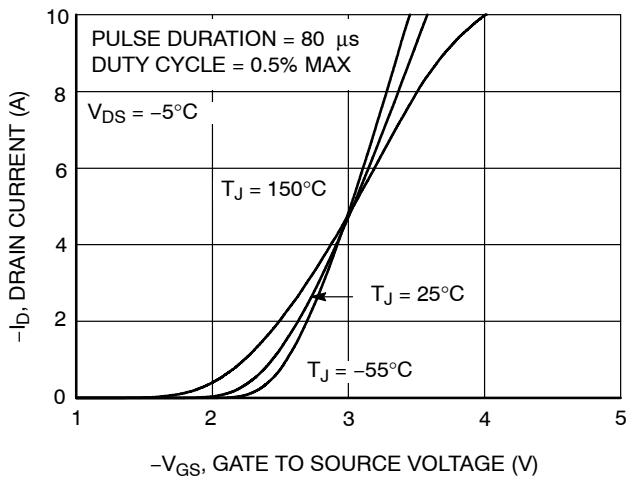


Figure 14. Transfer Characteristics

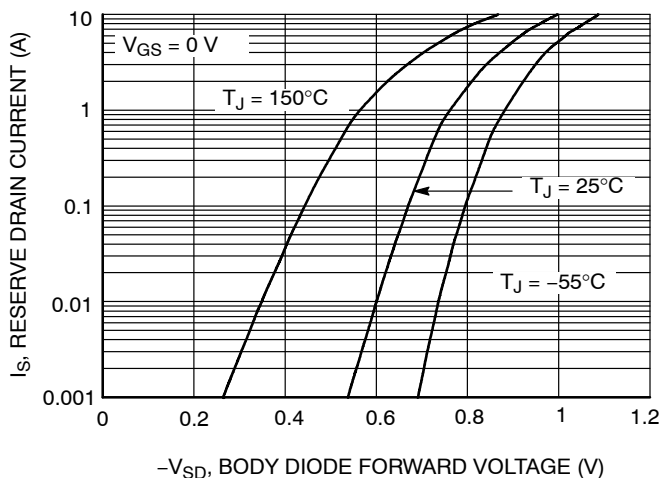


Figure 15. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q1 P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

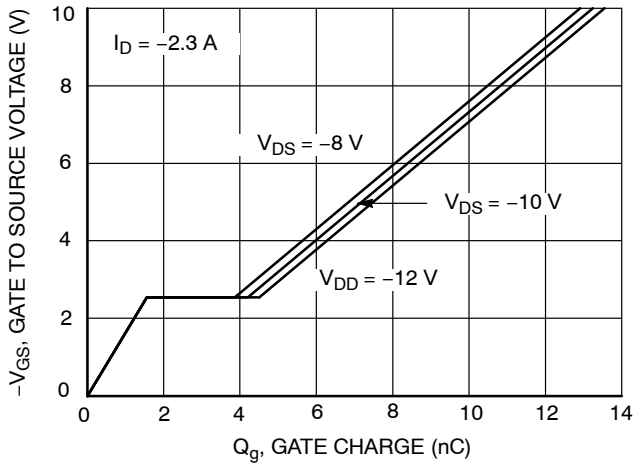


Figure 16. Gate Charge Characteristics

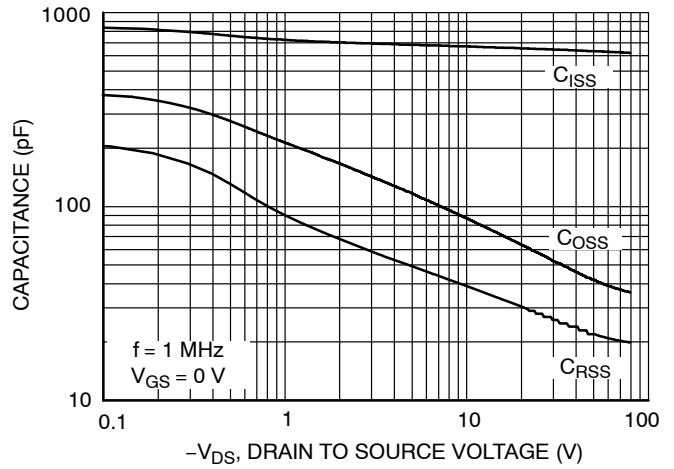


Figure 17. Capacitance vs Drain to Source Voltage

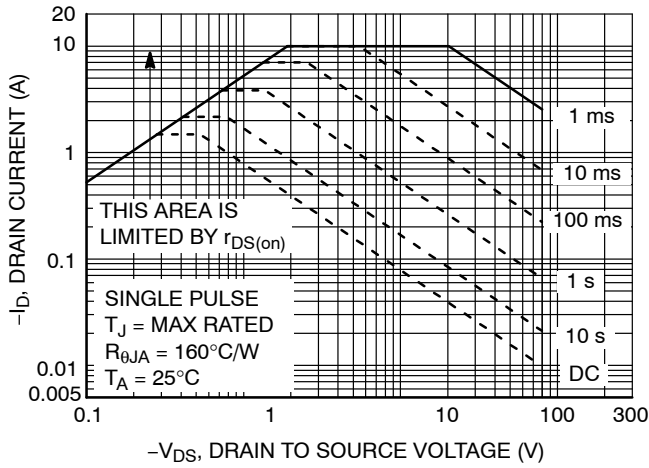


Figure 18. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

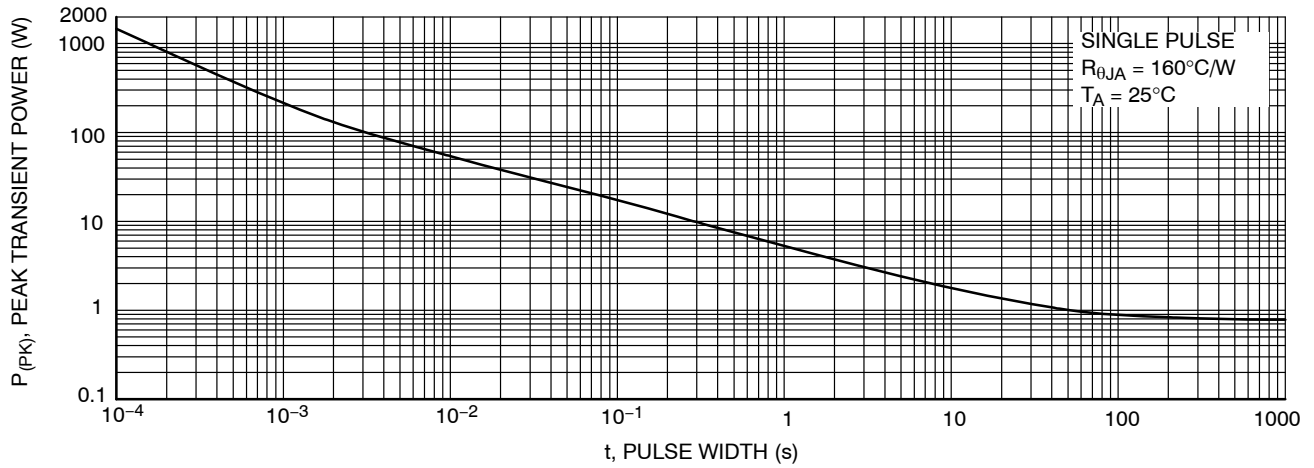


Figure 19. Single Pulse Maximum Power Dissipation

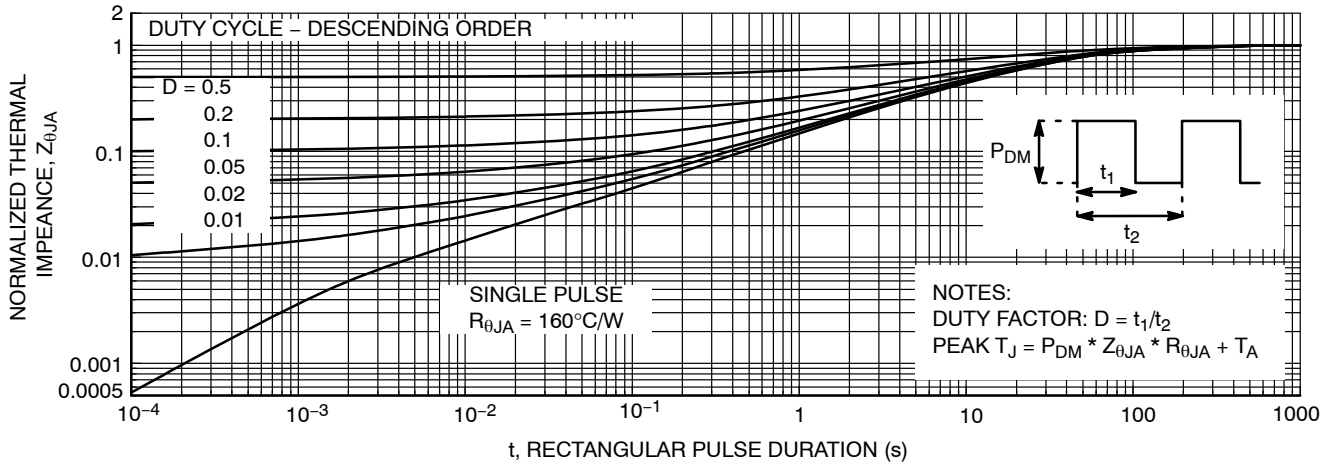


Figure 20. Junction-to-Ambient Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

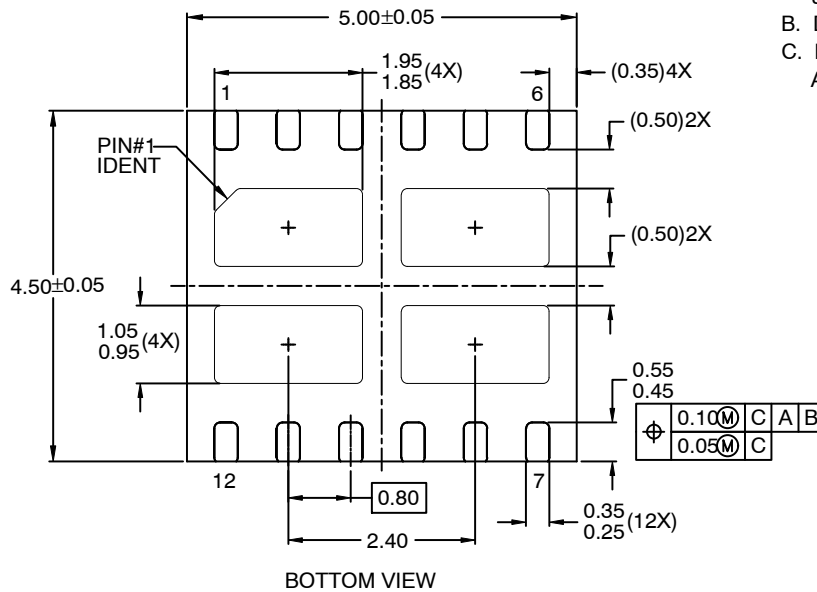
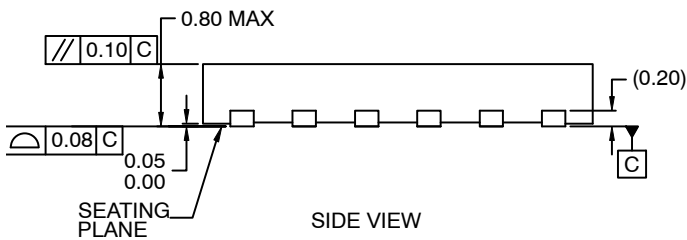
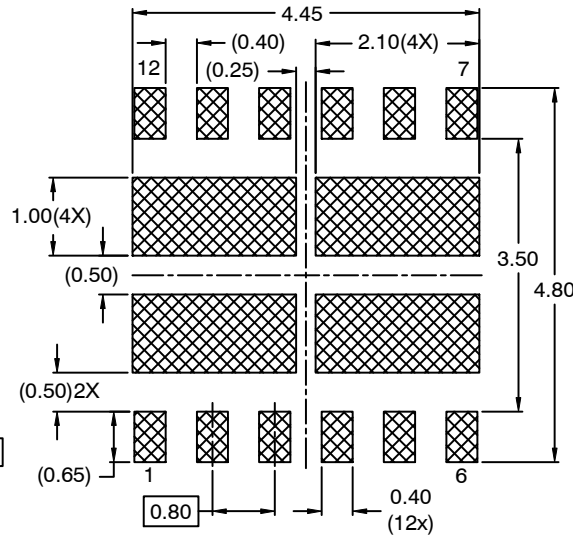
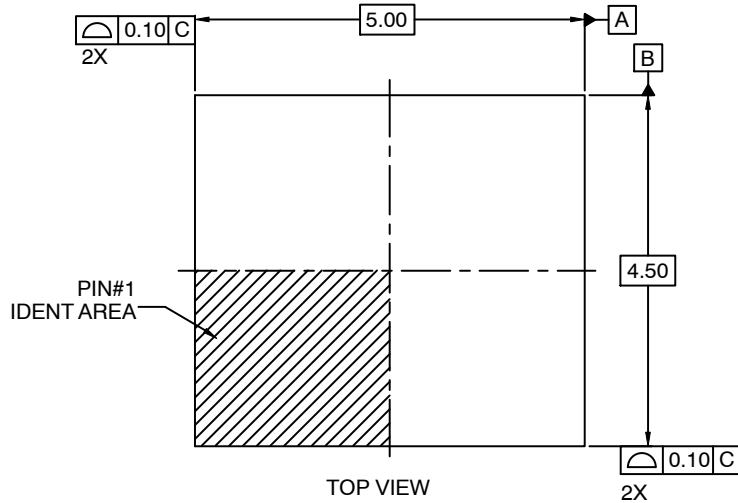
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN12 5x4.5, 0.8P
CASE 511CS
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

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