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Kind regards,

Team Nexperia

# DATA SHEET

## **74ALVCH16821**

20-bit bus-interface D-type flip-flop;  
positive-edge trigger (3-State)

Product specification

1998 May 29

IC24 Data Handbook

## 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

# 74ALVCH16821

### FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Current drive  $\pm 24$  mA at 3.0 V
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and ground pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50 $\Omega$  transmission lines @ 85°C

### DESCRIPTION

The 74ALVCH16821 has two 10-bit, edge triggered registers, with each register coupled to a 3-State output buffer. The two sections of each register are controlled independently by the clock (nCP) and Output Enable (nOE) control gates.

Each register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

When  $\overline{nOE}$  is LOW, the data in the register appears at the outputs. When  $\overline{nOE}$  is HIGH, the outputs are in high impedance OFF state. Operation of the nOE input does not affect the state of the flip-flops.

The 74ALVCH16821 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

### QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
$t_{PHL}/t_{PLH}$	Propagation delay nCP to nQ <sub>n</sub>	$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}, C_L = 50\text{pF}$	2.6 2.5	ns	
$C_I$	Input capacitance		5.0	pF	
$C_{PD}$	Power dissipation capacitance per buffer	$V_I = \text{GND to } V_{CC}^1$	Outputs enabled	33	pF
			Outputs disabled	17	
$F_{max}$	Maximum clock frequency	$V_{CC} = 2.5\text{V}, C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}, C_L = 50\text{pF}$	250	MHz	
			350		

#### NOTE:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ALVCH16821 DL	ACH16821 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16821 DGG	ACH16821 DGG	SOT364-1

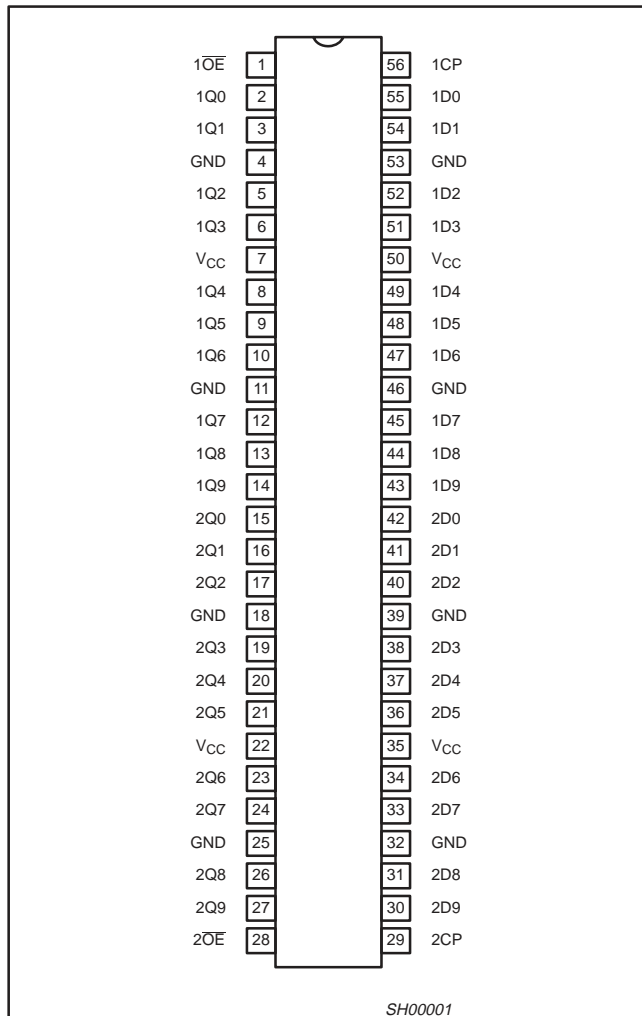
# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

## 74ALVCH16821

### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
55, 54, 52, 51, 49, 48, 47, 45, 44, 43	1D0 - 1D9	Data inputs
42, 41, 40, 38, 37, 36, 34, 33, 31, 30	2D0 - 2D9	
2, 3, 5, 6, 8, 9, 10, 12, 13, 14	1Q0 - 1Q9	Data outputs
15, 16, 17, 19, 20, 21, 23, 24, 26, 27	2Q0 - 2Q9	
1, 28	1OE, 2OE	Output enable inputs (active-Low)
56, 29	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage

### PIN CONFIGURATION

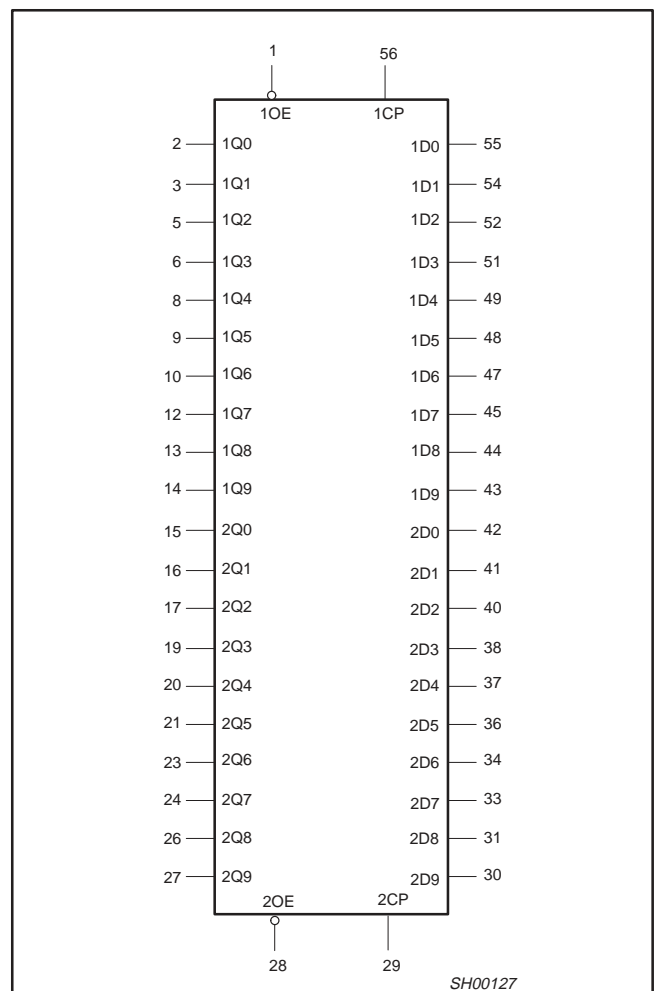


### FUNCTION TABLE

INPUTS			OUTPUT
nOE	CP	Dx	Q
L	↑	L	L
L	↑	H	H
L	‡	X	Q0
H	X	X	Z

H = HIGH voltage level  
 L = LOW voltage level  
 X = Don't care  
 Z = High impedance OFF state  
 ↑ = LOW to HIGH clock transition  
 ‡ = Not a LOW-to-HIGH clock transition

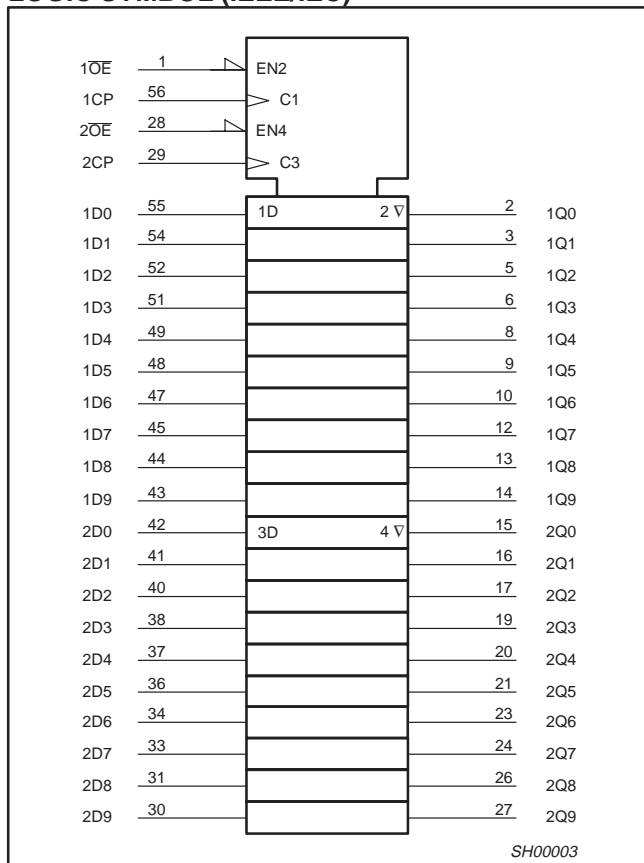
### LOGIC SYMBOL



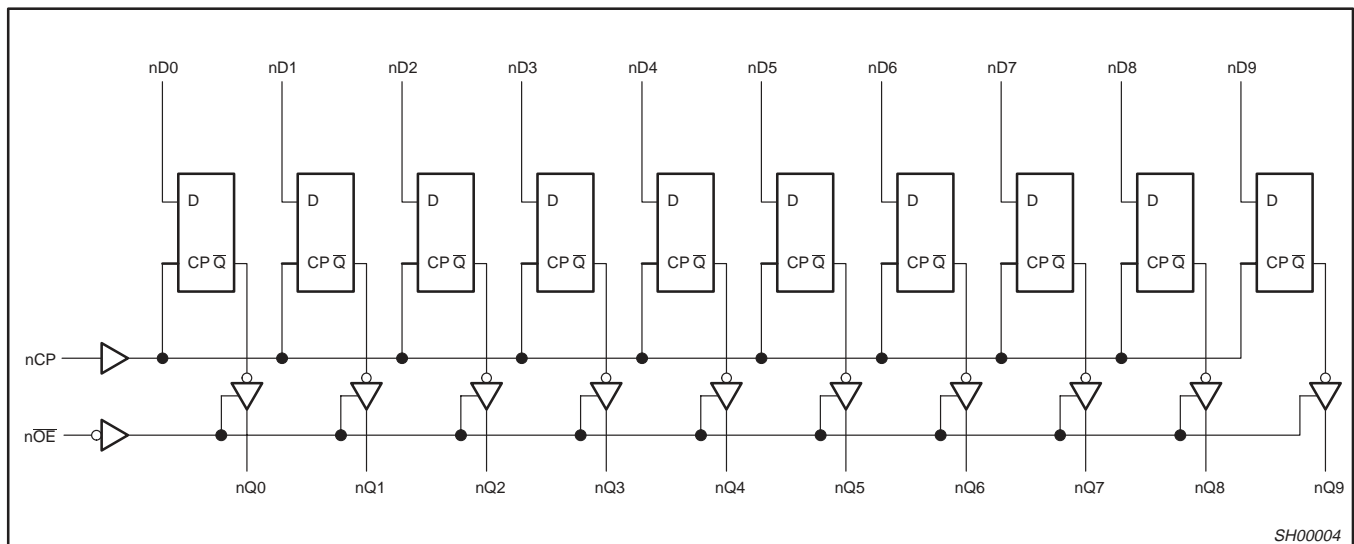
# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
$V_I$	DC Input voltage range		0	$V_{CC}$	V
$V_O$	DC output voltage range		0	$V_{CC}$	V
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 2.3$ to $3.0V$	0	20	ns/V
		$V_{CC} = 3.0$ to $3.6V$	0	10	

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For control pins <sup>1</sup>	-0.5 to +4.6	V
		For data inputs <sup>1</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

### NOTE:

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.40	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.70	V
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V <sup>2</sup>	45	-		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2</sup>	75	150		
I <sub>BHH</sub>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V <sup>2</sup>	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2</sup>	-75	-175		
I <sub>BHLO</sub>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	500			μA
I <sub>BHHO</sub>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	-500			μA

### NOTES:

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

## AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE

GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP <sup>1</sup>	MAX	
$t_{PLH}/t_{PHL}$	Propagation delay nCP to nQ <sub>n</sub>	1, 4	1.0	2.6	5.8	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE <sub>n</sub> to nQ <sub>n</sub>	2, 4	1.0	2.8	6.6	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE <sub>n</sub> to nQ <sub>n</sub>	2, 4	1.0	2.2	5.7	ns
$t_W$	nCP pulse width HIGH or LOW	3, 4	3.0	1.8		ns
$t_{SU}$	Set up time nD <sub>n</sub> to nCP	3, 4	1.4	0.3		ns
$t_h$	Hold time nD <sub>n</sub> to nCP	3, 4	0.4	0.0		ns
$F_{max}$	Maximum clock pulse frequency	1, 4	150	250		MHz

**NOTE:**1. All typical values are at  $V_{CC} = 2.5V$  and  $T_{amb} = 25^\circ C$ .

## AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$

GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3 \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nCP to nQ <sub>n</sub>	1, 4	1.0	2.5	4.5	1.0	2.8	5.3	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE <sub>n</sub> to nQ <sub>n</sub>	2, 4	1.0	2.3	5.1	1.0	3.2	6.2	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE <sub>n</sub> to nQ <sub>n</sub>	2, 4	1.0	2.8	4.6	1.0	3.1	5.0	ns
$t_W$	nCP pulse width HIGH or LOW	3, 4	3.3	0.2		3.3	1.7		ns
$t_{SU}$	Set up time nD <sub>n</sub> to nCP	3, 4	1.0	0.2		1.2	0.3		ns
$t_h$	Hold time nD <sub>n</sub> to nCP	3, 4	0.8	0.4		0.6	-0.3		ns
$F_{max}$	Maximum clock pulse frequency	1, 4	150	350		150	300		MHz

**NOTES:**1. All typical values are at  $T_{amb} = 25^\circ C$ .



# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

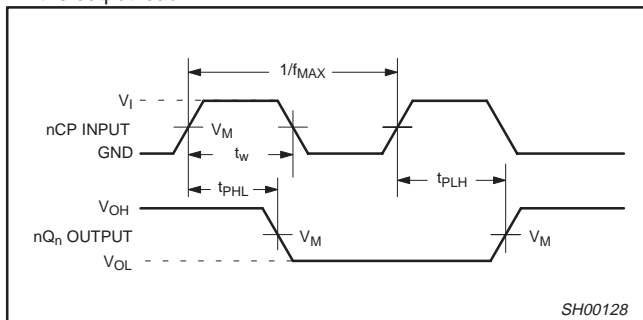
## AC WAVEFORMS

### V<sub>CC</sub> = 2.3 TO 2.7 V RANGE

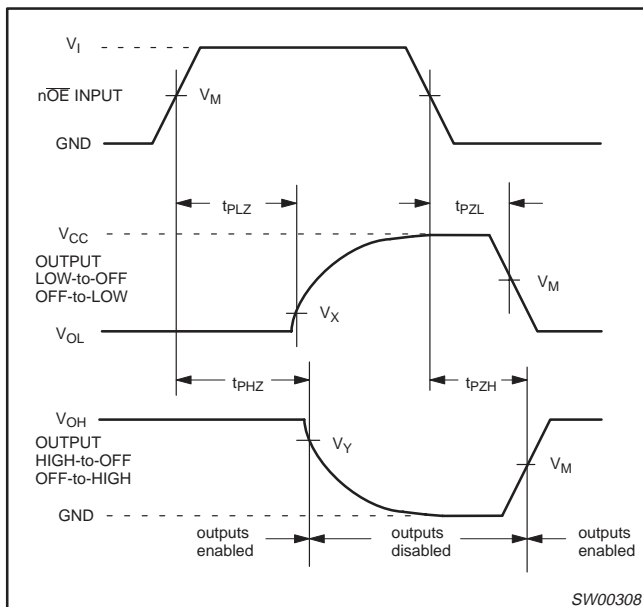
1. V<sub>M</sub> = 0.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.15V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.15V
4. V<sub>I</sub> = V<sub>CC</sub>
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

### V<sub>CC</sub> = 3.0 TO 3.6 V RANGE AND V<sub>CC</sub> = 2.7 V

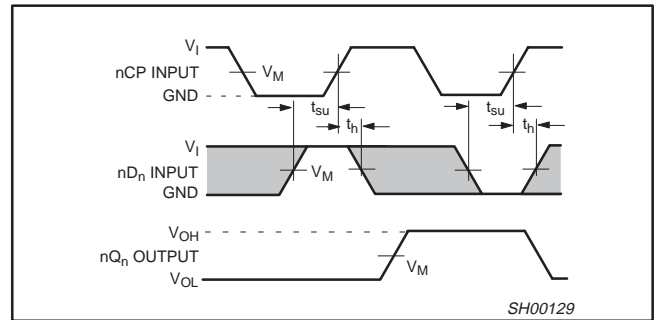
1. V<sub>M</sub> = 1.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.3V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.3V
4. V<sub>I</sub> = 2.7 V
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.



Waveform 1. The input (nCP) to output propagation delays.

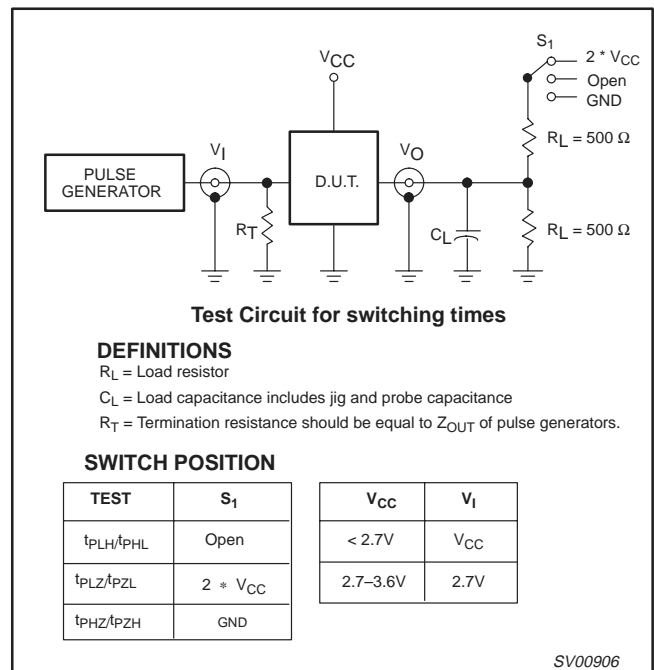


Waveform 2. The 3-State enable and disable times.



Waveform 3. Set up and hold times.

## TEST CIRCUIT



Test Circuit for switching times

### DEFINITIONS

- RL = Load resistor
- CL = Load capacitance includes jig and probe capacitance
- RT = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

### SWITCH POSITION

TEST	S <sub>1</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 * V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	V <sub>I</sub>
< 2.7V	V <sub>CC</sub>
2.7-3.6V	2.7V

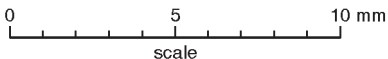
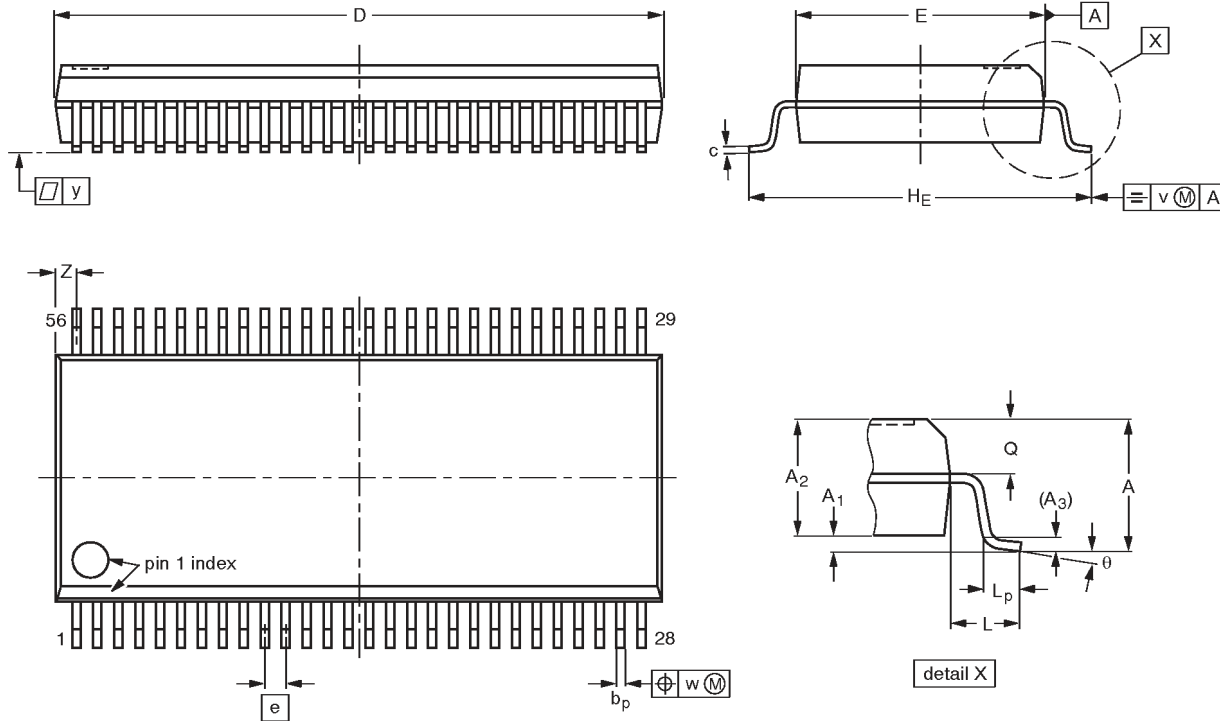
Waveform 4. Load circuitry for switching times

20-bit bus-interface D-type flip-flop;  
positive-edge trigger (3-State)

74ALVCH16821

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

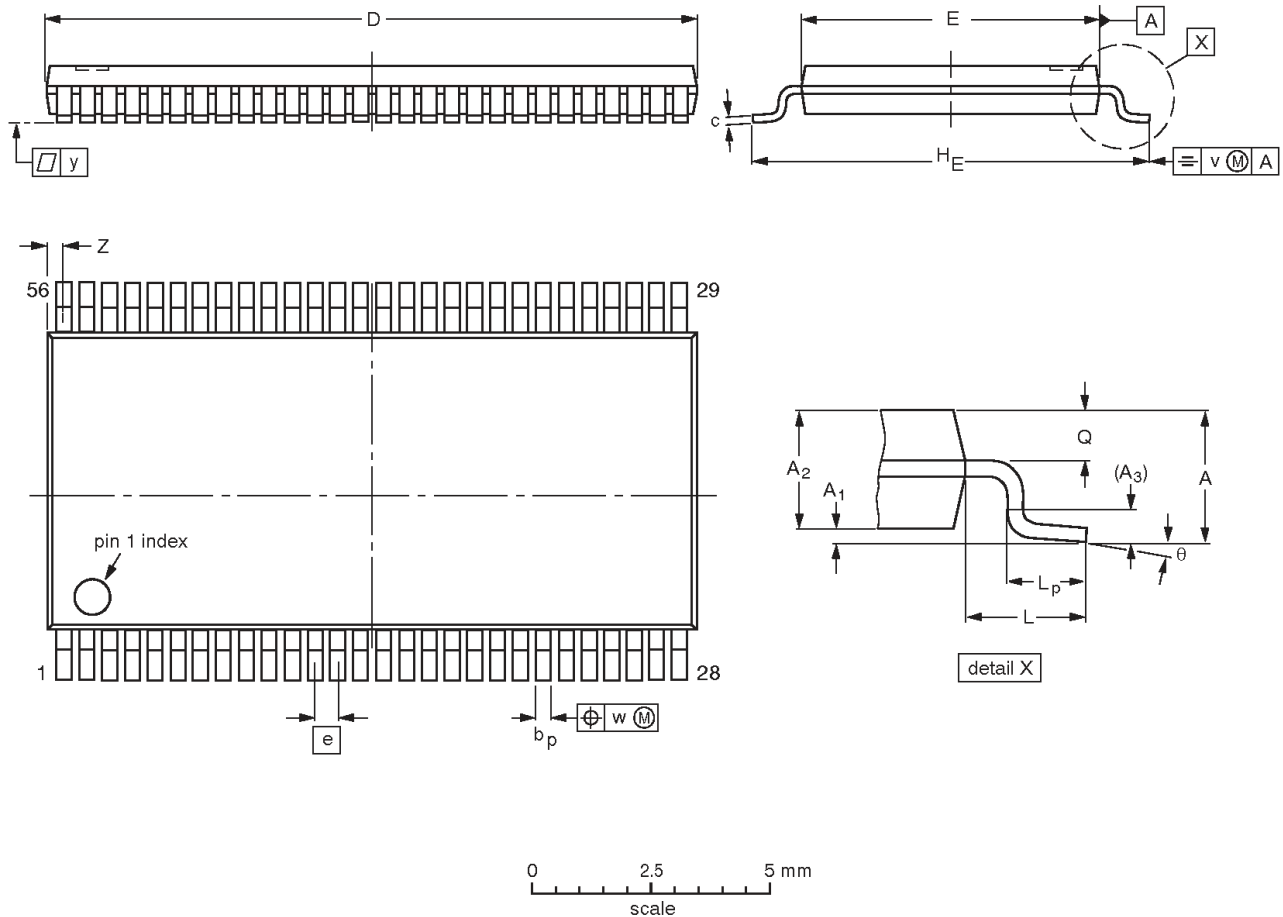
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

20-bit bus-interface D-type flip-flop;  
positive-edge trigger (3-State)

74ALVCH16821

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	$\theta$
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10

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20-bit bus-interface D-type flip-flop;  
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74ALVCH16821

**NOTES**

# 20-bit bus-interface D-type flip-flop; positive-edge trigger (3-State)

74ALVCH16821

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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