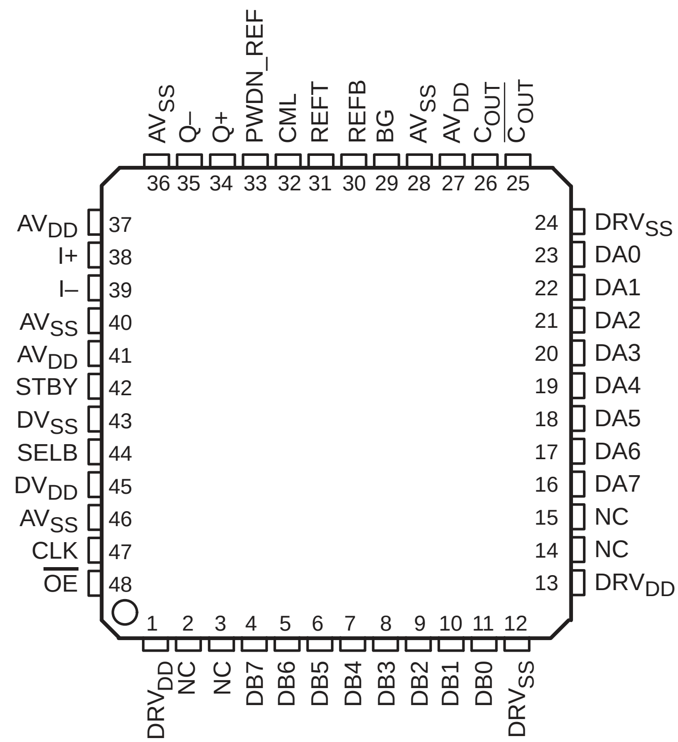
features

- **Dual Simultaneous Sample and Hold Inputs**
- **Differential or Single-Ended Analog Inputs**
- **8-Bit Resolution 40 MSPS Sampling Analog-to-Digital Converter (ADC)**
- **Single or Dual Parallel Bus Output**
- **Low Power Consumption: 275 mW Typ Using External References**
- **Wide Analog Input Bandwidth: 600 MHz Typ**
- **3.3 V Single-Supply Operation**
- **3.3 V TTL/CMOS-Compatible Digital I/O**
- **Internal or External Bottom and Top Reference Voltages**
- **Adjustable Reference Input Range**
- **Power-Down (Standby) Mode**
- **48-Pin Thin Quad Flat Pack (TQFP) Package**

PFB PACKAGE
(TOP VIEW)



applications

- **Digital Communications (Baseband Sampling)**
- **Cable Modems**
- **Set Top Boxes**
- **Test Instruments**

description

The THS0842 is a dual 8-bit 40 MSPS high-speed A/D converter. It alternately converts each analog input signal into 8-bit binary-coded digital words up to a maximum sampling rate of 40 MSPS with an 80 MHz clock. All digital inputs and outputs are 3.3 V TTL/CMOS-compatible.

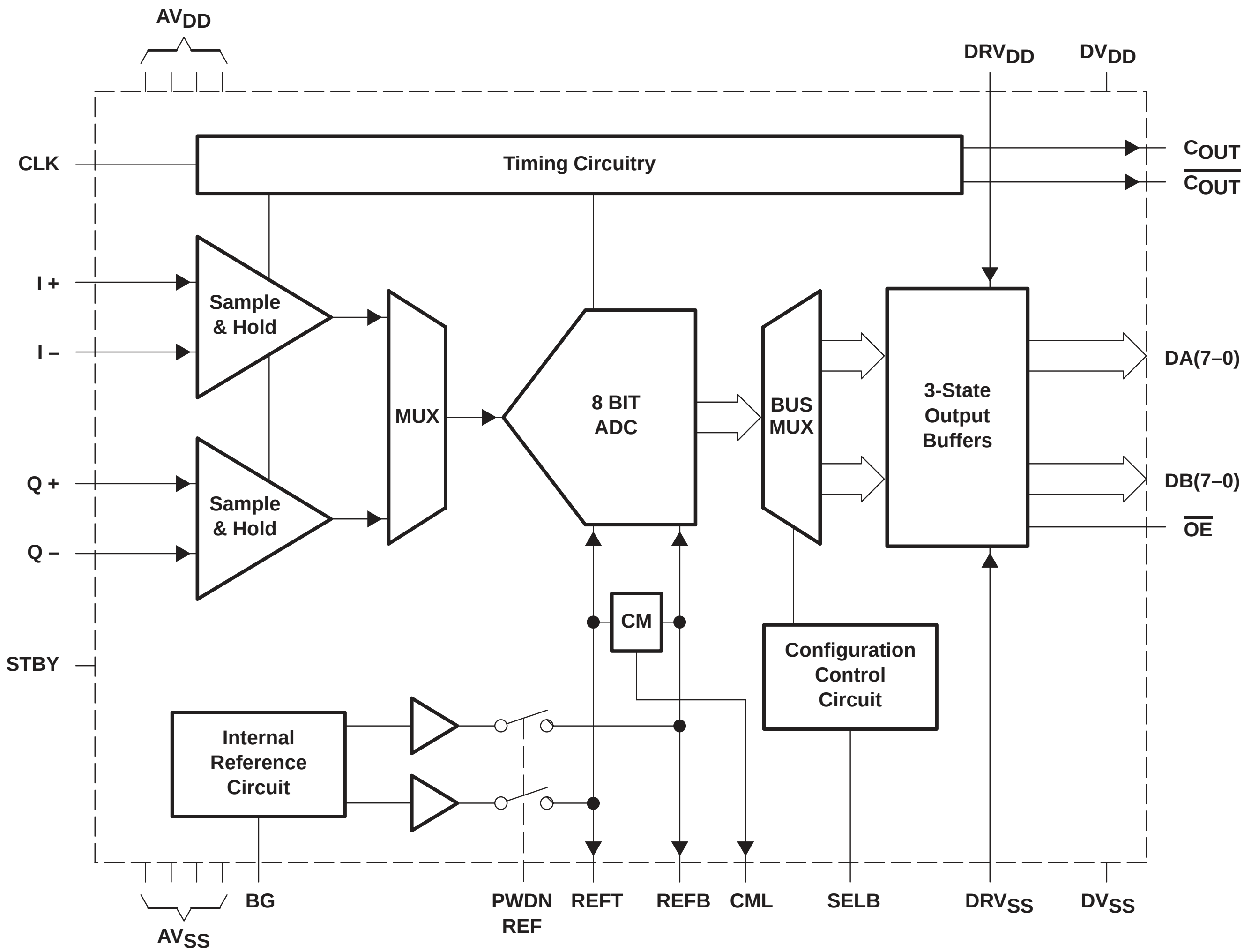
Thanks to an innovative single-pipeline architecture implemented in a CMOS process and the 3.3 V supply, the device consumes very little power. In order to provide maximum flexibility, both bottom and top voltage references can be set from user supplied voltages. Alternately, if no external references are available, on-chip references can be used which are also made available externally. The full-scale range is 1 Vpp, depending on the analog supply voltage. If external references are available, the internal references can be powered down independently from the rest of the chip, resulting in an even greater power saving.

The device is specifically suited for the baseband sampling of wireless local loop (WLL) communication, cable modems, set top boxes (STBs), and test instruments.

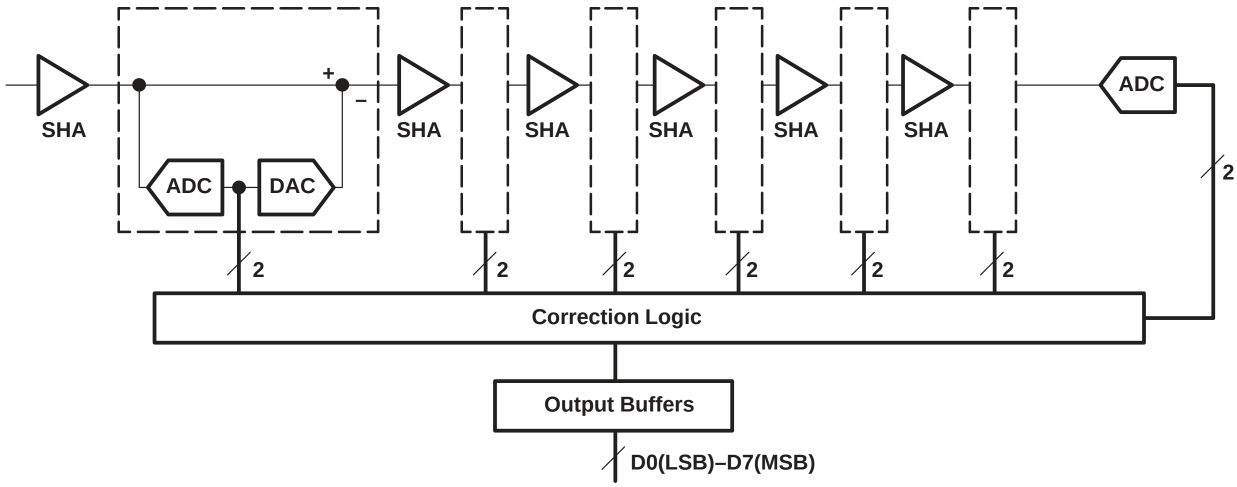
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TQFP-48
–40°C to 85°C	THS0842IPFB

functional block diagram

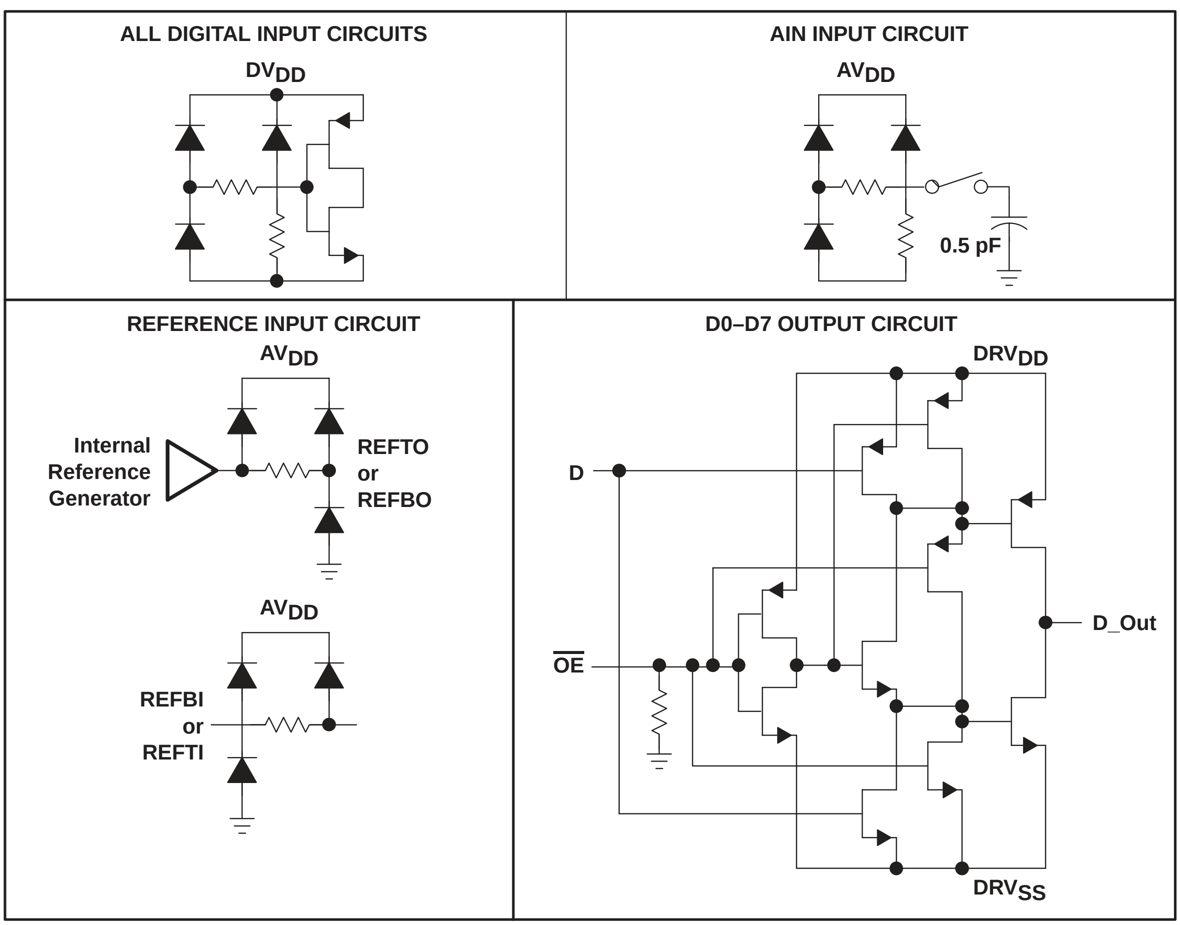


ADC pipeline block diagram



The single-pipeline architecture uses 6 ADC/DAC stages and one final flash ADC. Each stage produces a resolution of 2 bits. Digital correction logic generates its result using the 2-bit result from the first stage, 1 bit from each of the 5 succeeding stages, and 1 bit from the final stage in order to arrive at an 8-bit result. The correction logic ensures no missing codes over the full operating temperature range.

circuit diagrams of inputs and outputs



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	27, 37, 41	I	Analog supply voltage
AV_{SS}	28, 36, 40, 46	I	Analog ground
BG	29	O	Band gap reference voltage. A 1-µF capacitor with a 0.1-µF capacitor in parallel should be connected between this terminal and AV_{SS} for external filtering.
CLK	47	I	Clock input. The input is sampled on each rising edge of CLK.
CML	32	O	Common mode level. This voltage is equal to (AV_{DD} – AV_{SS})/2. An external 1-µF capacitor with a 0.1-µF capacitor in parallel should be connected between this terminal and AV_{SS}.
C_{OUT}	26	O	Latch clock for the data outputs
$\overline{C_{OUT}}$	25	O	Inverted latch clock for the data outputs
DB7 – DB0	4 – 11	O	Data outputs. D7 is the MSB. This is the second bus. Data is output from the Q channel when dual bus output mode is selected. Pin SELB selects the output mode.
DRV_{DD}	1, 13	I	Supply voltage for output drivers
DRV_{SS}	12, 24	I	Ground for digital output drivers
DA7 – DA0	16 – 23	I	Data outputs for bus A. D7 is MSB. This is the primary bus. Data from both input channels can be output on this bus or data from the I channel only. Pin SELB selects the output mode.
DV_{DD}	45	I	Digital supply voltage
DV_{SS}	43	I	Digital ground
I–	39	I	Negative input for analog channel 0.
I+	38	I	Positive input for analog channel 0.
NC	2,3,14,15		No connect. Reserved for future use
$\overline{OE}$	48	I	Output enable. A high on this terminal will disable the output bus.
PWDN_REF	33	I	Power down for internal reference voltages. A high on this terminal will disable the internal reference circuit.
Q–	35	I	Negative input for analog channel 1
Q+	34	I	Positive input for analog channel 1
REFB	30	I/O	Reference voltage bottom. The voltage at this terminal defines the bottom reference voltage for the ADC. Sufficient filtering should be applied to this input. A 1-µF capacitor with a 0.1-µF capacitor in parallel should be connected between REFB and AV_{SS}. Additionally, a 0.1-µF capacitor can be connected between REFT and REFB.
REFT	31	I/O	Reference voltage top. The voltage at this terminal defines the top reference voltage for the ADC. Sufficient filtering should be applied to this input. A 1-µF capacitor with a 0.1-µF capacitor in parallel should be connected between REFT and AV_{SS}. Additionally, a 0.1-µF capacitor can be connected between REFT and REFB.
SELB	44	I	Selects either single bus or data output or dual bus output data output. A low selects dual bus data output.
STBY	42	I	Standby input. A high level on this terminal will power down the device.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: AV_{DD} to AGND, DV_{DD} to DGND . . . . –0.5 V to 4 V
Supply voltage: AV_{DD} to DV_{DD}, AGND to DGND . . . . –0.5 V to 0.5 V
Digital input voltage range to DGND . . . . –0.5 V to DV_{DD} + 0.5 V
Analog input voltage range to AGND . . . . –0.5 V to AV_{DD} + 0.5 V
Digital output voltage applied from external source to DGND . . . . –0.5 V to DV_{DD} + 0.5 V
Reference voltage input range to AGND: $V_{(REFT)}$, $V_{(REFB)}$ . . . . –0.5 V to AV_{DD} + 0.5 V
Operating free-air temperature range, T_A: . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions over operating free-air temperature range

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD} DV_{DD} DRV_{DD}	3	3.3	3.6	V

analog and reference inputs

	MIN	NOM	MAX	UNIT
Reference input voltage (top), $V_{(REFT)}$	(NOM) – 0.2	AV_{DD} – 1	(NOM) + 0.2	V
Reference input voltage (bottom), $V_{(REFB)}$	0.8	1	1.2	V
Reference voltage differential, $V_{(REFT)} – V_{(REFB)}$			AV_{DD} – 2	V
Analog input voltage, $V_{(IN)}$	$V_{(REFB)}$		$V_{(REFT)}$	V

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	2.0		DV_{DD}	V
Low-level input voltage, V_{IL}	DGND		$0.2xDV_{DD}$	V
Clock period, t_c	12.5			ns
Pulse duration, clock high, $t_{w(CLKH)}$	5.25			ns
Pulse duration, clock low, $t_{w(CLKL)}$	5.25			ns

electrical characteristics over recommended operating conditions with f_{CLK} = 80 MSPS and use of internal voltage references, $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, $T_A = T_{MIN}$ to T_{MAX}, dual output bus mode (unless otherwise noted)

power supply

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating supply current	AV_{DD}	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.3 V, C_L = 15 pF, V_I = 1 MHz, –1 dBFS		73	95	mA
		DV_{DD}			3	3.8	
		DRV_{DD}			17	22	
P_D	Power dissipation		PWDN_REF = L		320	393	mW
			PWDN_REF = H		275	335	
$P_{D(STBY)}$	Standby power		STBY = H, CLK held high or low		11	15	

logic inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current on CLK†	$AV_{DD} = DV_{DD} = DRV_{DD}$ = CLK = 3.6 V			10	µA
I_{IL}	Low-level input current on digital inputs ($\overline{OE}$, STDBY, PWDN_REF, CLK)	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.6 V, Digital inputs at 0 V			10	µA
C_I	Input capacitance			5		pF

† I_{IH} leakage current on other digital inputs ($\overline{OE}$, STDBY, PWDN_REF) is not measured since these inputs have an internal pull-down resistor of 4 KΩ to DGND.

logic outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V at I_{OH} = 50 µA, Digital output forced high	2.8			V
V_{OL}	Low-level output voltage	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.6 V at I_{OL} = 50 µA, Digital output forced low			0.1	V
C_O	Output capacitance			5		pF
I_{OZH}	High-impedance state output current to high level	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.6 V			10	µA
I_{OZL}	High-impedance state output current to low level				10	µA

electrical characteristics over recommended operating conditions with f_{CLK} = 80 MSPS and use of internal voltage references, $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, $T_A = T_{MIN}$ to T_{MAX}, dual output bus mode (unless otherwise noted) (continued)

dc accuracy

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Integral nonlinearity (INL), best-fit	See Note 1	T_A = –40°C to 85°C	–2.2	±1.5	2.2	LSB
Differential nonlinearity (DNL)	See Note 2	T_A = –40°C to 85°C	–1	±0.7	2	LSB
Offset error	T_A = –40°C to 85°C, (see Note 3)			±0.1	5	%FS
Gain error	T_A = –40°C to 85°C, (see Note 3)			±7.1		%FS
Offset match	T_A = –40°C to 85°C, (see Note 4)		–1	±0.1	1	LSB
Gain match	T_A = –40°C to 85°C, (see Note 5)		–5		1	LSB
Missing codes – no missing codes assured						

NOTES: 1. Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full–scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best fit line between these two endpoints.
2. An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level) ÷ (2^n – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.
3. Offset error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).

   Gain error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 254 to code 255. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).
4. Offset match is the change in offset error between I and Q channels.
5. Gain match is the change in gain error between I and Q channels.

analog input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance			4		pF

reference input ($AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.6 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ref}	Reference input resistance			200		Ω
I_{ref}	Reference input current			5		mA

reference outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REFT)}$	Reference top voltage	AV_{DD} = 3 V		2 + [(AV_{DD} – 3)/2]		V
$V_{(REFB)}$	Reference bottom voltage	AV_{DD} = 3 V		1 + [(AV_{DD} – 3)/2]		V
$V_{REFB}–V_{REFB}$		Absolute min/max values valid and tested for AV_{DD} = 3 V	0.9	1	1.3	V

electrical characteristics over recommended operating conditions with f_{CLK} = 80 MSPS and use of internal voltage references, $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, $T_A = T_{MIN}$ to T_{MAX}, dual output bus mode (unless otherwise noted) (continued)

dynamic performance†

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Effective number of bits, ENOB	f_{in} = 1 MHz	6.6	6.9		Bits
	f_{in} = 15 MHz	6.4	6.8		
	f_{in} = 20 MHz	6.4	6.8		
Signal-to-total harmonic distortion + noise, S/(THD+N)	f_{in} = 1 MHz	41.5	43.5		dB
	f_{in} = 15 MHz	40	42.5		
	f_{in} = 20 MHz	40	42.5		
Total harmonic distortion (THD)	f_{in} = 1 MHz		–51	–46	dB
	f_{in} = 15 MHz		–48.5	–44	
	f_{in} = 20 MHz		–48.5	–44	
Spurious free dynamic range (SFDR)	f_{in} = 1 MHz	48	53		dB
	f_{in} = 15 MHz	47	52.2		
	f_{in} = 20 MHz	46	52		
Analog input full-power bandwidth, BW	See Note 6		600		MHz
Intermodulation distortion	f1 = 1 MHz, f2 = 1.02 MHz		50		dBc
I/Q channel crosstalk	$AV_{DD} = DV_{DD} = DRV_{DD}$ = 3.3 V		–52		dBc

† Based on analog input voltage of –1 dBFS referenced to a 1.3 V_{pp} full-scale input range.

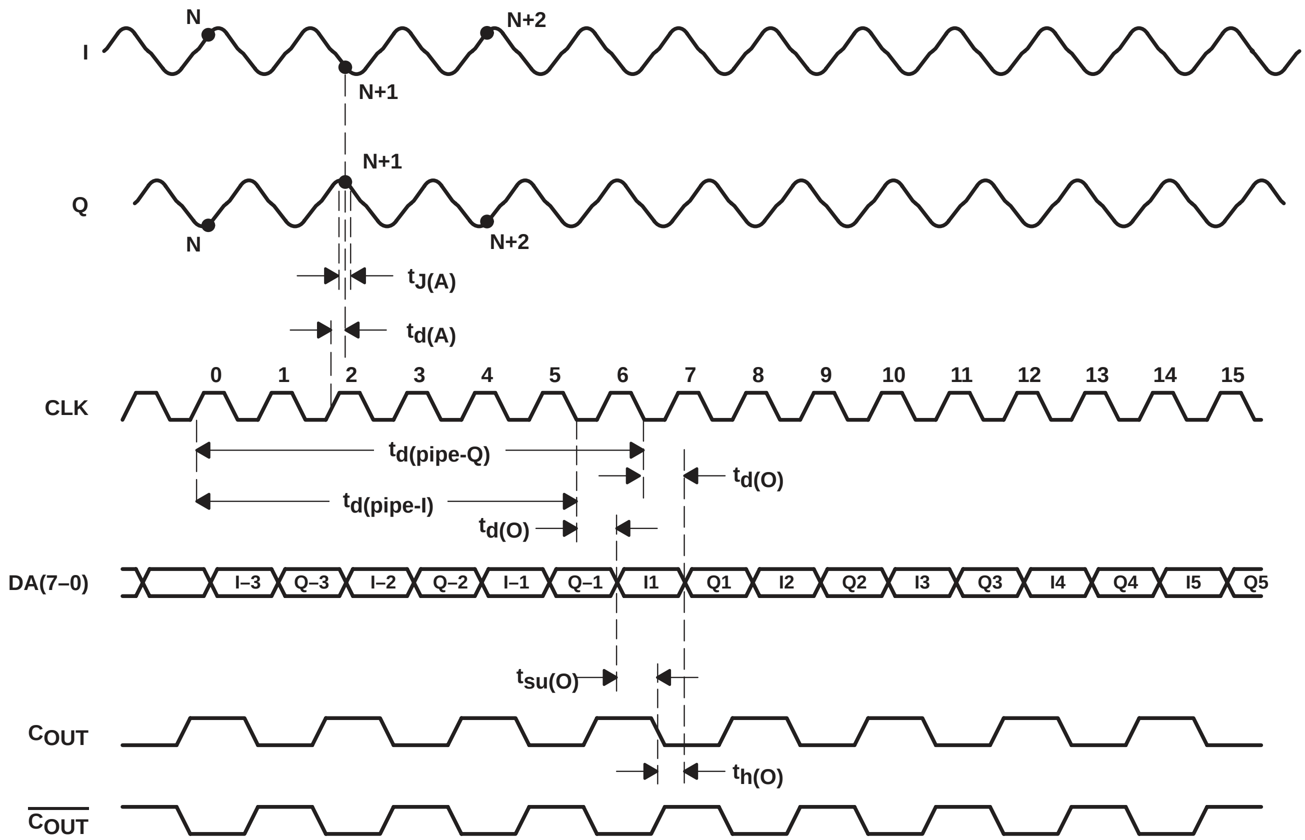
NOTE 6: The analog input bandwidth is defined as the maximum frequency of a –1 dBFS input sine that can be applied to the device for which an extra 3 dB attenuation is observed in the reconstructed output signal.

timing requirements

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Maximum clock rate (see Note 7)					80	MHz
	Minimum clock rate			10			kHz
$t_{d(O)}$	Output delay time (see timing diagram)		C_L = 10 pF			9	ns
$t_{h(O)}$	Output hold time from C_{OUT} or $\overline{C_{OUT}}$ to data invalid			2			ns
$t_{d(pipe)}$	Pipeline delay (latency)	I data		5.5	5.5	5.5	CLK cycles
		Q data		6.5	6.5	6.5	
$t_{d(a)}$	Aperture delay time				3		ns
$t_{j(a)}$	Aperture jitter				1.5		ps, rms
t_{dis}	Disable time, $\overline{OE}$ rising to Hi-Z				5		ns
t_{en}	Enable time, $\overline{OE}$ falling to valid data				5		ns
$t_{su(O)}$	Output setup time from data to C_{OUT} or $\overline{C_{OUT}}$			8	7		ns

NOTE 7: Conversion rate is 1/2 the clock rate, f_{clk}.

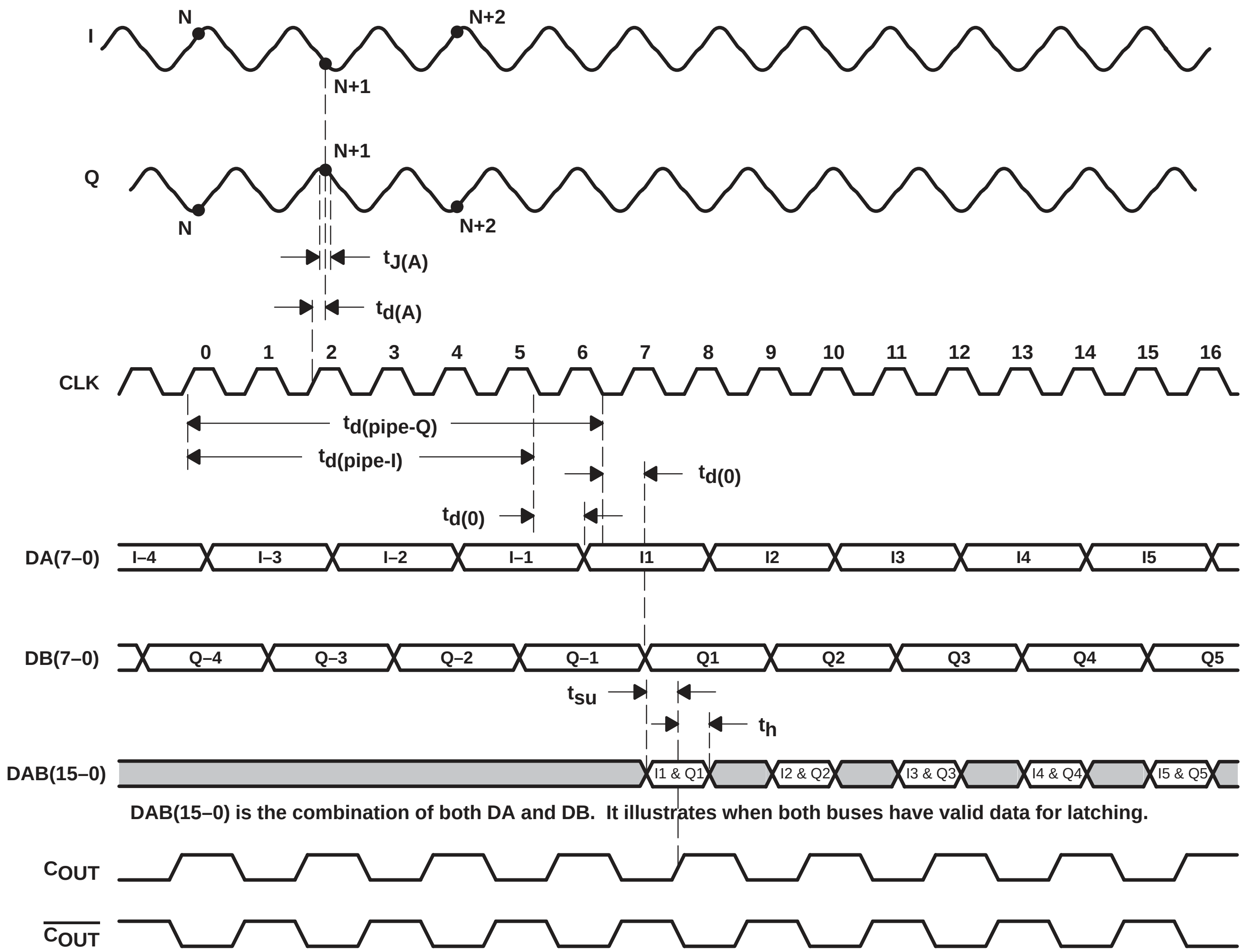
PARAMETER MEASUREMENT INFORMATION



NOTE A: The relationship between CLK and $C_{OUT}/\overline{C_{OUT}}$ is not fixed and depends on the power-on conditions. Data out should be referenced to C_{OUT} and $\overline{C_{OUT}}$.

Figure 1. Timing Diagram, Single Bus Output

PARAMETER MEASUREMENT INFORMATION



NOTE A: The relationship between CLK and $C_{OUT}/\overline{C_{OUT}}$ is not fixed and depends on the power-on conditions. Data out should be referenced to C_{OUT} and $\overline{C_{OUT}}$.

Figure 2. Timing Diagram, Dual Bus Output

TYPICAL CHARACTERISTICS†

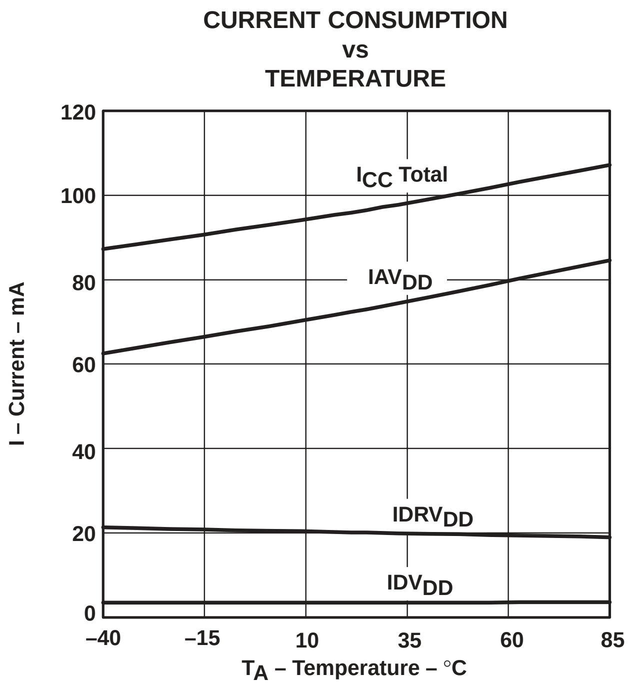


Figure 3

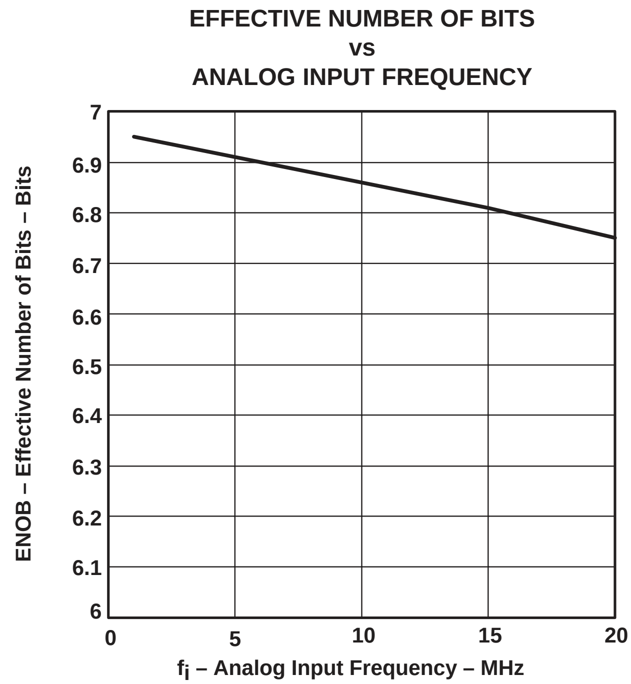


Figure 4

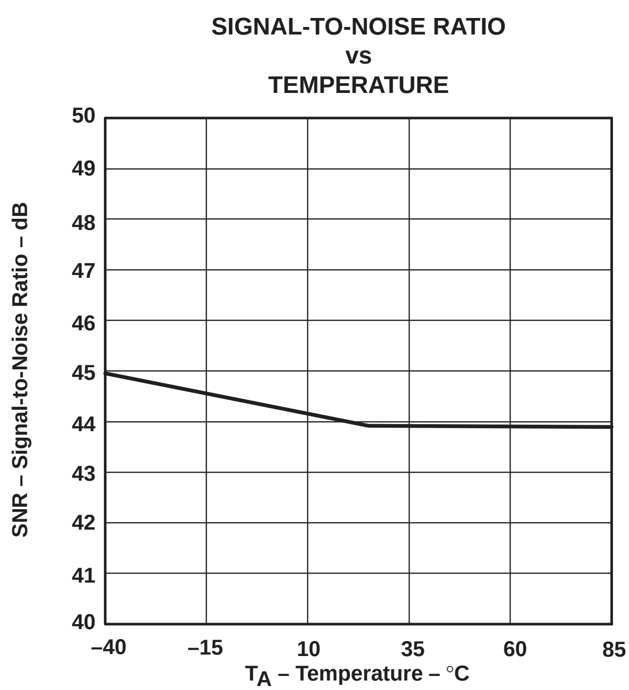


Figure 5

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD} = 3$ V, $f_{CLK} = 80$ MHz, analog input = –1 dB FS, $T_A = 25°C$.

TYPICAL CHARACTERISTICS†

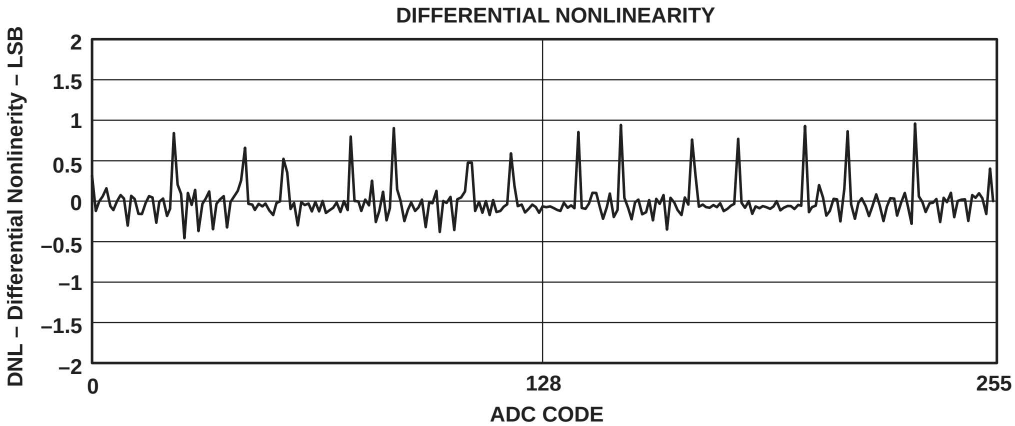


Figure 6

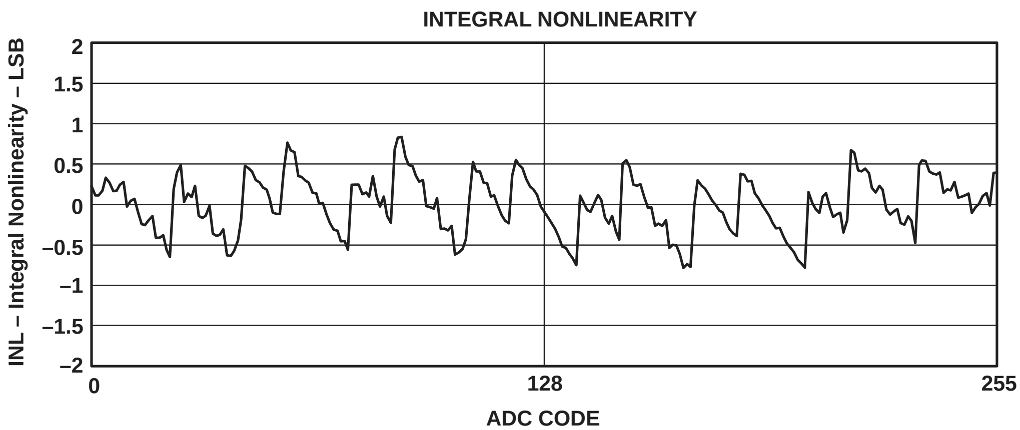


Figure 7

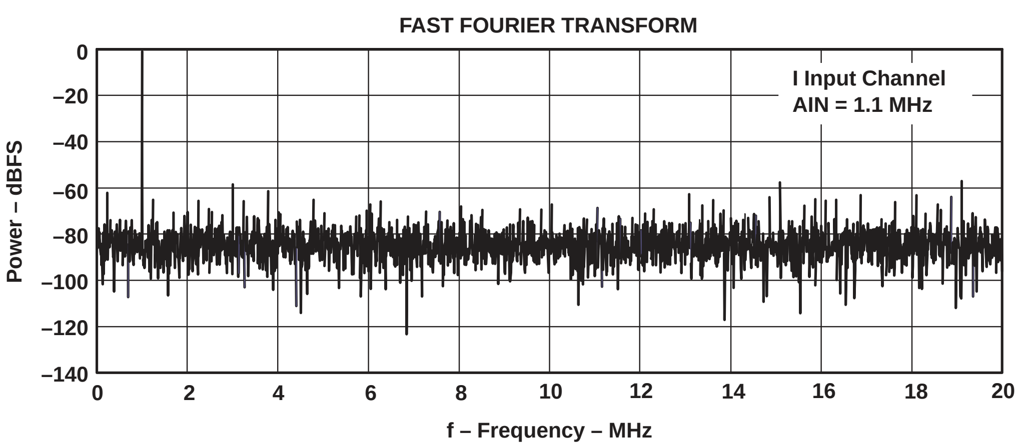


Figure 8

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, f_{CLK} = 80 MHz, analog input = –1 dB FS, T_A = 25°C.

TYPICAL CHARACTERISTICS†

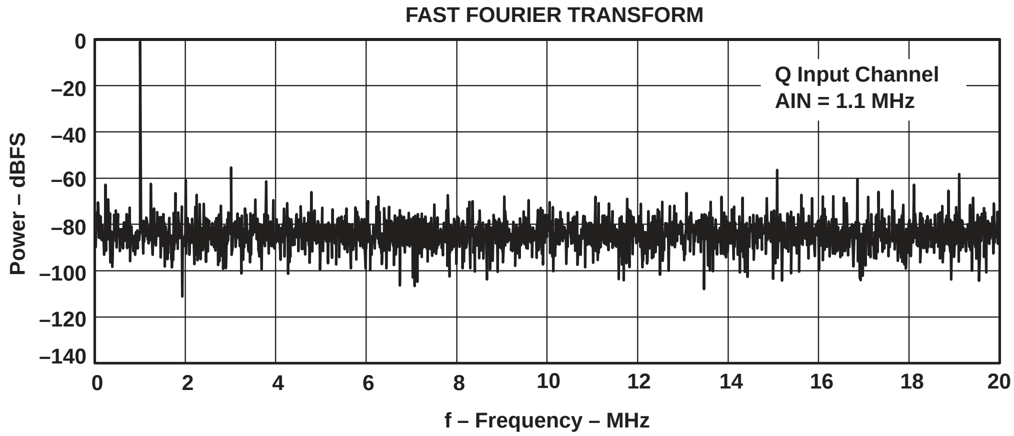


Figure 9

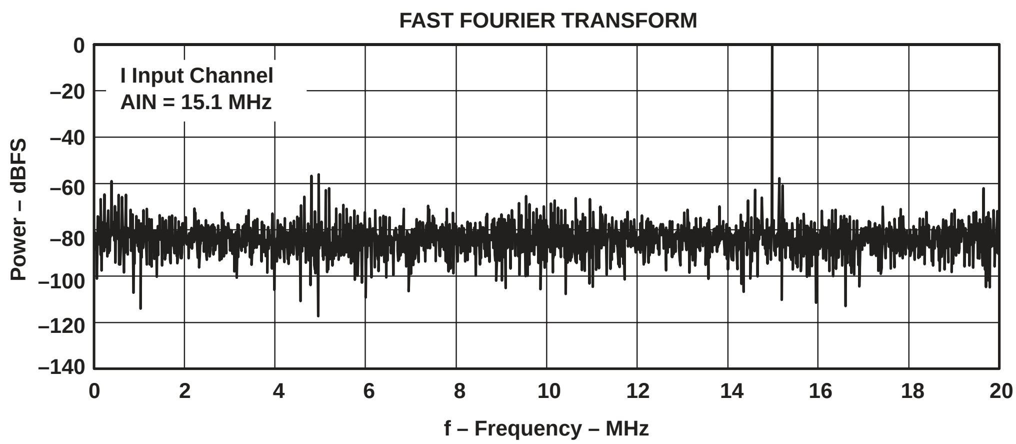


Figure 10

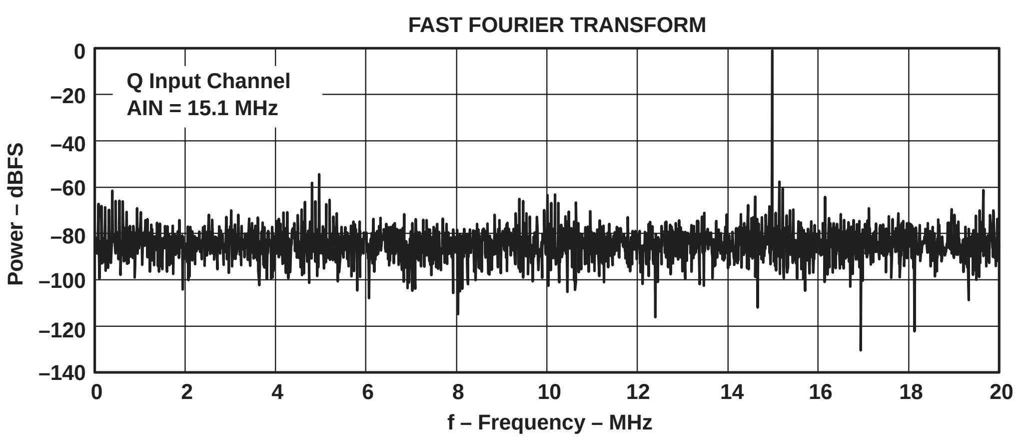


Figure 11

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, f_{CLK} = 80 MHz, analog input = –1 dB FS, T_A = 25°C.

TYPICAL CHARACTERISTICS†

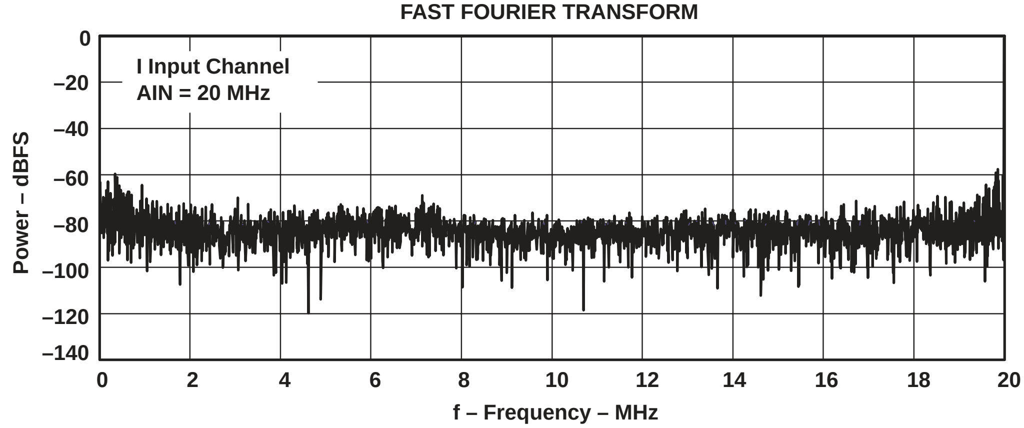


Figure 12

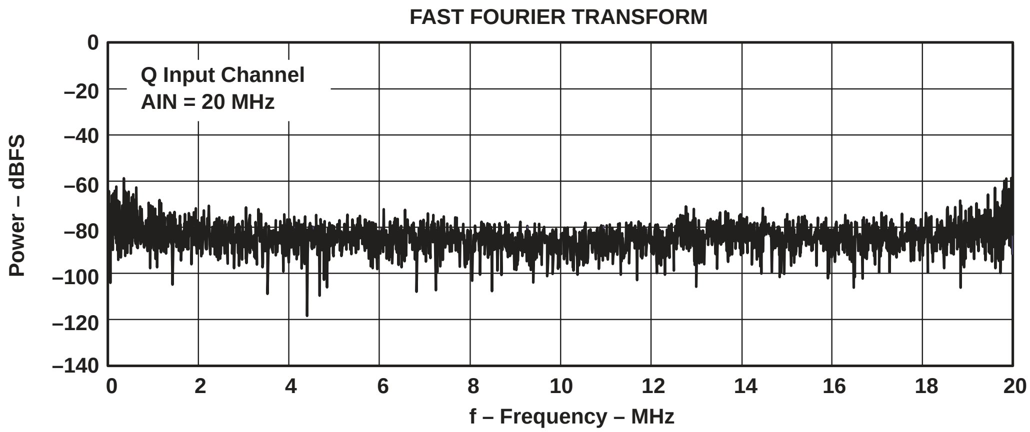


Figure 13

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD} = 3$ V, $f_{CLK} = 80$ MHz, analog input = –1 dB FS, $T_A = 25°C$.

TYPICAL CHARACTERISTICS†

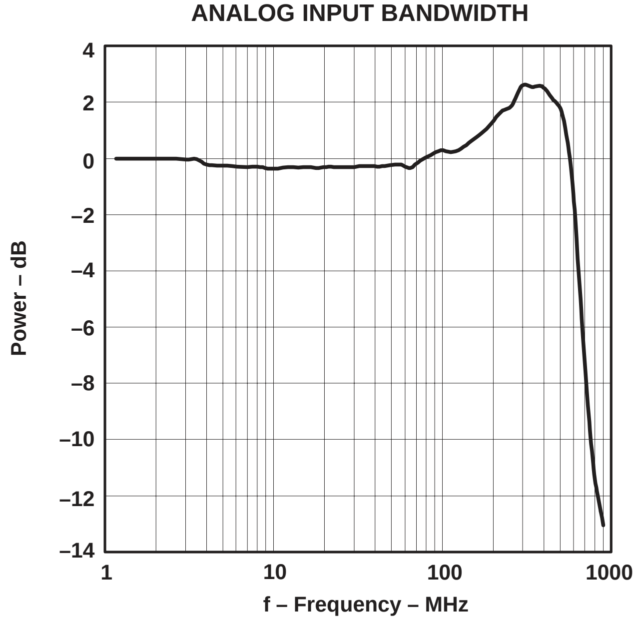


Figure 14

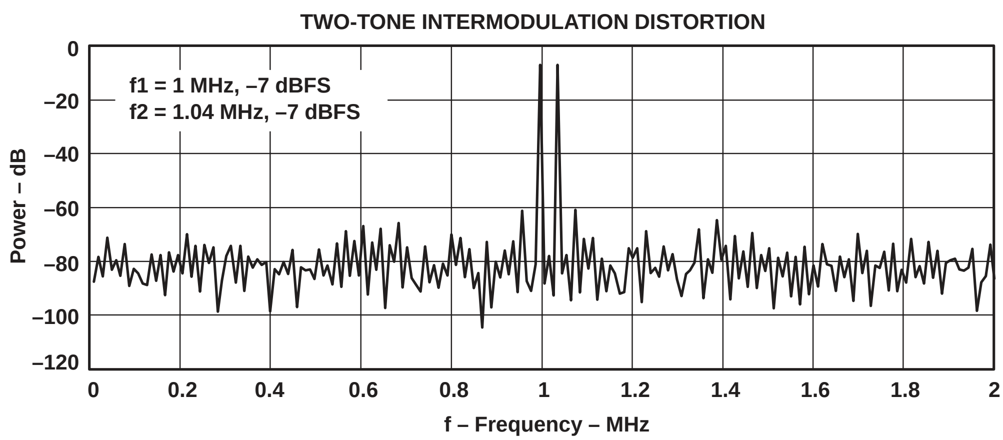


Figure 15

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, f_{CLK} = 80 MHz, analog input = –1 dB FS, T_A = 25°C.

TYPICAL CHARACTERISTICS†

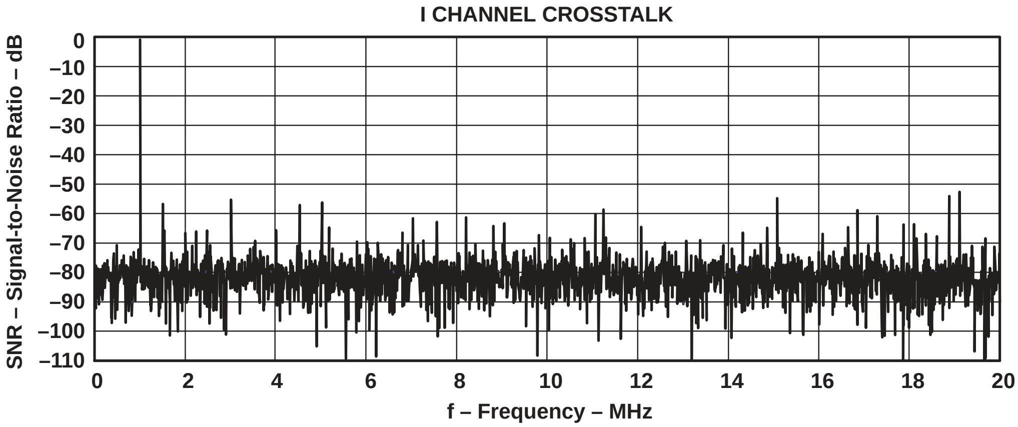


Figure 16

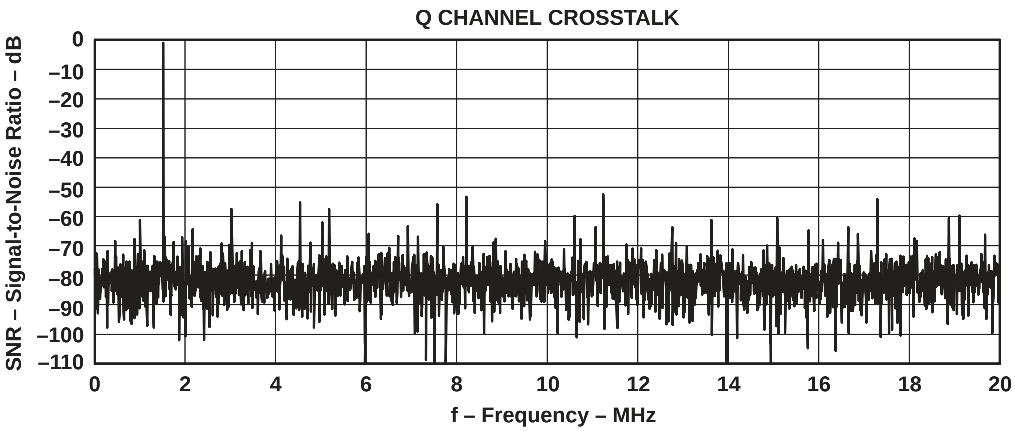


Figure 17

† Unless otherwise noted $AV_{DD} = DV_{DD} = DRV_{DD}$ = 3 V, f_{CLK} = 80 MHz, analog input = –1 dB FS, T_A = 25°C.

PRINCIPLES OF OPERATION

definitions of specifications and terminology

integral nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

differential nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test, i.e. (last transition level – first transition level)/(2n –2). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.

offset and gain error

Offset error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).

Gain error is defined as the difference in analog input voltage – between the ideal voltage and the actual voltage – that will switch the ADC output from code 254 to code 255. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (256).

analog input bandwidth

The analog input bandwidth is defined as the maximum frequency of a 1-dBFS input sine wave that can be applied to the device for which an extra 3-dB attenuation is observed in the reconstructed output signal.

output timing

Output timing $t_{d(o)}$ is measured from the 1.5-V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10 pF.

Output hold time $t_{h(o)}$ is measured from the 1.5-V level of the CLK input falling edge to the10%/90% level of the digital output. The digital output load is not less than 2 pF.

Aperture delay $t_{d(A)}$ is measured from the 1.5-V level of the CLK input to the actual sampling instant.

The OE signal is asynchronous.

OE timing t_{dis} is measured from the $V_{IH(min)}$ level of OE to the high-impedance state of the output data. The digital output load is not higher than 10 pF.

OE timing t_{en} is measured from the $V_{IL(max)}$ level of OE to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10 pF.

PRINCIPLES OF OPERATION

definitions of specifications and terminology (continued)

pipeline delay (latency)

The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipeline is full, new valid output data is provided on every clock cycle. In order to know when data is stable on the output pins, the output delay time $t_{d(o)}$ (i.e., the delay time through the digital output buffers) needs to be added to the pipeline latency. Note that since the max $t_{d(o)}$ is more than 1/2 clock period at 80 MHz, data cannot be reliably clocked in on a rising edge of CLK at this speed. The falling edge should be used.

The THS0842 implements a high-speed 40 MSPS converter in a cost effective CMOS process. Powered from 3.3 V, the single pipeline design architecture ensures low power operation and 8-bit accuracy. Signal inputs are differential and the clock signal is single ended. The digital inputs are 3.3 V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Therefore, the converter forms a self-contained solution. Alternatively, the user may apply externally generated reference voltages. In doing so, both input offset and input range can be modified to suit the application.

The analog input signal is captured by a high speed sampling and hold. Multiple stages will generate the output code with a pipeline delay of 6.5 CLK cycles. Correction logic combines the multistage data and aligns the 8-bit output word. All digital logic operates at the rising edge of CLK.

analog input

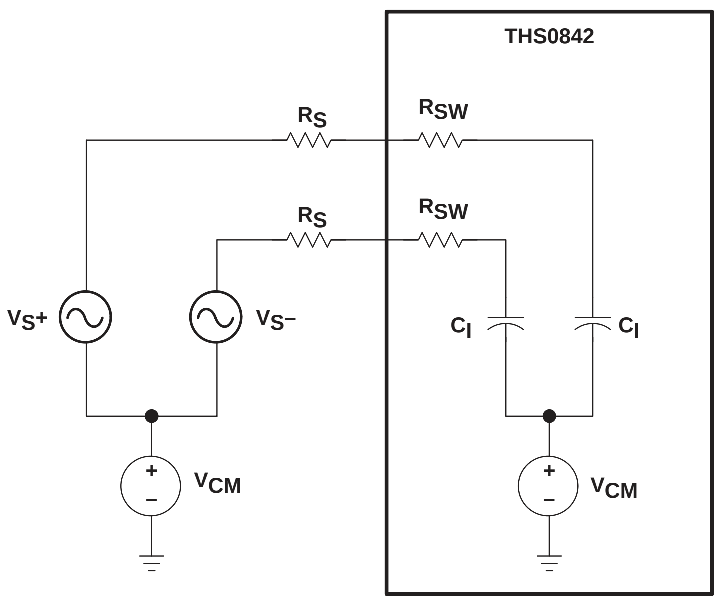


Figure 18. Simplified Equivalent Input Circuit

A first-order approximation for the equivalent analog input circuit of the THS0842 is shown in Figure 18. The equivalent input capacitance C_I is 5 pF typical. The input must charge/discharge this capacitance within the sample period of one half of a clock cycle. When a full-scale voltage step is applied, the input source provides the charging current through the switch resistance R_{SW} (200 Ω) of S1 and quickly settles. In this case the input impedance is low. Alternatively, when the source voltage equals the value previously stored on C_I, the hold capacitor requires no input current and the equivalent input impedance is very high.

PRINCIPLES OF OPERATION

analog input (continued)

To maintain the frequency performance outlined in the specifications, the total source impedance should be limited to the following equation with f_{CLK} = 80 MHz, C_I = 5 pF, R_{SW} = 200 Ω:

$$R_S < \left[1 \div \left(2f_{CLK} \times C_I \times \ln(256)\right) - R_{SW}\right]$$

So, for applications running at a lower f_{CLK}, the total source resistance can increase proportionally.

The analog input of the THS0842 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 20) will deliver the best performance from the converter. A dc voltage source, CML, equal to 1.5 V (typical for AV_{DD} = 3 V), is made available to the user to help simplify circuit design when using an ac coupled differential input. This low output impedance voltage source(300 Ω, typical) is not designed to be a reference or to be loaded, but makes an excellent dc bias source and stays well within the analog input common mode voltage range over temperature. If load on that pin is foreseen, the use of an external buffer is recommended. Defining VREFD = VREFT – VREFB, each single-ended analog input is limited to be between VCML + VREFD/2 and VCML – VREFD/2. See Table 1 for the minimum and maximum reference input levels.

For the ac-coupled differential input with AV_{DD} = 3 V (see Figure 23), full scale is achieved when the +I/Q and –I/Q input signals are 0.5 VPP, with –I/Q being 180 degrees out of phase with +I/Q. The converter will be at positive full scale when the +I/Q input is at CML + 0.25 V and the –I/Q input is at CML – 0.25 V (+I/Q + I/Q – = 0.5 V). Conversely, the converter will be at negative full scale when the +I/Q input is equal to CML – 0.25 V and –I/Q is at CML + 0.25 V (I/Q+ + I/Q– = –0.5 V) (see Figure 19).

PRINCIPLES OF OPERATION

analog input (continued)

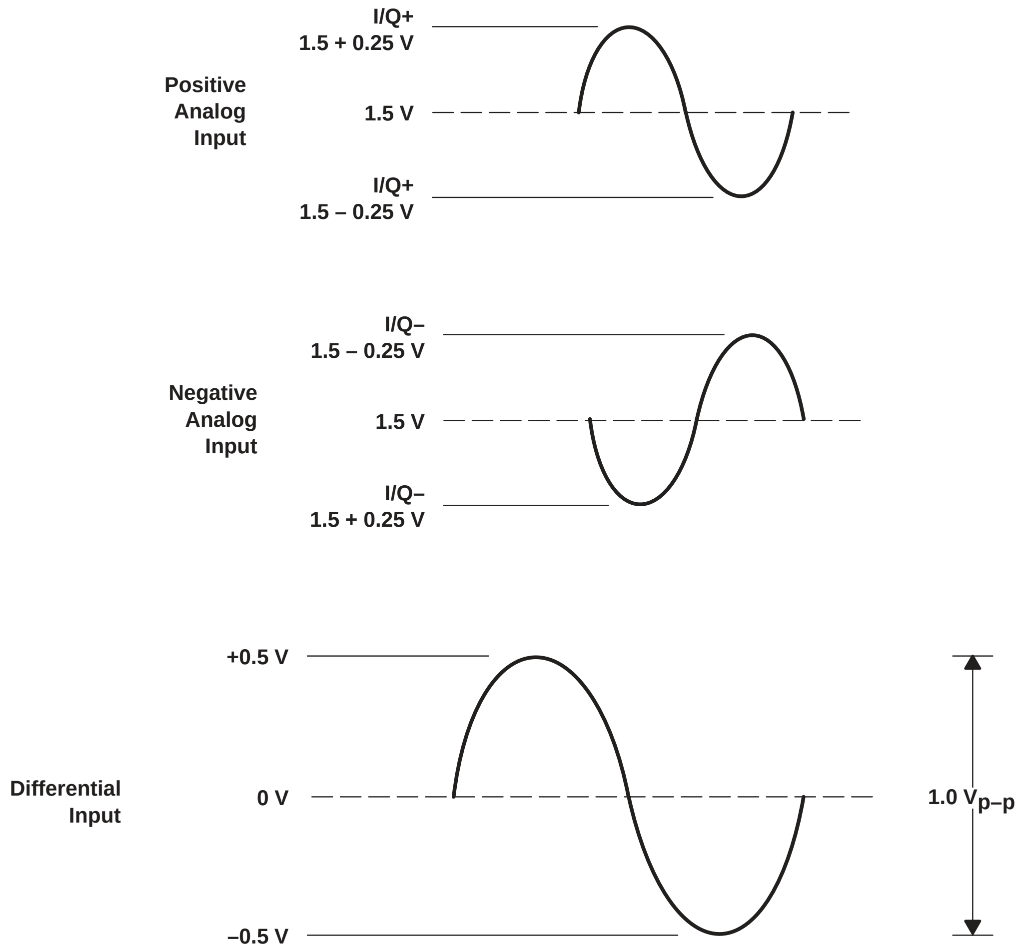


Figure 19. Differential Input Waveform With AV_{DD} = 3 V

The analog input can be dc coupled (see Figure 21) as long as the inputs are within the analog input common mode voltage range. For example (see Figure 21), V+ and V– are signals centered on GND with a peak-to-peak voltage of 2 V, and the circuit in Figure 21 is used to interface it with the THS0842. Assume AV_{DD} of the converter is 3 V. Two problems have to be solved. The first is to shift CML from 0 V to 1.5 V (AV_{DD}/2). To do that, a V_{bias} voltage and an adequate ratio of R1 and R2 have to be selected. For instance, if V_{bias} = AV_{DD} = 3 V, then R1 = R2. The second is that the differential voltage has to be reduced from 4 V (2 x 2 V) to 1 V, and for that an attenuation of 4 to1 is needed. The attenuation is determined by the relation: (R3||2R2)/((R3||2R2) + 2R1). One possible solution is R1 = R2 = R3 = 150 Ω. In this case, moreover, the input impedance (2R1 + (R3||2R2)) will be 400 Ω. The values can be changed to match any other input impedance. A capacitor, C, connected from I/Q IN+ to I/Q IN– will help filter any high frequency noise on the inputs, also improving performance. Note, that the chosen value of capacitor C must take into account the highest frequency component of the analog input signal.

PRINCIPLES OF OPERATION

ac coupled input

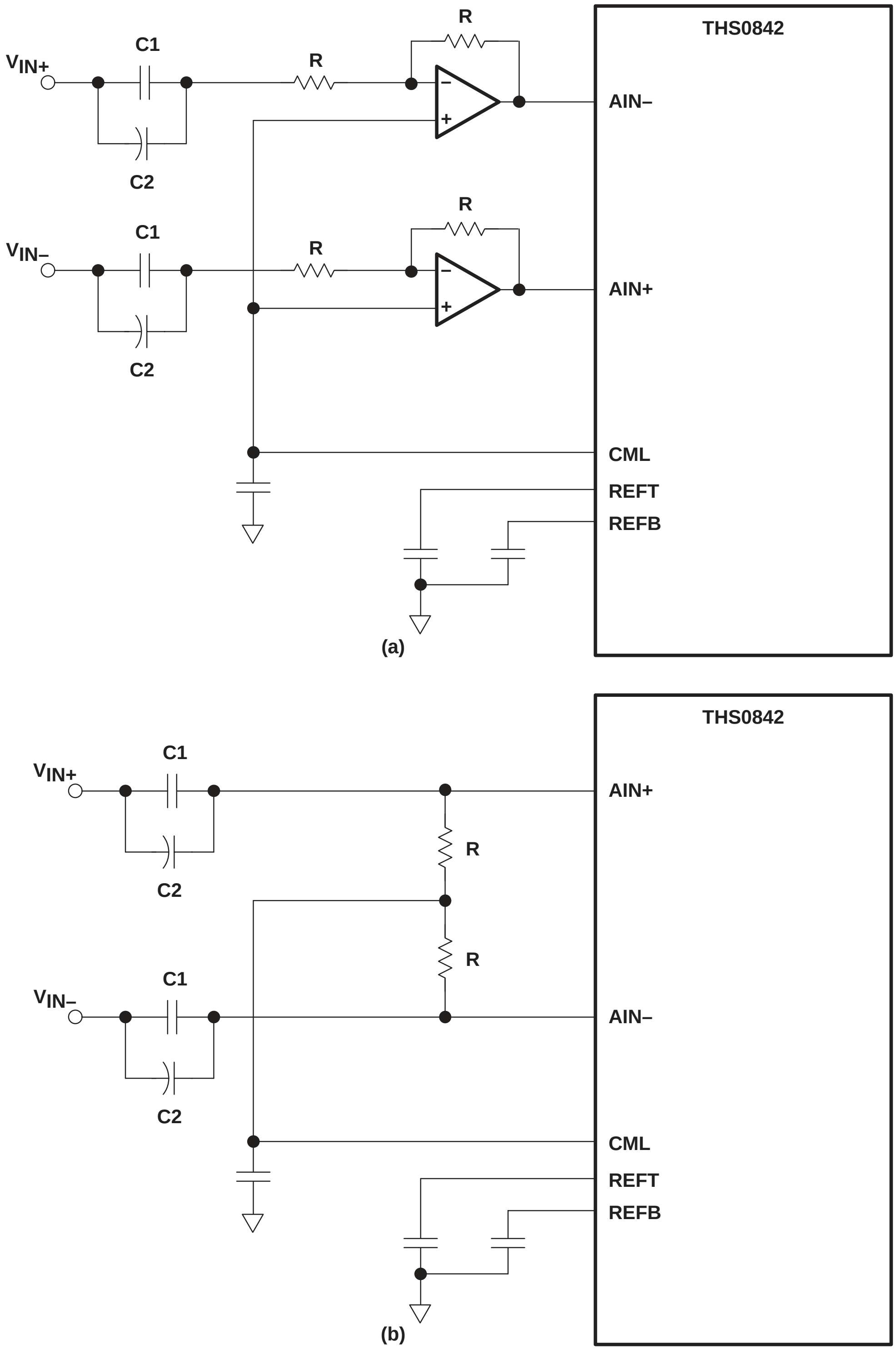


Figure 20. AC-Coupled Differential Input Circuits

PRINCIPLES OF OPERATION

ac coupled input (continued)

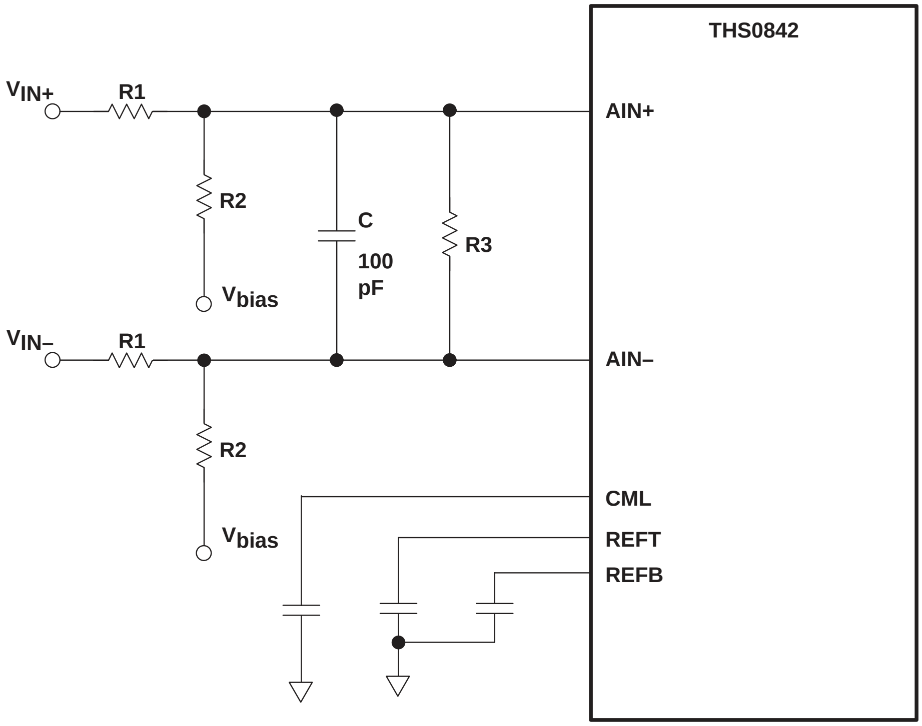


Figure 21. DC-Coupled Differential Input Circuit

For many applications, ac coupling offers a convenient way for biasing the analog input signal at the proper signal range. Figure 20 shows a typical configuration. To maintain the outlined specifications, the component values need to be carefully selected. The most important issue is the positioning of the 3 dB high-pass corner point $f_{-3\ dB}$, which is a function of R ($R_S + R_{SW}$ as shown in Figure 18) and the parallel combination of C_1 and C_2, called C_{eq}. This is given by the following equation:

$$f_{-3\ dB} = 1 \div \left(2\pi \times R \times C_{eq}\right)$$

Since C1 is typically a large electrolytic or tantalum capacitor, the impedance becomes inductive at higher frequencies. Adding a small ceramic or polystyrene capacitor, C2 of approximately 0.01 µF, which is not inductive within the frequency range of interest, maintains low impedance.

analog input, single-ended connection

The configuration shown in Figure 23 may be used with a single-ended ac coupled input. If I/Q is a 1 V_{pp} sinewave, then I/Q IN+ is a 1 V_{pp} sinewave riding on a positive voltage equal to CML (see Figure 22). The converter will be at positive full scale when I/Q IN+ is at CML+0.5V (I/Q IN+ – I/Q IN– = 0.5 V) and will be at negative full scale when I/Q IN+ is equal to CML – 0.5 V (I/Q IN+ – I/Q IN– = –0.5 V). Sufficient headroom must be provided such that the input voltage never goes above 3.3 V or below AGND. The simplest way is to use the dc bias source output (CML) of the THS0842.

PRINCIPLES OF OPERATION

analog input, single-ended connection (continued)

The single ended analog input can be dc coupled (Figure 24) as long as the input is within the analog input common mode voltage range. A capacitor, C, connected from I/Q IN+ to I/Q IN– will help filter any high frequency noise on the inputs, also improving performance. Note, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

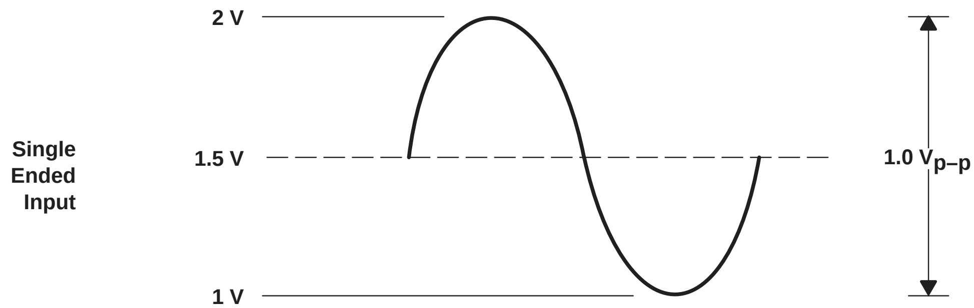


Figure 22. Single-Ended Input Waveform With AV_{DD} = 3 V

A single-ended source may give better overall system performance if it is first converted to differential before driving the THS0842.

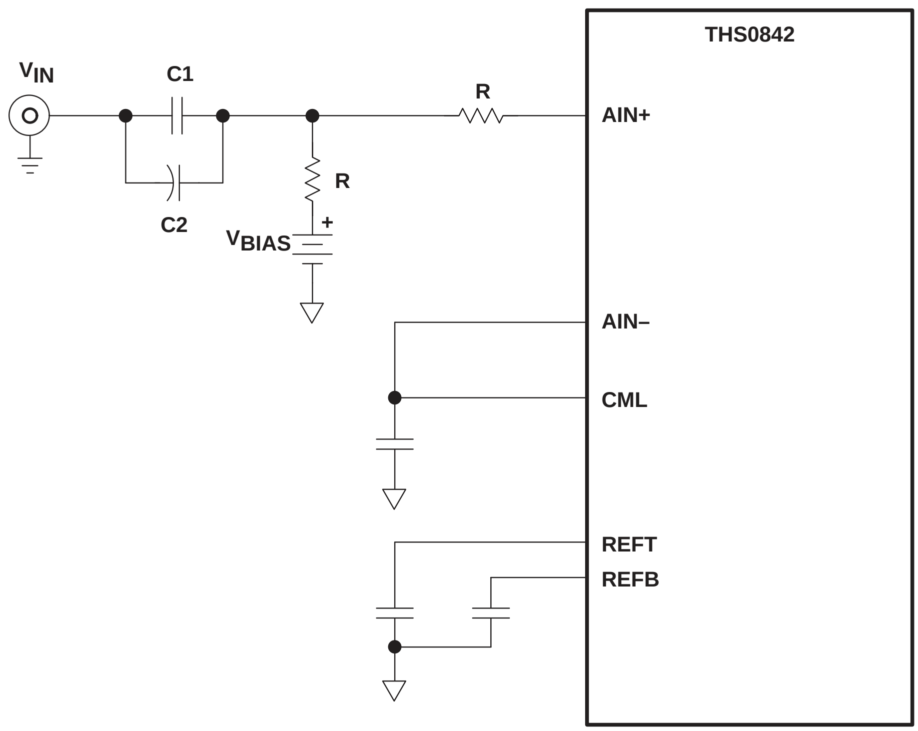


Figure 23. AC-Coupled Input

PRINCIPLES OF OPERATION

dc coupled input

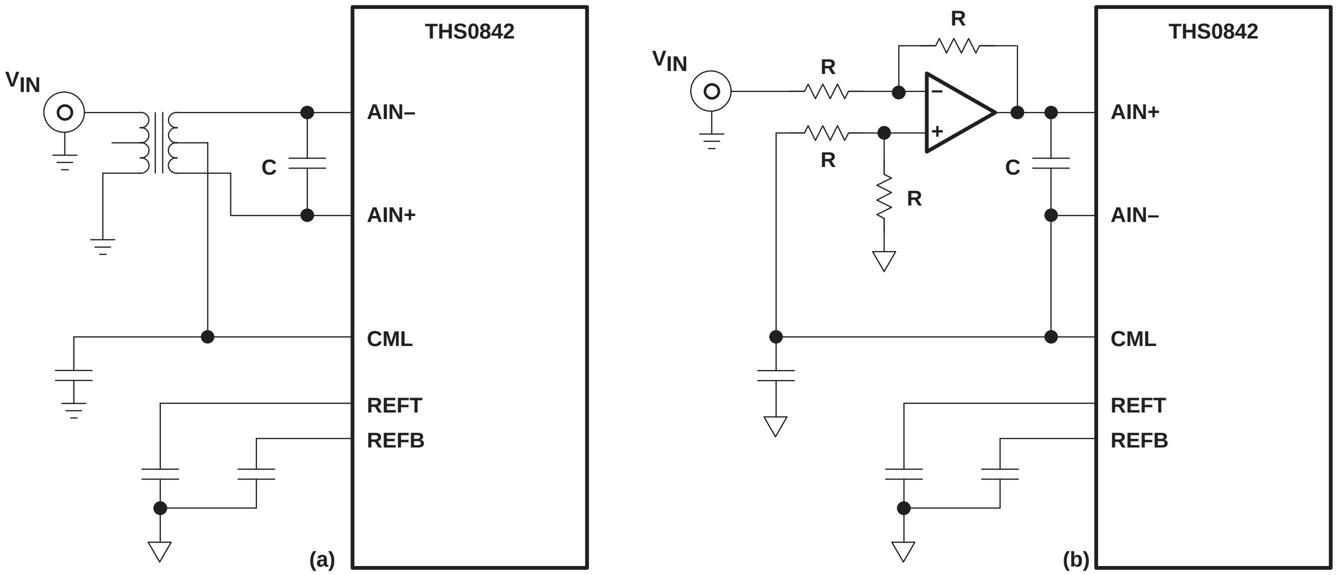


Figure 24. DC-Coupled Input Circuits

For dc-coupled systems, an op-amp can level shift a ground referenced input signal. A circuit like Figure 24(b) could be used. In this case, the AIN voltage is given by: AIN = $-V_{IN} + V_{CML}$

reference terminals

The THS0842 input voltage range is determined by the voltages on terminals REFBI and REFTI. Since the device has an internal voltage reference generator, it must be placed in power down before applying an external voltage to the REFT and REFB pins. Especially at higher sampling rates, it is advantageous to have a wider analog input range. This can be achievable by using external voltage references (e.g., at AV_{DD} = 3.3 V, the full scale range can be extended from 1 V_{pp} (internal reference) to 1.3 V_{pp} (external reference) as shown in Table 1). These voltages should not be derived via a voltage divider from a power supply source. Instead, use a bandgap-derived voltage reference to derive both references via an op-amp circuit. Refer to the schematic of the THS0842 evaluation module in this datasheet for an example circuit.

When using external references, the full-scale ADC input range and its dc position can be adjusted. The full-scale ADC range is always equal to $V_{REFT} - V_{REFB}$. The maximum full-scale range is dependent on AV_{DD} as shown in the specification section. Next to the constraint on their difference, there are limitations on the useful range of V_{REFT} and V_{REFB} individually as well, dependent also on AV_{DD}.

Table 1 summarizes these limits for 3 cases.

Table 1. Min/Max Reference Input Levels

AV_{DD}	$V_{REFB(min)}$	$V_{REFB(max)}$	$V_{REFT(min)}$	$V_{REFT(max)}$	$[V_{REFT}-V_{REFB}]_{max}$
3 V	0.8 V	1.2 V	1.8 V	2.2 V	1 V
3.3 V	0.8 V	1.2 V	2.1 V	2.5 V	1.3 V
3.6 V	0.8 V	1.2 V	2.4 V	2.8 V	1.6 V

PRINCIPLES OF OPERATION

digital inputs

The digital inputs are CLK, STDBY, PWDN_REF, and $\overline{OE}$. All these signals, except CLK, have an internal pulldown resistor to connect to digital ground. This provides a default active operation mode using internal references when left unconnected.

The CLK signal at high frequencies should be considered as an analog input. Overshoot/undershoot should be minimized by proper termination of the signal close to the THS0842. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency (f) and resolution (2^N) of a signal that needs to be sampled and the maximum amount of aperture error dt_{max} that is tolerable. The following formula shows the relation:

$$dt_{max} = 1 \div \left[\pi\ f\ 2^{(N+1)}\right]$$

As an example, for an 8-bit converter with a 15-MHz input, the jitter needs to be kept <41 pS in order not to have changes in the LSB of the ADC output due to the total aperture error.

digital outputs

The output of THS0842 is straight binary code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10 pF is recommended) to provide best performance. Higher output loading causes higher dynamic output currents and can increase noise coupling into the device analog front end. To drive higher loads, use an output buffer is recommended. See Figure 25 through Figure 28 for examples.

When clocking output data from the THS0842, it is important to observe its timing relation to COUT. See Note 6 in the specification section for more details.

PRINCIPLES OF OPERATION

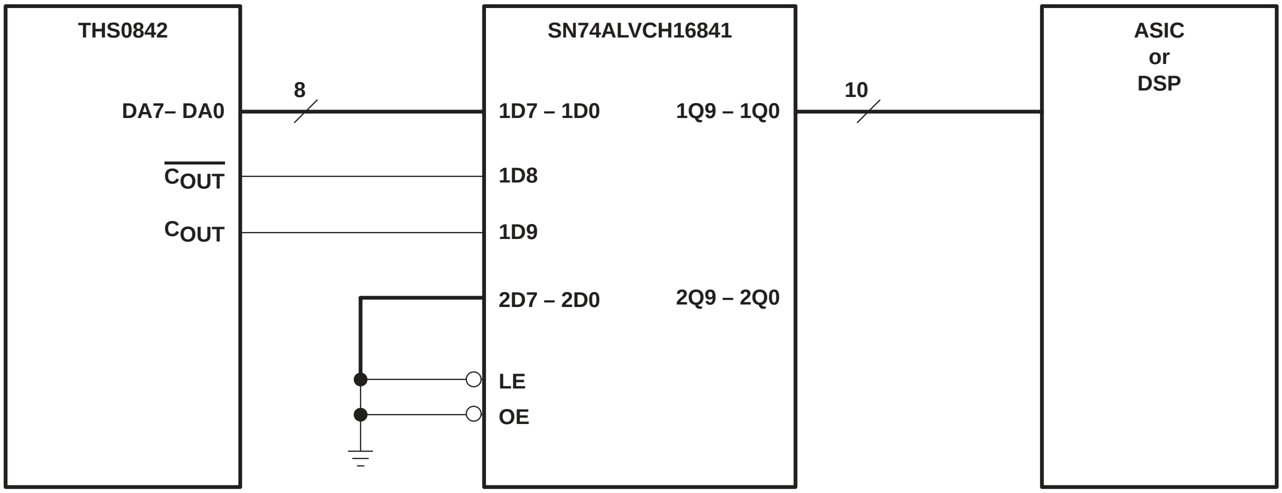


Figure 25. Single Bus Connection Example

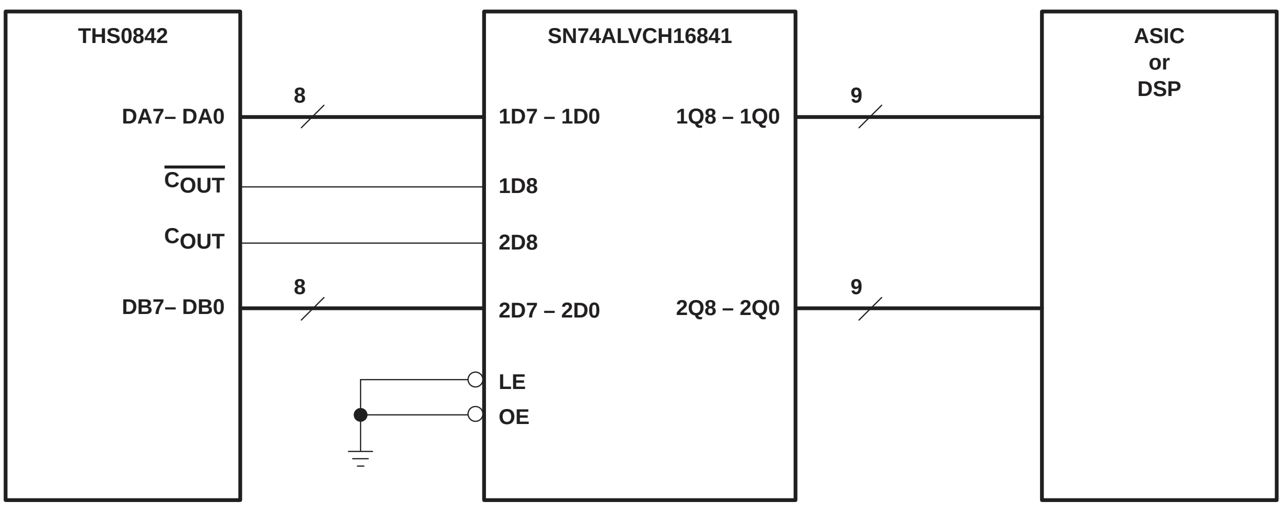


Figure 26. Dual Bus Connection Example

NOTE: The SN74ALVCH16841 latches are used to buffer the THS8042 and C_{OUT} pins.

PRINCIPLES OF OPERATION

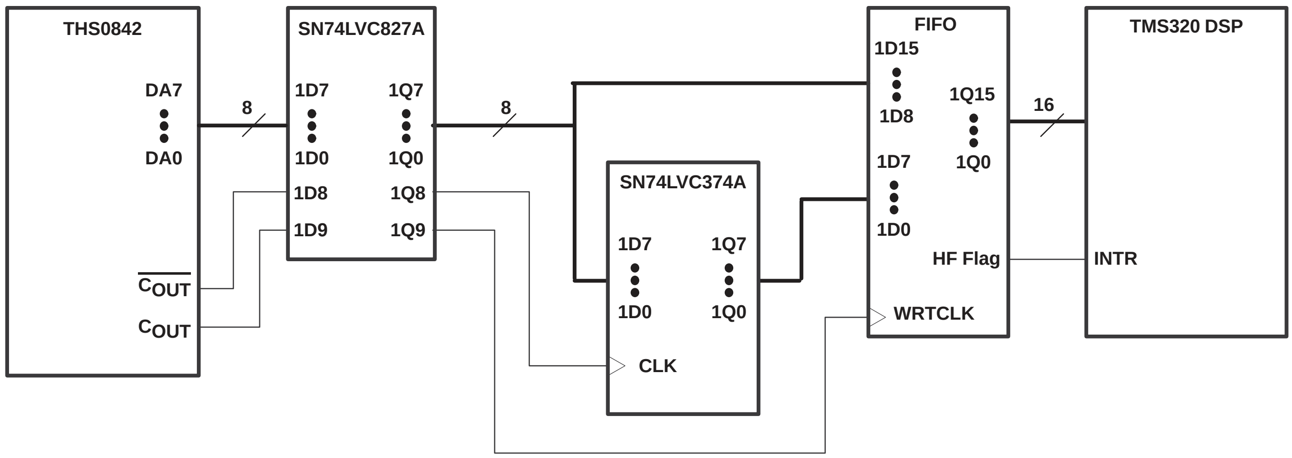


Figure 27. Single Bus FIFO Connection to DSP Example

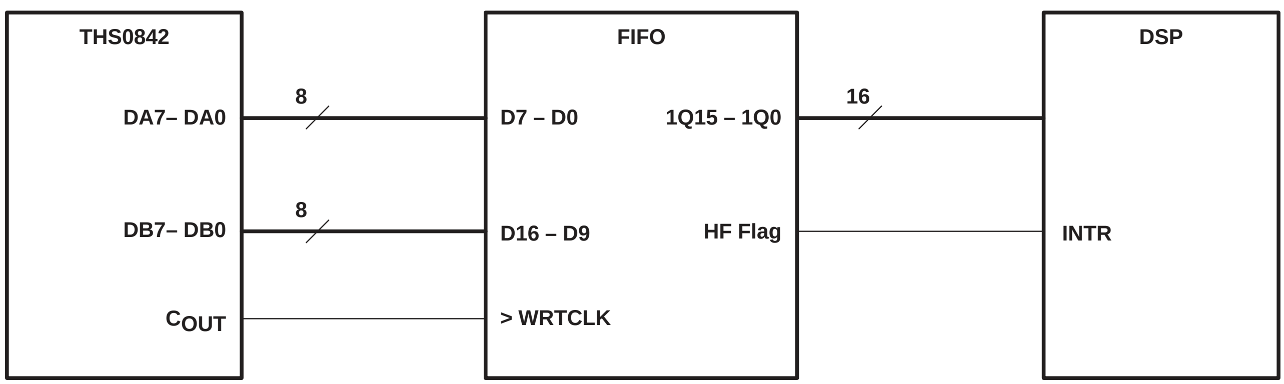


Figure 28. Dual Bus FIFO Connection to DSP Example

layout, decoupling and grounding rules

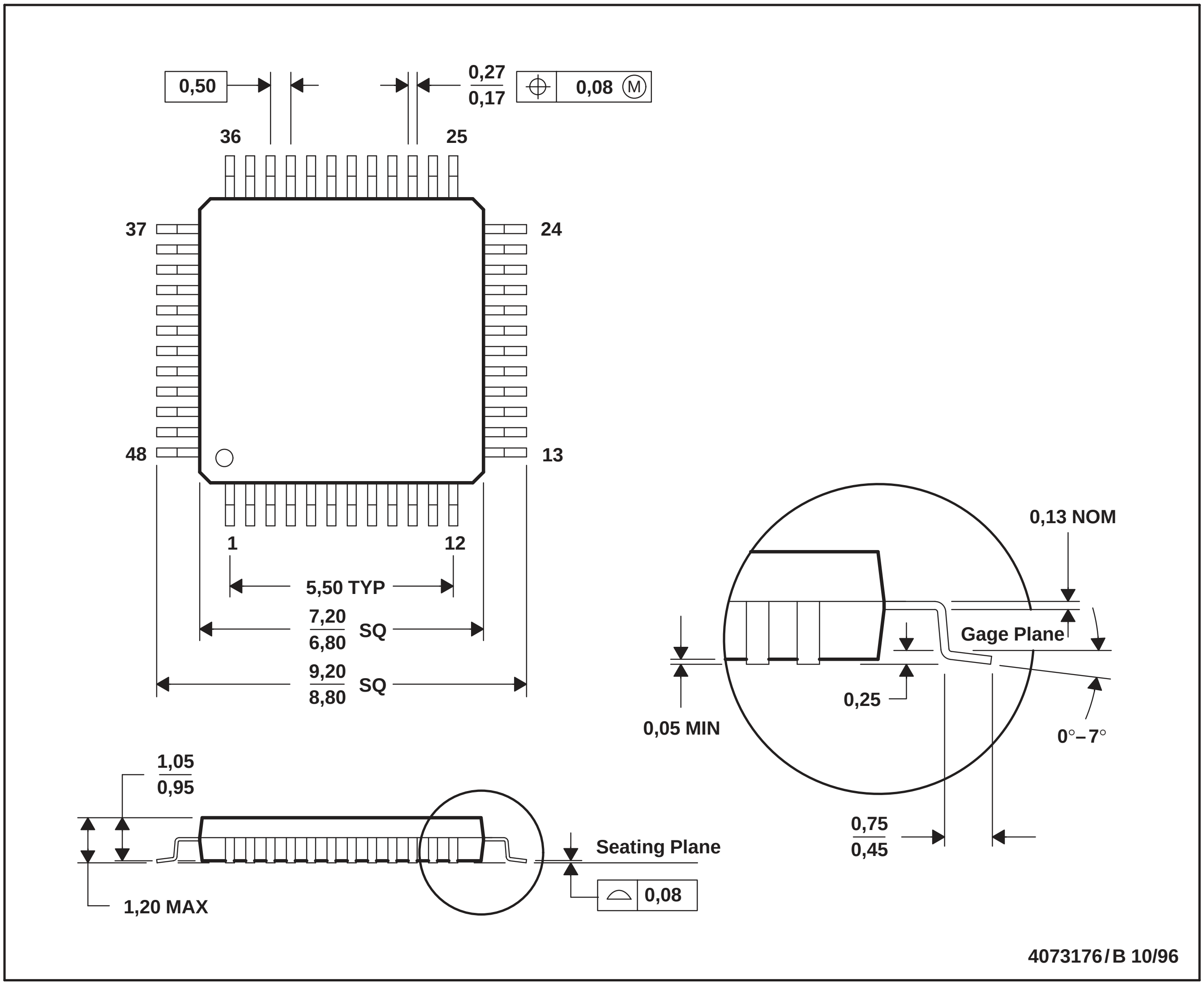
Proper grounding and layout of the PCB on which the THS0842 is populated are essential to achieve the stated performance. It is advisable to use separate analog and digital ground planes that are spliced underneath the device. The THS0842 has digital and analog terminals on opposite sides of the package to make this easier. Since there is no internal connection between analog and digital grounds, they have to be joined on the PCB. It is advisable to do this at one point in close proximity to the THS0842.

As for power supplies, separate analog and digital supply terminals are provided on the device (AV_{DD}/DV_{DD}). The supply to the digital output drivers is kept separate also (DRV_{DD}). Lowering the voltage on this supply to 3 V instead of the nominal 3.3 V improves performance because of the lower switching noise caused by the output buffers.

Because of the high sampling rate and switched-capacitor architecture, THS0842 generates transients on the supply and reference lines. Proper decoupling of these lines is essential. Decoupling as shown in the schematic of the THS0842 EVM is recommended.

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS0842IPFB	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TJ0842	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

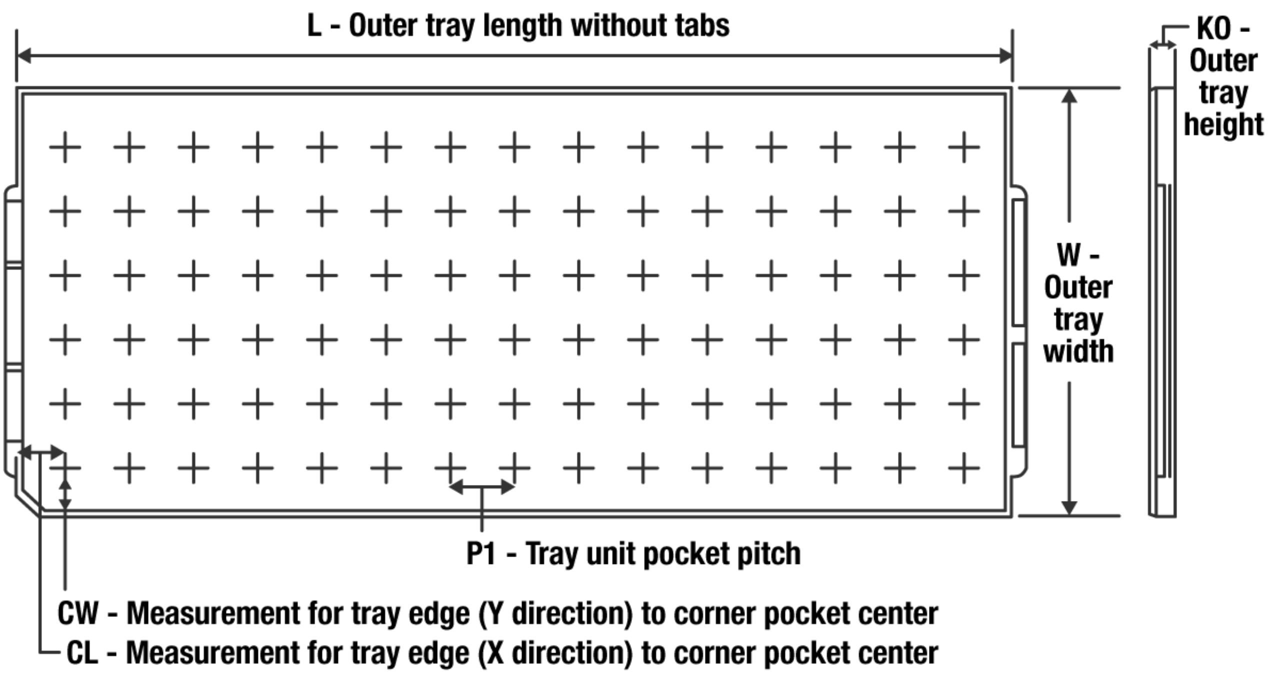
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
THS0842IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25