N-Channel Power MOSFET

800V, 3A, 4.2Ω

FEATURES

- Low $R_{DS(ON)}$ 3.3Ω (Typ.)
- Low gate charge typical @ 19nC (Typ.)
- Low Crss typical @ 10.2pF (Typ.)
- Improved dv/dt capability

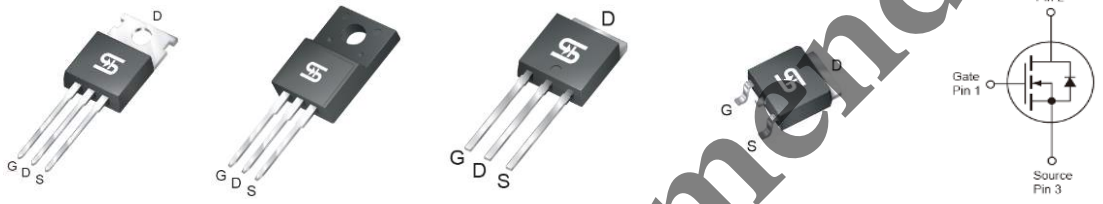
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	800	V
$R_{DS(on)}$ (max)	4.2	Ω
Q_g	19	nC

APPLICATION

- Power Supply
- Lighting

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-220 **ITO-220** **TO-251(IPAK)** **TO-252(DPAK)**



Notes: MSL 3 (Moisture Sensitivity Level) for TO-252 (D-PAK) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT			UNIT
		IPAK/DPAK	ITO-220	TO-220	
Drain-Source Voltage	V_{DS}	800			V
Gate-Source Voltage	V_{GS}	±30			V
Continuous Drain Current (Note 1) T_C = 25°C	I_D	3			A
Continuous Drain Current (Note 1) T_C = 100°C	I_D	1.83			A
Pulsed Drain Current (Note 2)	I_{DM}	12			A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	48			mJ
Single Pulsed Avalanche Current (Note 3)	I_{AS}	3			A
Repetitive Avalanche Energy (Note 3)	E_{AR}	9.4			mJ
Repetitive Avalanche Energy (Note 4)	dV/dt	4.5			V/ns
Total Power Dissipation @ T_C = 25°C	P_{DTOT}	94	32	94	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150			°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT			UNIT
		IPAK/DPAK	ITO-220	TO-220	
Junction to Case Thermal Resistance	$R_{\Theta JC}$	1.33	3.9	1.33	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	110	62.5		°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 5)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	800	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2	--	4	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 800V, V_{GS} = 0V	I_{DSS}	--	--	10	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 1.5A	$R_{DS(ON)}$	--	3.3	4.2	Ω
Forward Transfer Conductance	V_{DS} = 30V, I_D = 1.5A	g_{fs}	--	3.7	--	S
Dynamic (Note 6)						
Total Gate Charge	V_{DS} = 640V, I_D = 3A, V_{GS} = 10V	Q_g	--	19	--	nC
Gate-Source Charge		Q_{gs}	--	4	--	
Gate-Drain Charge		Q_{gd}	--	7.6	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	696	--	pF
Output Capacitance		C_{oss}	--	65	--	
Reverse Transfer Capacitance		C_{rss}	--	10.2	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	3.2	--	Ω
Switching (Note 7)						
Turn-On Delay Time	V_{GS} = 10V, I_D = 3A, V_{DD} = 400V, R_G =25Ω	$t_{d(on)}$	--	48	--	ns
Turn-On Rise Time		t_r	--	36	--	
Turn-Off Delay Time		$t_{d(off)}$	--	106	--	
Turn-Off Fall Time		t_f	--	41	--	
Source-Drain Diode (Note 5)						
Source Current	Integral reverse diode in the MOSFET	I_S	--	--	3	A
Source Current (Pulse)		I_{SM}	--	--	12	A
Diode Forward Voltage	I_S = 3A, V_{GS} = 0V	V_{SD}	--	--	1.5	V
Reverse Recovery Time	V_{GS} = 0V, I_S =3A, dI_F/dt = 100A/us	t_{rr}	--	370	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.8	--	μC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. L = 10mH, I_{AS} = 3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 3A, dI/dt ≤ 200A/uS, V_{DD} ≤ BV_{DSS}, Starting T_J = 25ºC
5. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%
6. For DESIGN AID ONLY, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM3N80CZ C0G	TO-220	50pcs / Tube
TSM3N80CI C0G	ITO-220	50pcs / Tube
TSM3N80CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM3N80CP ROG	TO-252 (DPAK)	2,500pcs / 13” Reel

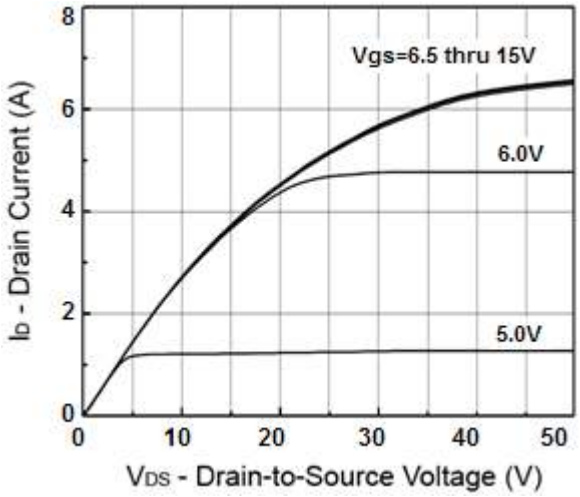
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

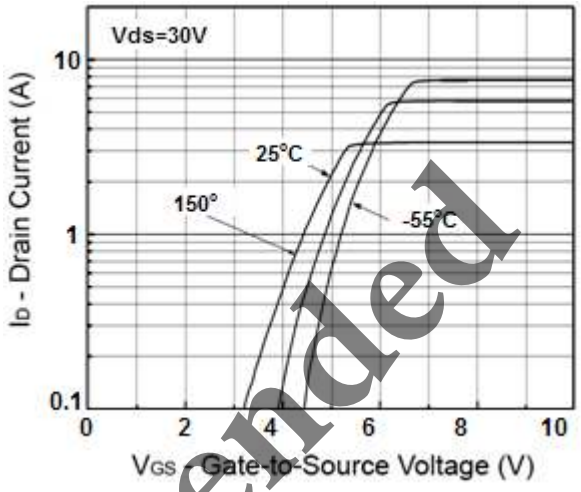
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

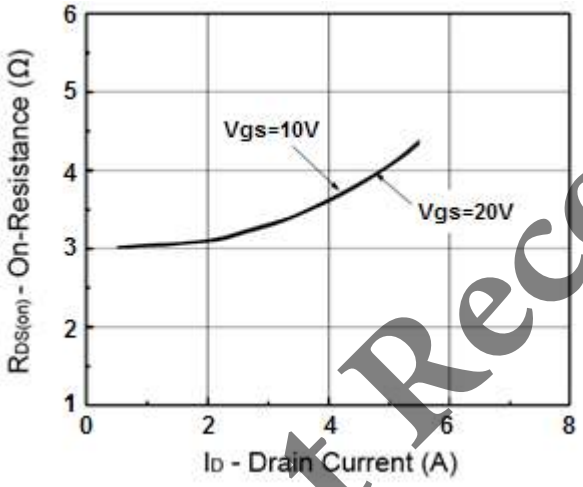
Output Characteristics



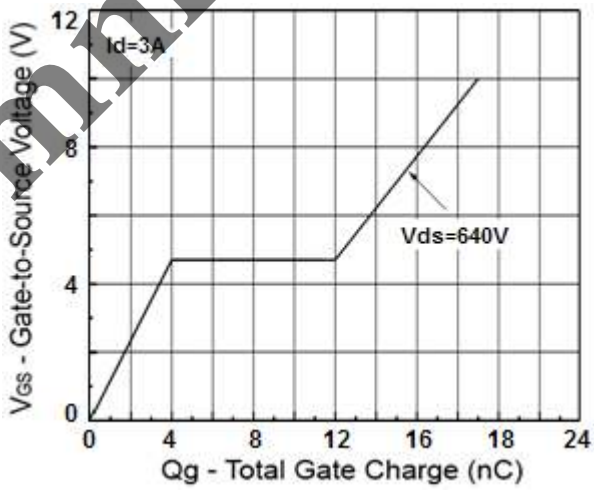
Transfer Characteristics



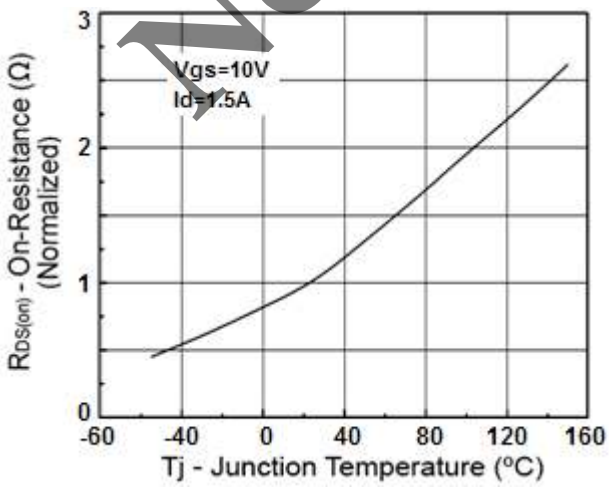
On-Resistance vs. Drain Current



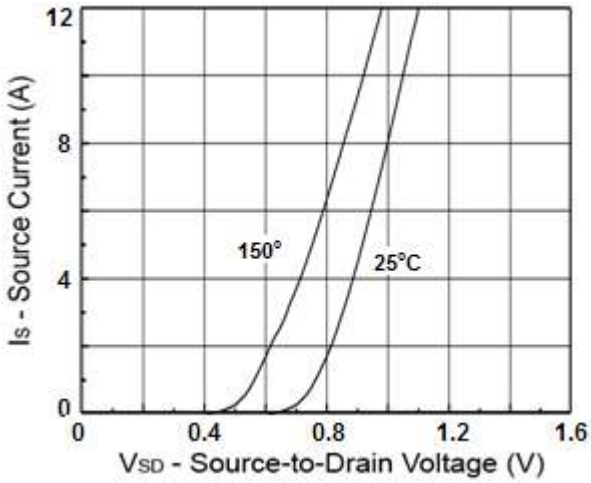
Gate Charge



On-Resistance vs. Junction Temperature



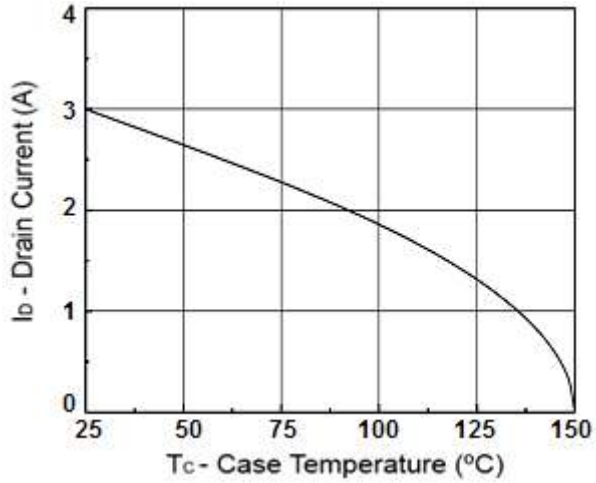
Source-Drain Diode Forward Voltage



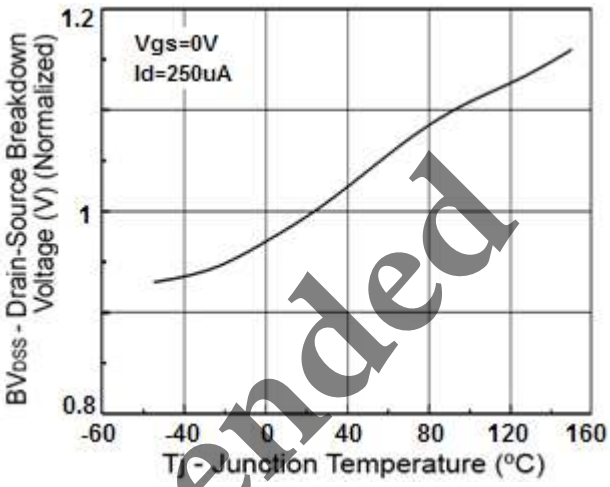
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

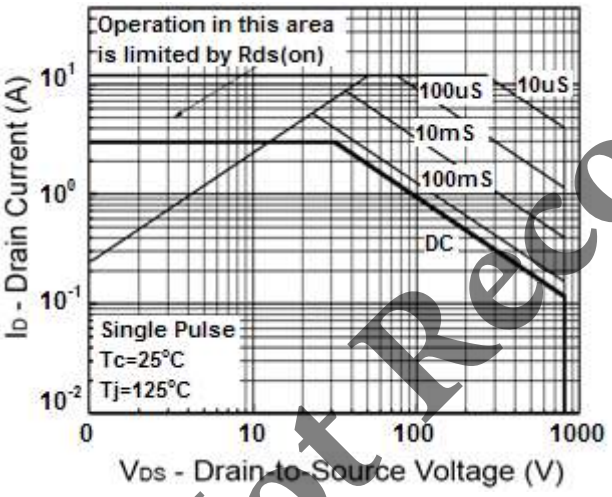
Drain Current vs. Case Temperature



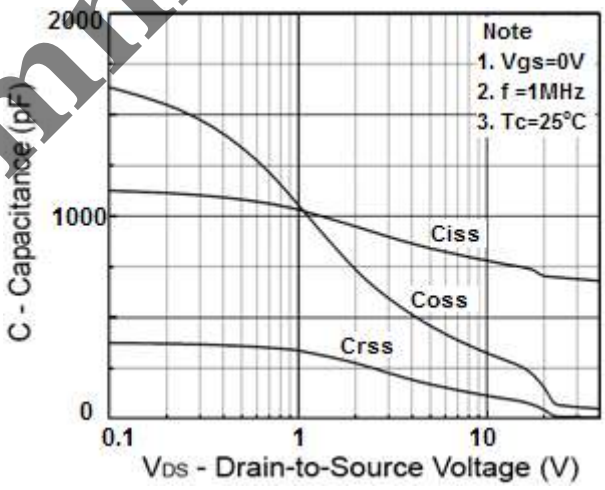
BV_{DSS} vs. Junction Temperature



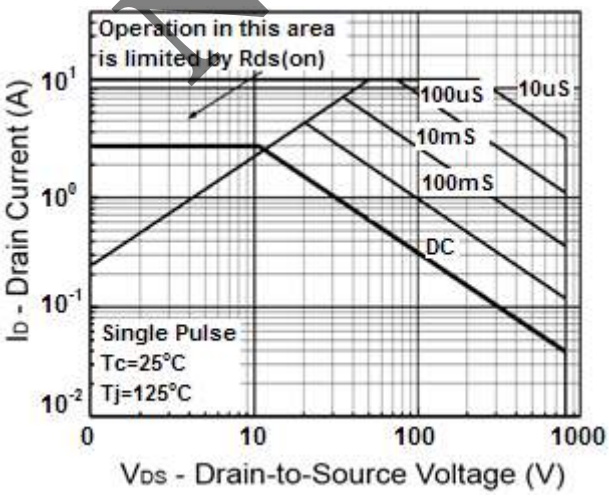
Maximum Safe Operating Area(TO-220, I/D-PAK)



Capacitance vs. Drain-Source Voltage



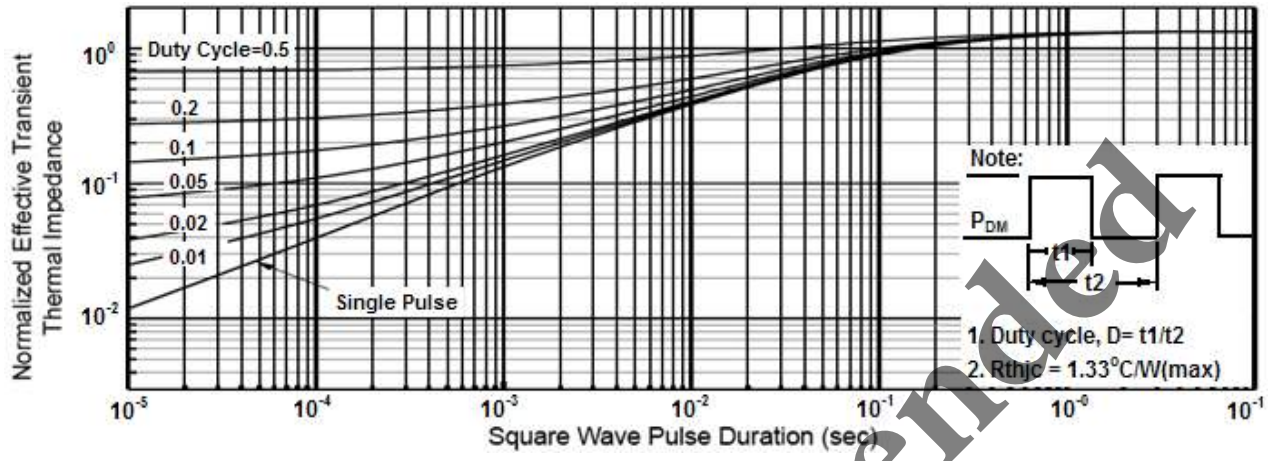
Maximum Safe Operating Area(ITO-220)



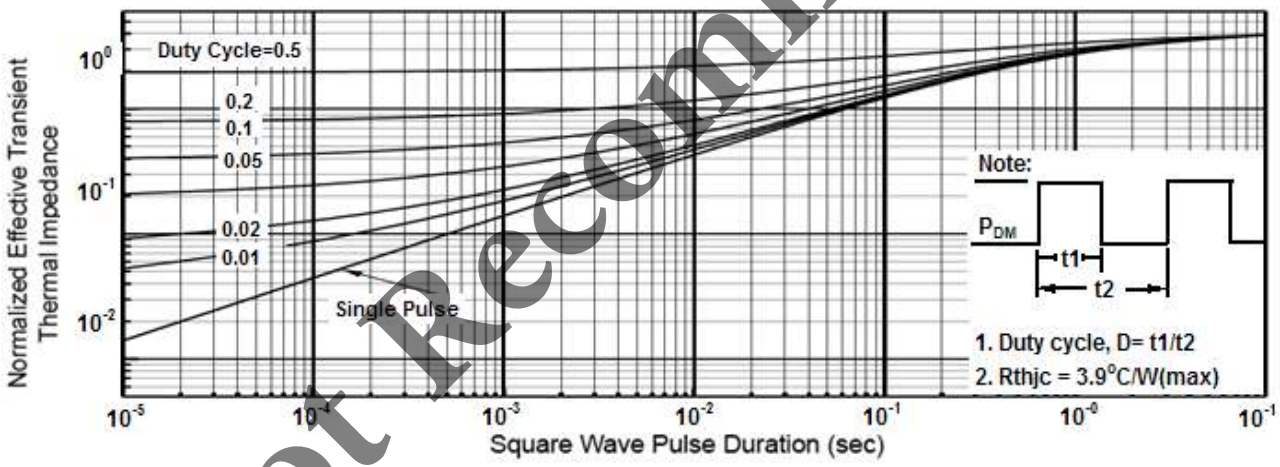
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient (TO-220, I/D-PAK)

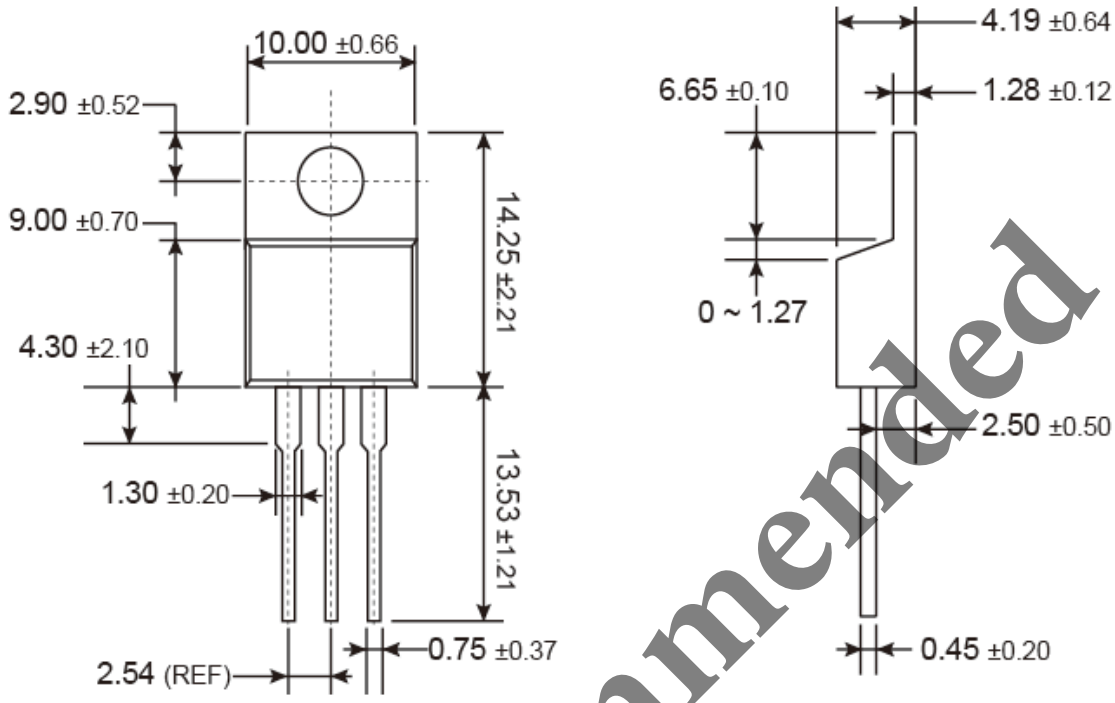


Normalized Thermal Transient Impedance, Junction-to-Ambient (ITO-220)

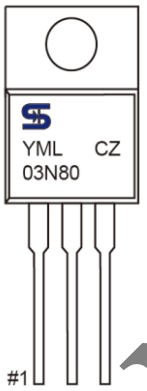


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-220



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O	=Jan	**P**	=Feb	**Q**	=Mar	**R**	=Apr
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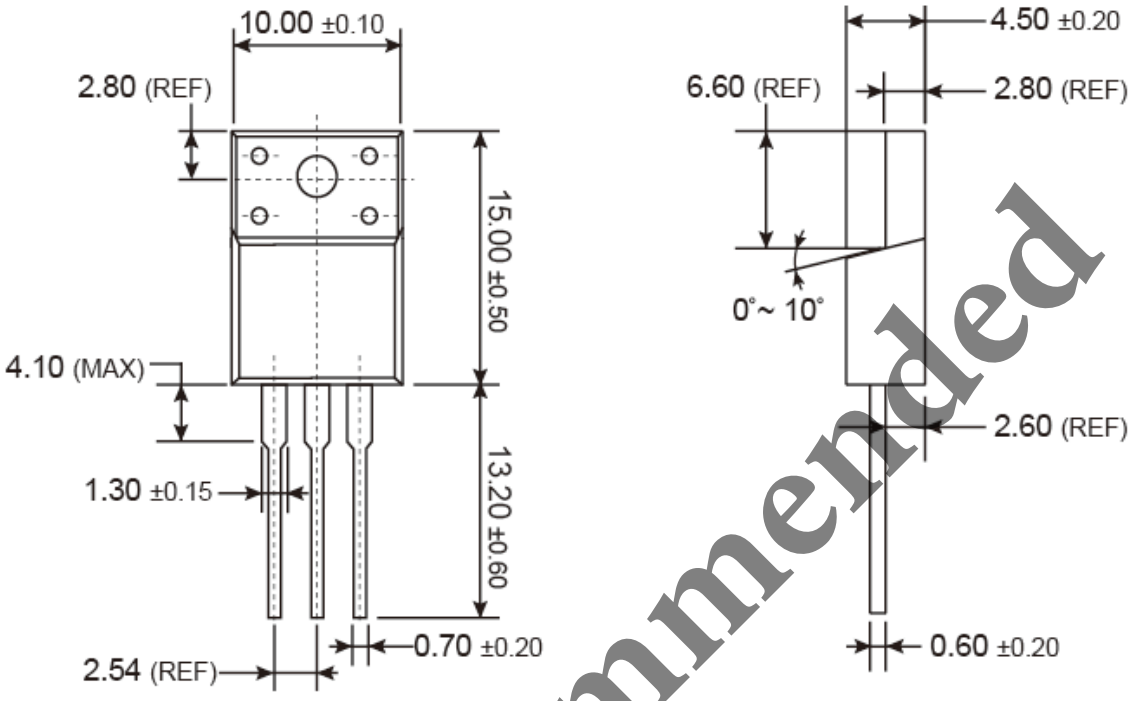
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

ITO-220



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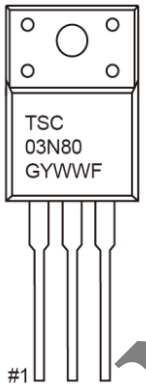
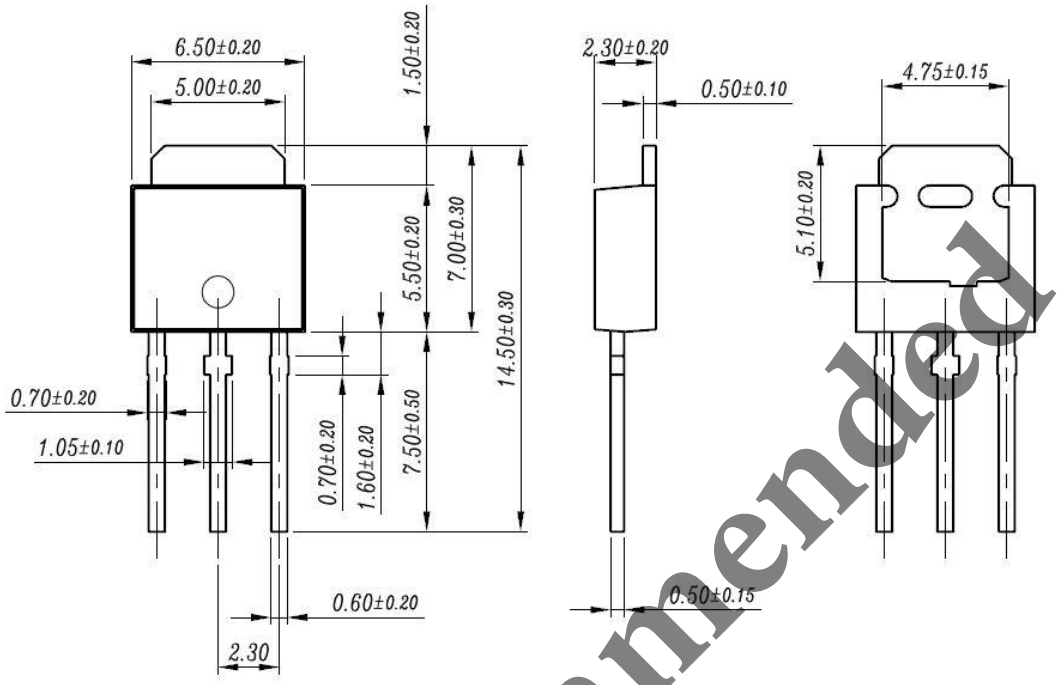


G = Halogen Free
Y = Year Code
WW = Week Code (01~52)
F = Factory Code

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251(IPAK)



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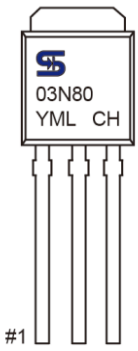

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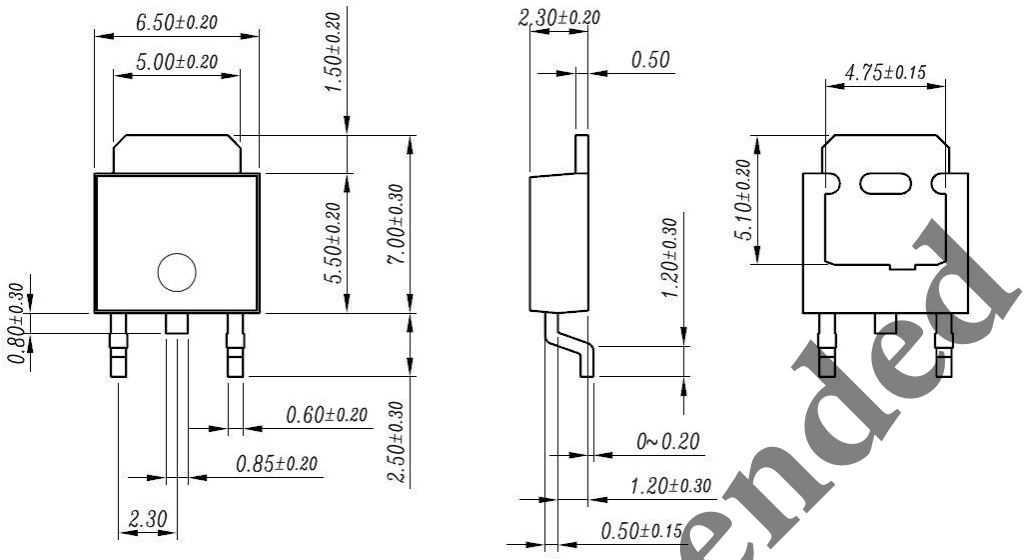
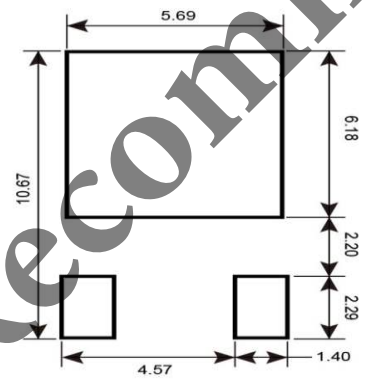
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252(DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



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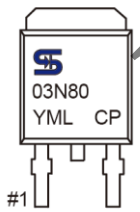

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