

January 1993

N-Channel Enhancement-Mode Power Field-Effect Transistor (MegaFET)

Features

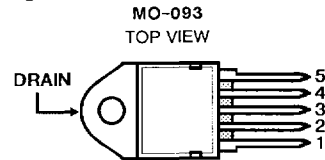
- 100A, 50V
- $r_{DS(on)} = 0.008\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

Description

The RFA100N05E n-channel ESD rated power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFA100N05E is supplied in the MO-093 plastic package.

Package

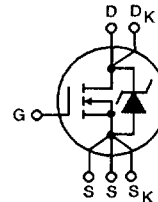


TERMINAL CONNECTIONS

- 1 - Gate
- 2 - Source Kelvin
- 3 - Drain Kelvin
- 4 - Source Current
- 5 - Source Current

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	RFA100N05E	UNITS
Drain-Source Voltage	V_{DSS}	V
Drain-Gate Voltage ($R_{GS} = 1\text{ M}\Omega$)	V_{DGR}	V
Continuous Drain Current	100	A
Pulsed Drain Current	300	A
Gate-Source Voltage	± 20	V
Maximum Power Dissipation		
$T_C = +25^\circ\text{C}$	240	W
Derated Above 25°C	1.6	W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_{JC}, T_{STG}	$^\circ\text{C}$
Electrostatic Discharge Rating		
MIL-STD-883, Category B(2)	ESD	kV
Single-Pulse Avalanche Rating	2	kV

Refer to UIS SOA Curves

Specifications RFA100N05E

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage	B _V DSS	I _D = 0.25mA, V _{GS} = 0V	50	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} I _D = 0.25mA	2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	-	-	1	μA
		T _C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	100	nA
On Resistance	r _{DS(on)}	I _D = 100A, V _{GS} = 10V	-	-	0.008	Ω
Turn-On Time	t _(on)	V _{DD} = 25V, I _D = 50A	-	-	60	ns
Turn-On Delay Time	t _{d(on)}	R _L = 0.50Ω	-	17	-	ns
Rise Time	t _r	I _{G1} = I _{G2} = 3A	-	8	-	ns
Turn-Off Delay Time	t _{d(off)}	V _{GS(clamp)} = +10V, -0.6V	-	50	-	ns
Fall Time	t _f		-	10	-	ns
Turn-Off Time	t _(off)		-	-	100	ns
Total Gate Charge	Q _{g(tot)}	V _{GS} = 0, 20V	V _{DD} = 40V		430	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0, 10V	I _D = 100A		230	nC
Threshold Gate Charge	Q _{g(th)}	V _{GS} = 0, 2V	R _L = 0.40Ω		15	nC
Plateau Voltage	V _(plateau)	I _D = 100A, V _{DS} = 15V	-	-	7.5	V
Turn-Off Energy Loss per Cycle	E _{off}	V _{DD} = 25V, I _D = 50A, I _{G1} = I _{G2} = 3A V _{GS(clamp)} = +10V, -0.6V, L = 0.2μH, R _L = 0.50Ω	-	-	500	μJ
Thermal Resistance Junction to Case	R _{θJC}		-	-	0.625	°C/W
Thermal Resistance Diode Junction to Ambient	R _{θJA}		-	-	80	°C/W

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Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Forward Voltage	V _{SD}	I _{SD} = 100A	-	-	1.5	V
Reverse Recovery Time	t _{rr}	I _f = 100A, di _f /dt = 100A/μs	-	-	125	ns

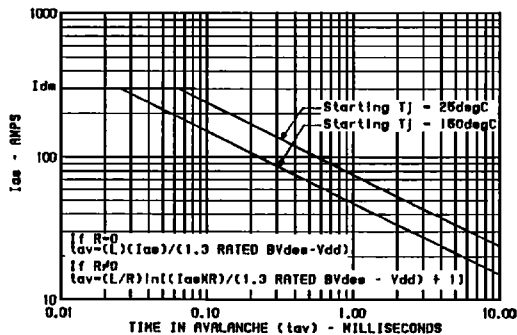


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

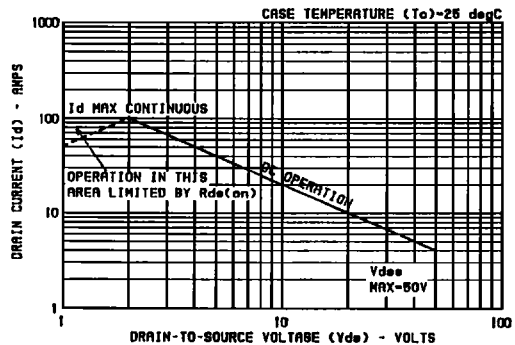


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

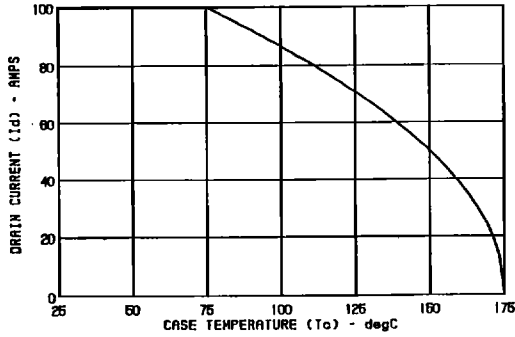


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

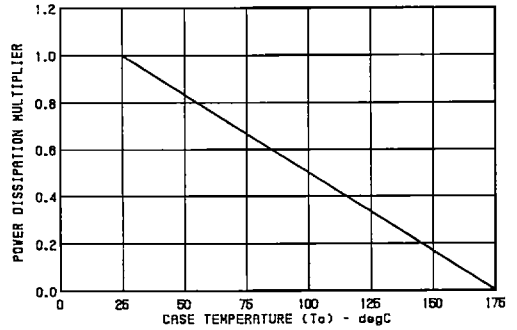


FIGURE 4. NORMALIZED POWER DISSIPATION VS. TEMPERATURE DERATING CURVE

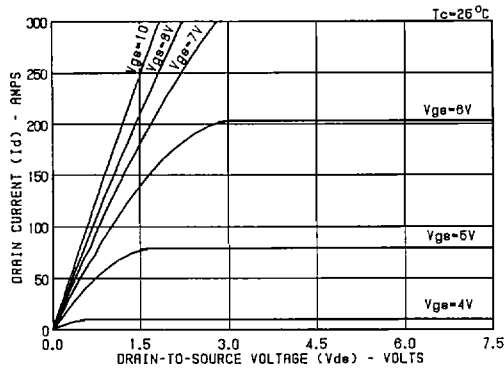


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

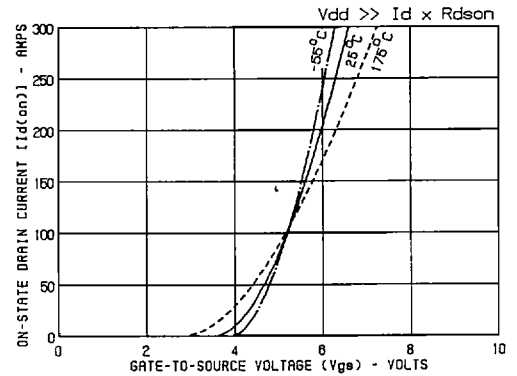


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

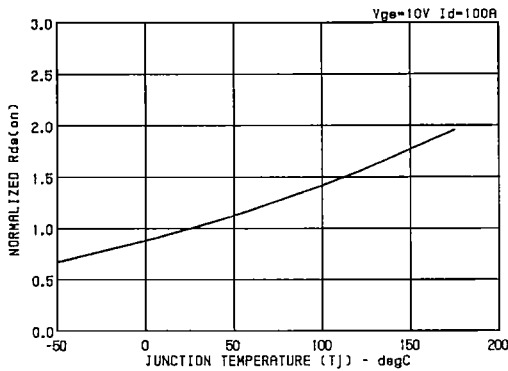


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

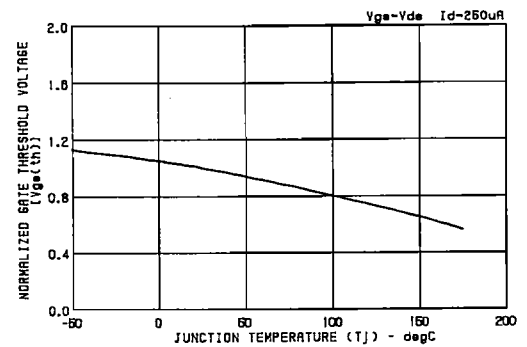


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

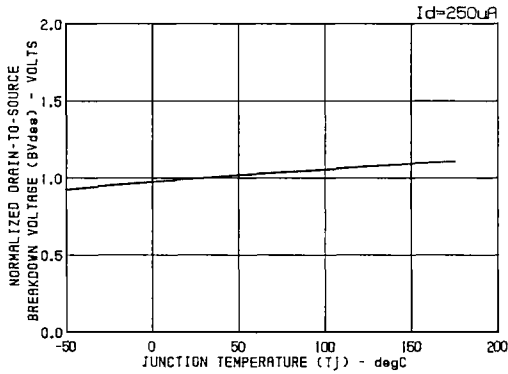


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

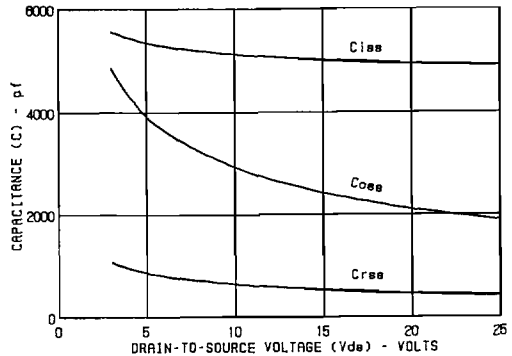


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

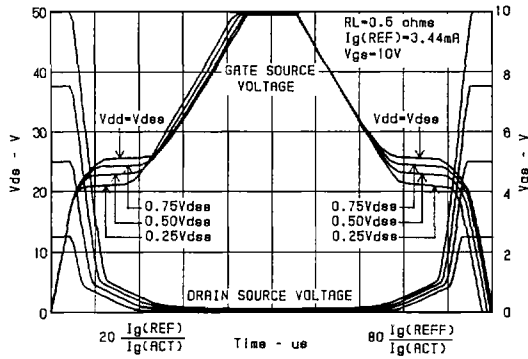


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

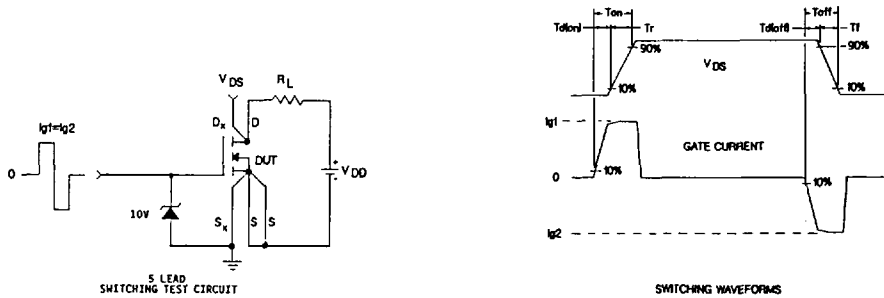
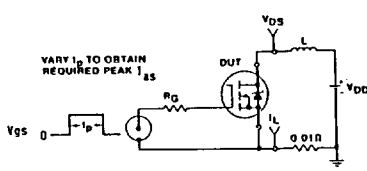


FIGURE 12. RESISTIVE SWITCHING

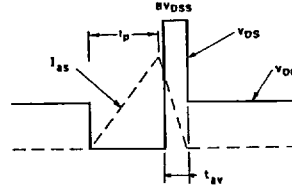
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Performance Curves (Continued)



UIS TEST CIRCUIT.

FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT



UIS WAVEFORMS.

FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

Spice Model

.SUBCKT RFA100N05 6 1 4 5 3 2 ; rev 10/30/90

*Nominal Temperature = 25°C

CchargeA 12 8 8.98e-9

CchargeB 15 14 8.8e-9

Cin 24 8 4.48e-009

Depletion_cap 10 21 DPLCAPMOD

Dbody 7 21 DBODYMOD

Dbreak 21 11 DBREAKMOD

Egs 14 8 21 8 1

Egs 13 8 24 8 1

Esg 24 10 24 8 1

Ebreak 11 7 17 18 58.4

Evto 20 24 18 8 1

Ipos 8 17 1

Ldkelvin 3 23 1e-9

Ldrain 6 21 2e-10

Lgate 1 9 5e-9

Lskelvin 2 7 5e-9

Lsource1 4 22 6e-9

Lsource2 5 25 6e-9

Mos 16 24 8 8 MOSMOD

Rbreak 17 18 RBREAKMOD 1

Rdrain 21 16 RSOURCEMOD 2.74e-3

Rgate 9 20 1.2

Rkdrain 23 21 0.33e-3

Rksource1 7 22 1.6e-3

Rksource2 7 25 1.6e-3

Rin 24 8 1e+9

Rsource 8 7 RSOURCEMOD 1.2e-3

Rvto 18 19 RVTONEGMOD 1

S1a 24 12 13 8 S1AMOD

S1b 13 12 13 8 S1BMOD

S2a 24 15 14 13 S2AMOD

S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.48 VOFF=-0.48)

.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.48 VOFF=-2.48)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.25 VOFF=2.75)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.75 VOFF=-2.25)

.MODEL DBODYMOD D (IS=2.23e-12 RS=2.5e-3 TRS1=2.5e-3 CJO=7.55e-9 TT=4e-8)

.MODEL DBREAKMOD D (RS=8e-2 TRS1=2.5e-3)

.MODEL DPLCAPMOD D (IS=1e-030 N=10 CJO=2.14e-9)

.MODEL RBREAKMOD RES (TC1=9.5e-4 TC2=-1.17e-6)

.MODEL RSOURCEMOD RES (TC1=5.2e-3 TC2=1.37e-5)

.MODEL RVTONEGMOD RES (TC1=-3.78e-3 TC2=-7.5e-7)

.MODEL MOSMOD NMOS (VTO=3.48 N=10 IS=1e-030 KP=78.5 TOX=1 L=1u W1u)

.ENDS

