

# 54FCT/74FCT273 Octal D Flip-Flop

## General Description

The 54FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{MR}$ ) input load and reset (clear) all flip-flops simultaneously.

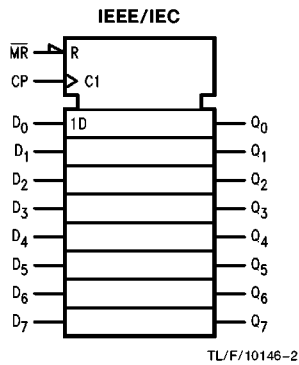
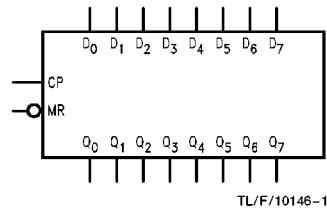
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## Features

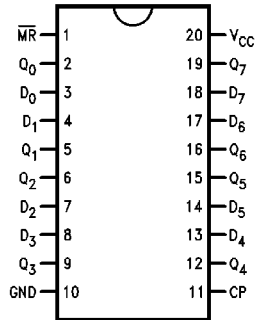
- $I_{CC}$  reduced to 40.0  $\mu A$
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- TTL input and output level compatible
- TTL levels accept CMOS levels
- $I_{OL} = 48$  mA (Com), 32 mA (Mil)
- NSC 54/74FCT273 is pin and functionally equivalent to IDT 54/74FCT273
- Military product compliant to MIL-STD-883 and Standard Military Drawing #5962-87656

## Logic Symbols



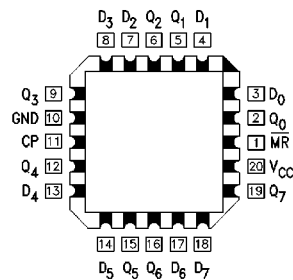
## Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

Pin Assignment for LCC

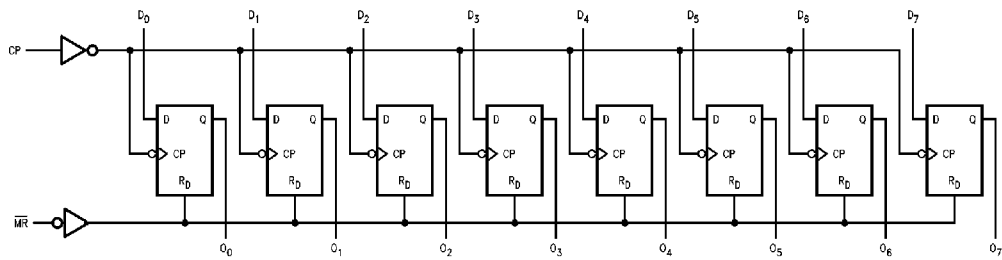


## Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	$D_n$	$Q_n$
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↗	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

## Logic Diagram



TL/F/10146-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND	
(V <sub>TERM</sub> )	
54FCT	-0.5 to +7.0V
74FCT	-0.5 to +7.0V
Temperature Under Bias (T <sub>BIAS</sub> )	
74FCT	-55°C to +125°C
54FCT	-65°C to +135°C
Storage Temperature (T <sub>STG</sub> )	
74FCT	-55°C to +125°C
54FCT	-65°C to +150°C
DC Output Current (I <sub>OUT</sub> )	
	120 mA

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage (V <sub>CC</sub> )	
54FCT	4.5V to 5.5V
74FCT	4.75 to 5.25V
Input Voltage	
	0V to V <sub>CC</sub>
Output Voltage	
	0V to V <sub>CC</sub>
Operating Temperature (T <sub>A</sub> )	
54FCT	-55°C to +125°C
74FCT	0°C to +70°C
Junction Temperature (T <sub>J</sub> )	
CDIP	175°C
PDIP	140°C

**Note:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

## DC Characteristics for 'FCT Family Devices

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V<sub>CC</sub> = 5.0V ± 5%, T<sub>A</sub> = 0°C to +70°C; Mil: V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = -55°C to +125°C, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Minimum High Level Input Voltage	2.0			V		
V <sub>IL</sub>	Maximum Low Level Input Voltage			0.8	V		
I <sub>IH</sub>	Input High Current			5.0 5.0	μA	V <sub>CC</sub> = Max	V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V (Note 2)
I <sub>IL</sub>	Input Low Current			-5.0 -5.0	μA	V <sub>CC</sub> = Max	V <sub>I</sub> = 0.5V (Note 2) V <sub>I</sub> = GND
V <sub>IK</sub>	Clamp Diode Voltage		-0.7	-1.2	V	V <sub>CC</sub> = Min; I <sub>N</sub> = -18 mA	
I <sub>OS</sub>	Short Circuit Current	-60	-120		mA	V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> = GND	
V <sub>OH</sub>	Minimum High Level Output Voltage	2.8	3.0		V	V <sub>CC</sub> = 3V; V <sub>IN</sub> = 0.2V or V <sub>HC</sub> ; I <sub>OL</sub> = -32 μA	
		V <sub>HC</sub>	V <sub>CC</sub>			V <sub>CC</sub> = Min	I <sub>OH</sub> = -300 μA
		2.4	4.3			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -12 mA (Mil) I <sub>OH</sub> = -15 mA (Com)
		2.4	4.3				

## DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at  $V_{CC} = 5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
$V_{OL}$	Maximum Low Level Output Voltage		GND	0.2	V	$V_{CC} = 3V$ ; $V_{IN} = 0.2V$ or $V_{HC}$ ; $I_{OL} = 300 \mu A$	
			GND	0.2		$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA (Mil)}$ $I_{OL} = 32 \text{ mA (Com)}$
			0.3	0.5			
$I_{CC}$	Maximum Quiescent Supply Current		1.0	40.0	$\mu A$	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}$ , $V_{IN} \leq 0.2V$ $f_I = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	
$I_{CCD}$	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $\overline{MR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
$V_H$	Input Hysteresis on Clock Only		200		mV		
$I_C$	Total Power Supply Current (Note 6)		1.5	4.0	mA	$V_{CC} = \text{Max}$ Outputs Open $\overline{MR} = V_{CC}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		$f_I = 10 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
			3.0	7.8		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $\overline{MR} = V_{CC}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8		$f_I = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
$V_H$	Input Hysteresis on Clock Only		200		mV		

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_I$  = Input Frequency

$N_I$  = Number of Inputs at  $f_I$

All currents are in milliamps and all frequencies are in megahertz.

## AC Electrical Characteristics

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_A, V_{CC} = \text{Com}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Mil}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$		
		Typ	Min	Max	Min	Max	
$t_{PHL}$ $t_{PLH}$	Propagation Delay Clock to Output	7.0	2.0	13.0	1.5	9.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{MR}$ to Output	8.0	2.0	13.0	1.5	10.5	ns
$t_{SU}$	Setup Time HIGH or LOW Data to CP	1.5	3.0		3.5		ns
$t_h$	Hold Time HIGH or LOW Data to CP	1.0	2.0		2.0		ns
$t_w$	Clock Pulse Width HIGH or LOW	4.0	7.0		5.0		ns
$t_w$	$\overline{MR}$ Pulse Width HIGH or LOW	4.0	7.0		5.0		ns
$t_{rec}$	Recovery Time $\overline{MR}$ to CP	3.0	4.0		4.0		ns
$f_{max}$	Maximum Clock Frequency				90		MHz

**Note 1:** Minimum limits are guaranteed but not tested on Propagation Delays.

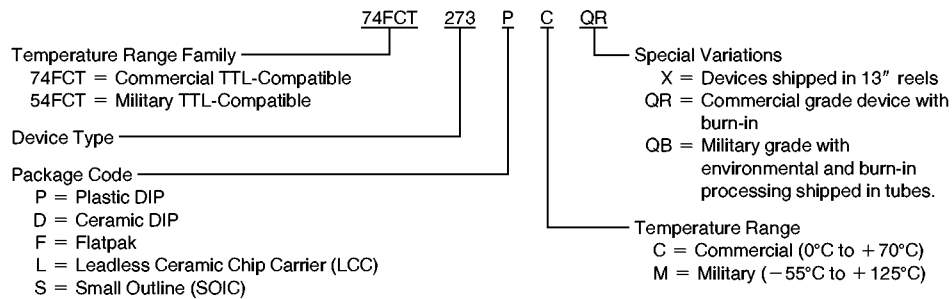
## Capacitance $T_A = 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$

Symbol	Parameter	Conditions	Typ	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

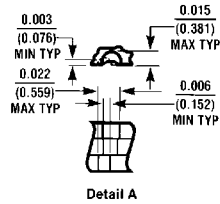
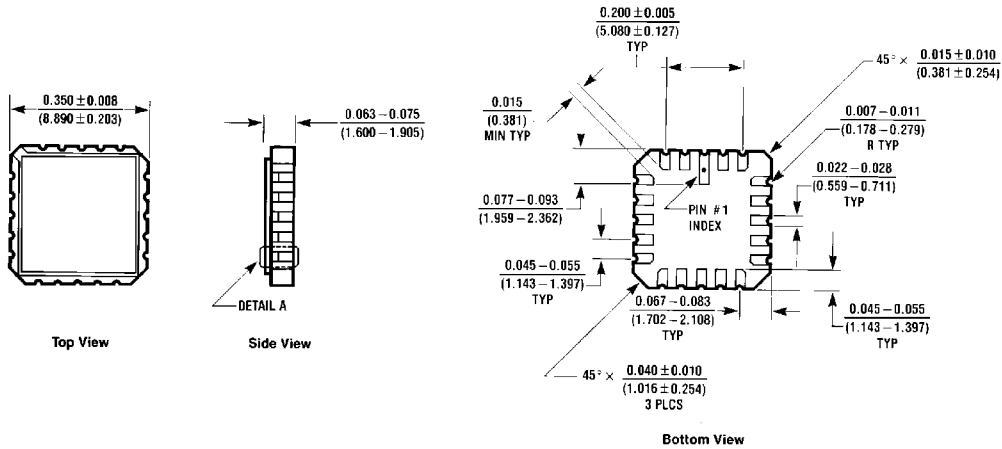
**Note:** This parameter is guaranteed by characterization data and not tested.

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

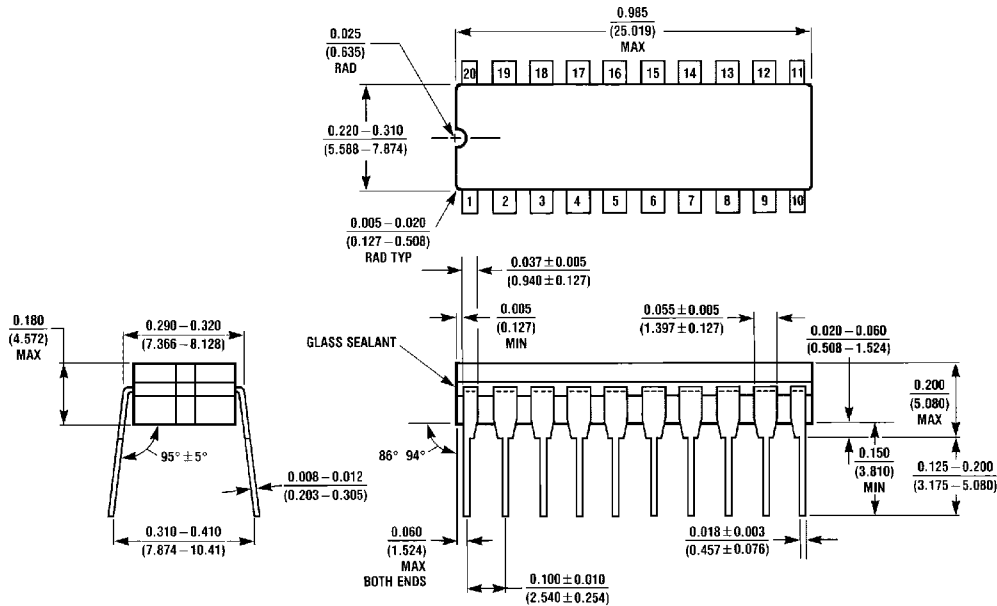


**Physical Dimensions** inches (millimeters)



**20-Terminal Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

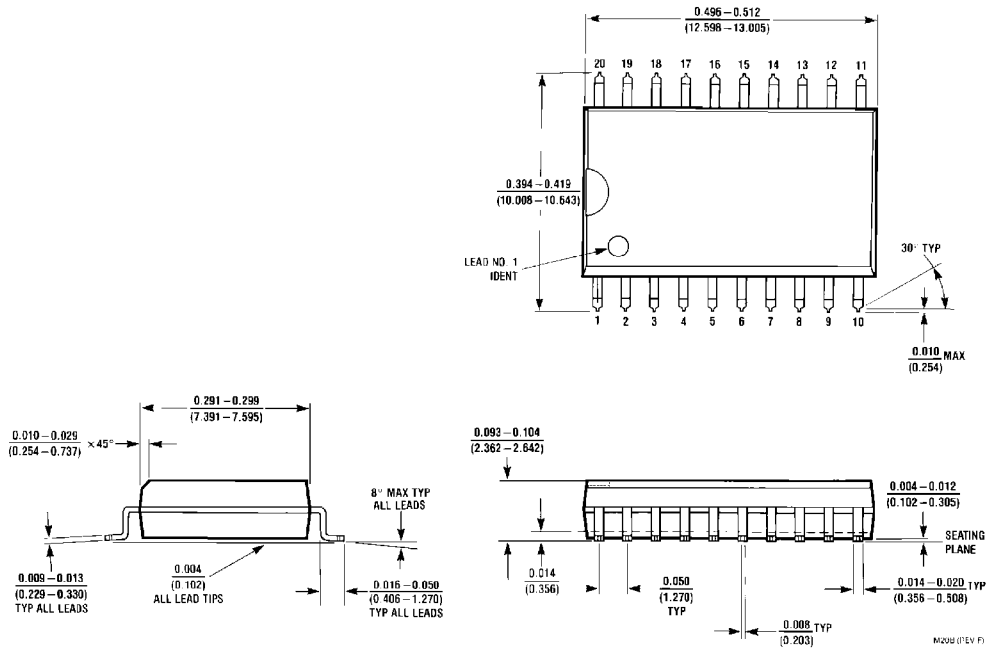
E20A (REV D)



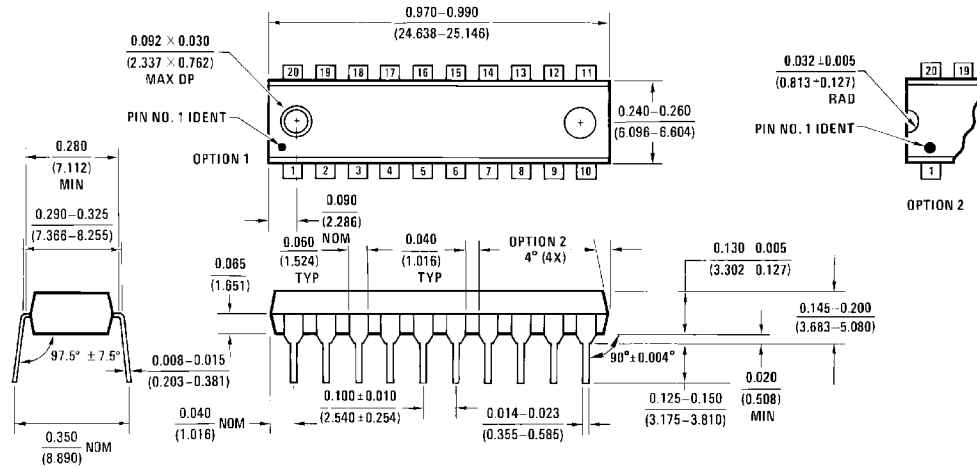
**20-Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)



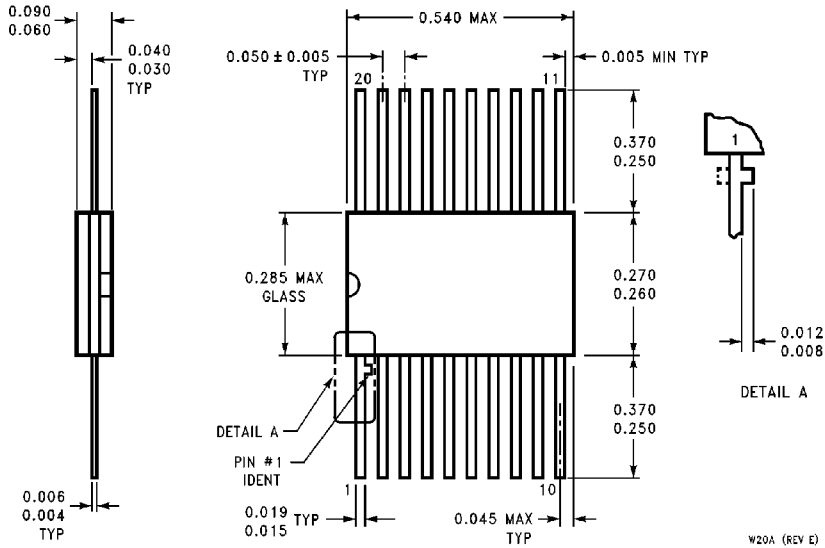
**20-Lead Small Outline Integrated Circuit (S)  
NS Package Number M20B**



**20-Lead Plastic Dual-In-Line Package (P)  
NS Package Number N20B**

**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 114706



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

W20A (REV E)

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
1111 West Bardin Road  
Arlington, TX 76017  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018

**National Semiconductor Europe**  
Fax: (+49) 0-180-530 85 86  
Email: onjwge@tevm2.nsc.com  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Français Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.