

# SN74LS195A

## Universal 4-Bit Shift Register

The SN74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL products.

- Typical Shift Right Frequency of 39 MHz
- Asynchronous Master Reset
- J,  $\bar{K}$  Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

### GUARANTEED OPERATING RANGES

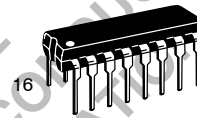
Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current - High			-0.4	mA
I <sub>OL</sub>	Output Current - Low			8.0	mA



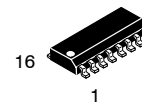
ON Semiconductor™

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LOW  
POWER  
SCHOTTKY



PLASTIC  
N SUFFIX  
CASE 648



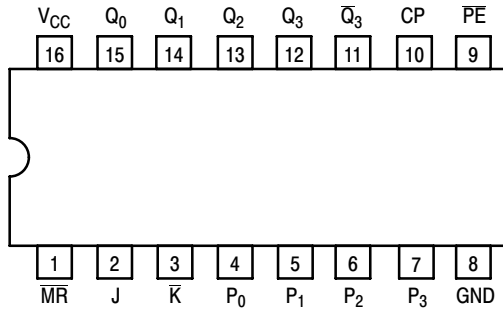
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS195AN	16 Pin DIP	2000 Units/Box
SN74LS195AD	SOIC-16	38 Units/Rail
SN74LS195ADR2	SOIC-16	2500/Tape & Reel

# SN74LS195A

## CONNECTION DIAGRAM DIP (TOP VIEW)



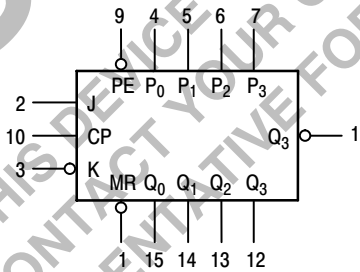
NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
PE	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
P <sub>0</sub> - P <sub>3</sub>	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
K	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> - Q <sub>3</sub>	Parallel Outputs	10 U.L.	5 U.L.
Q <sub>3</sub>	Complementary Last Stage Output	10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

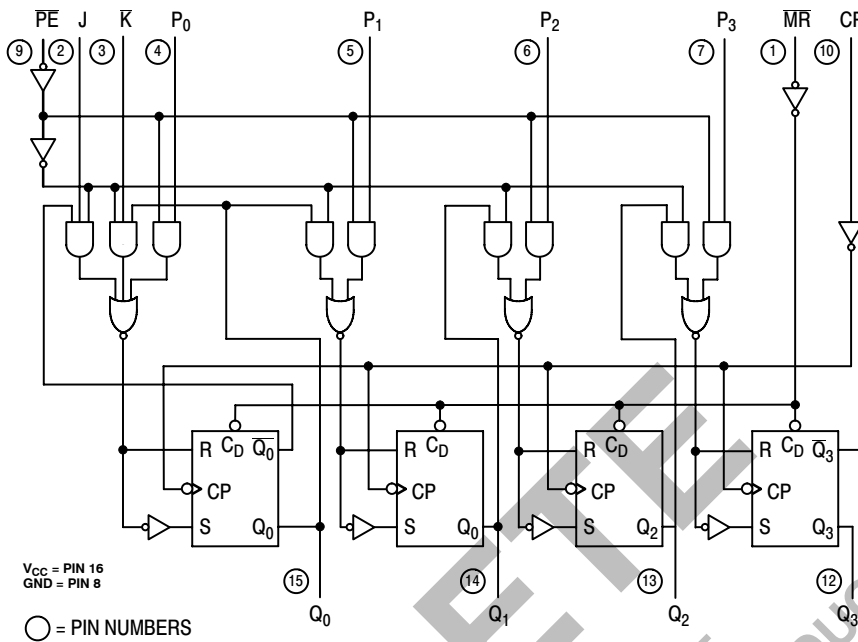
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN74LS195A

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load which are controlled by the state of the Parallel Enable ( $\overline{PE}$ ) input. When the PE input is HIGH, serial data enters the first flip-flop  $Q_0$  via the J and  $\overline{K}$  inputs and is shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$  following each LOW to HIGH clock transition. The  $\overline{JK}$  inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two pins together. When the  $\overline{PE}$

input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs  $P_0, P_1, P_2, P_3$  is transferred to the respective  $Q_0, Q_1, Q_2, Q_3$  outputs following the LOW to HIGH clock transition. Shift left operations ( $Q_3 \rightarrow Q_2$ ) can be achieved by tying the  $Q_n$  Outputs to the  $P_{n-1}$  inputs and holding the  $\overline{PE}$  input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J,  $\overline{K}$ ,  $P_n$  and  $\overline{PE}$  inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ( $\overline{MR}$ ) input sets all Q outputs LOW, independent of any other input condition.

## MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	MR	PE	J	K	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Reset First	H	h	l	l	X	L	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Toggle First Stage	H	h	h	l	X	$\overline{q}_0$	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Shift, Retain First Stage	H	h	l	h	X	$q_0$	$q_0$	$q_1$	$q_2$	$\overline{q}_2$
Parallel Load	H	l	X	X	$p_n$	$p_0$	$p_1$	$p_2$	$p_3$	$\overline{p}_3$

L = LOW voltage levels

H = HIGH voltage levels

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.

$p_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

# SN74LS195A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA I <sub>OL</sub> = 8.0 mA
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			21	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	39		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		14 17	22 26	ns	
t <sub>PHL</sub>	Propagation Delay, MR to Output		19	30	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP Clock Pulse Width	16			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	MR Pulse Width	12			ns	
t <sub>s</sub>	PE Setup Time	25			ns	
t <sub>s</sub>	Data Setup Time	15			ns	
t <sub>rec</sub>	Recovery Time	25			ns	
t <sub>rel</sub>	PE Release Time			10	ns	
t <sub>h</sub>	Data Hold Time	0			ns	

**DEFINITIONS OF TERMS**

SETUP TIME( $t_s$ ) —is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

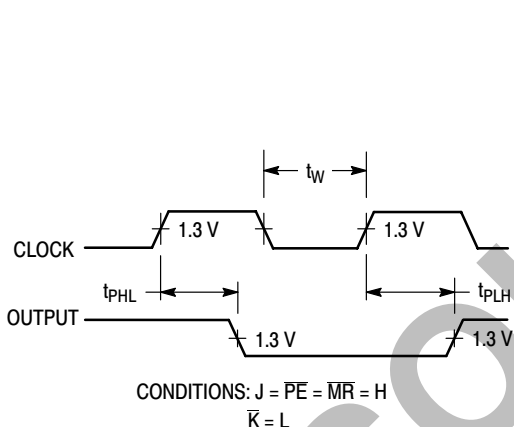
HOLD TIME ( $t_h$ ) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

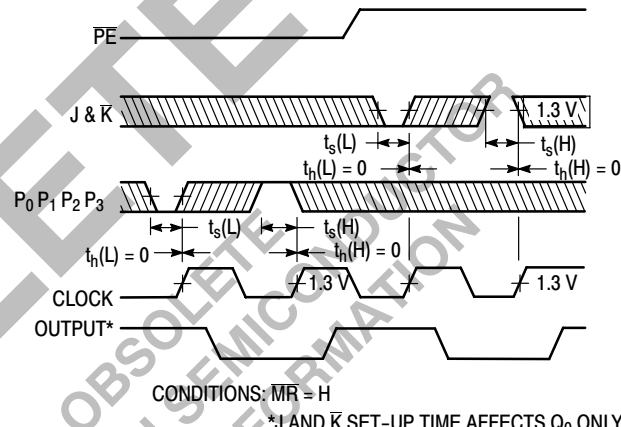
RECOVERY TIME ( $t_{rec}$ ) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

**AC WAVEFORMS**

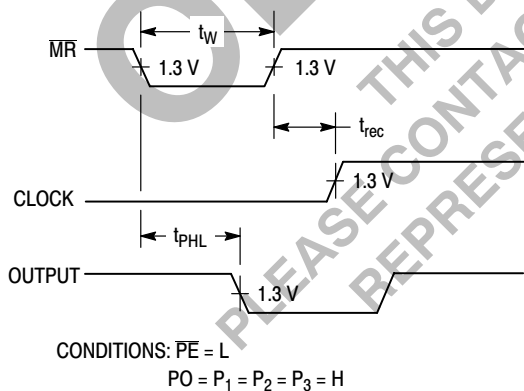
The shaded areas indicate when the input is permitted to change for predictable output performance.



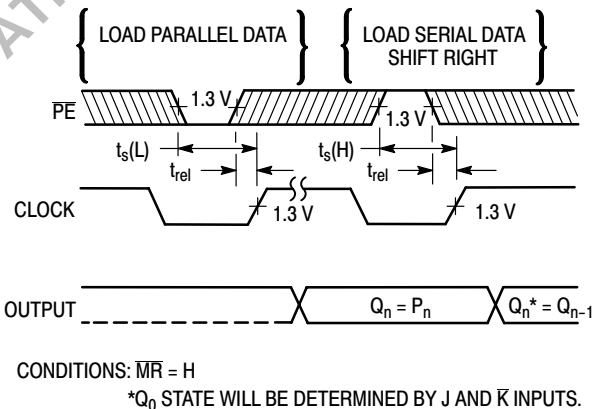
**Figure 1. Clock to Output Delays and Clock Pulse Width**



**Figure 3. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for Serial Data (J & K) and Parallel Data ( $P_0, P_1, P_2, P_3$ )**



**Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time**

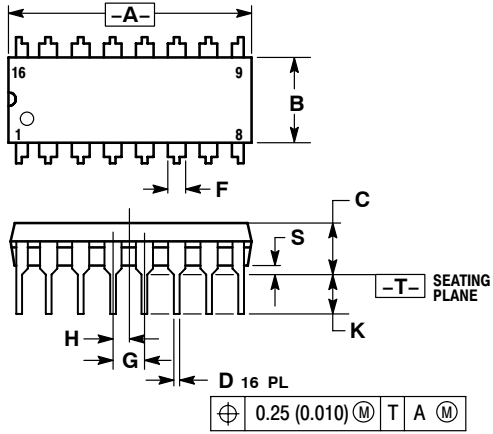


**Figure 4. Setup ( $t_s$ ) and Hold ( $t_h$ ) Time for  $\overline{PE}$  Input**

# SN74LS195A

## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

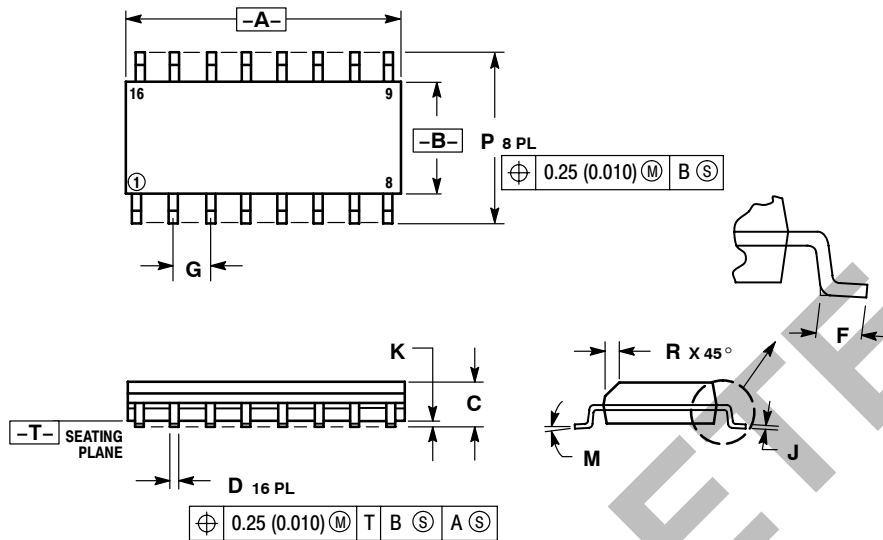
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

OBSOLETE

THIS DEVICE IS OBSOLETE  
 PLEASE CONTACT YOUR ON SEMICONDUCTOR  
 REPRESENTATIVE FOR INFORMATION

# SN74LS195A

## D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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