I_{OUT} = 1 A Linear Regulator ICs

SI-3000KD Series

Data Sheet

Description

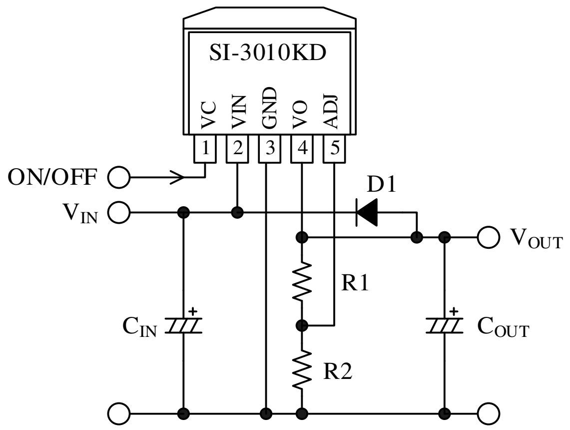
The SI-3000KD series are linear regulator ICs whose maximum output current is 1 A. The output voltage of the SI-3010KD is adjusted by external resistors. The output voltage of the SI-3033KD is 3.3 V fixed.

The ICs have a built-in low saturation PNP bipolar transistor and can operate with a low input/output voltage difference. The ICs have various functions including the Output On/Off Function, the Overcurrent Protection and the Thermal Shutdown, and achieve a linear regulator circuit with few external components.

Features

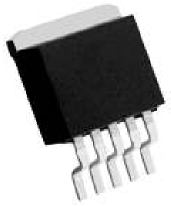
- Low Dropout Voltage, $\Delta V_{DIF} \leq 0.6$ V (I_{OUT} = 1 A)
- Output On/Off Function
- Protections
  Overcurrent Protection (OCP): Fold-back (SI-3010KD), Drooping (SI-3033KD), Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application (SI-3010KD)



Packages

TO263-5L



Not to scale

Selection Guide

Part Number	Output Voltage
SI-3010KD	Adjustable
SI-3033KD	3.3 V

Applications

- Audio Visual Equipment
- Office Automation Equipment
- White Goods

Contents

1. Absolute Maximum Ratings

Unless otherwise specified, $T_A = 25$ °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
VIN Pin Voltage	V_{IN}		35[1]	V	SI-3010KD
			17	V	SI-3033KD
VC Pin Voltage	V_C		V_{IN}	V	
Output Current	I_{OUT}		1	A	
Power Dissipation	P_D	Mounted on the board [2]	3	W	
Junction Temperature	T_J		−30 to 125	°C	
Operating Ambient Temperature [2]	T_{OP}		−30 to 85	°C	
Storage Temperature	T_{STG}		−30 to 125	°C	

2. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance between Junction and Ambient	θ_{J-A}	Mounted on the board [2]	—	—	33.3	°C/W
Thermal Resistance between Junction and Case[3]	θ_{J-C}		—	—	3	°C/W

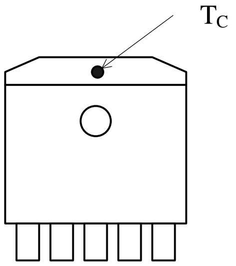


Figure 2-1. Case Temperature Measurement Point

[1] Limited by overvoltage protection voltage of 33 V.
[2] Glass-epoxy board (40 mm × 40 mm), copper area 100%
[3] The case temperature (°C) is measured at the point defined in Figure 2-1.

3. Recommended Operating Range

Parameter	Symbol	Min.	Max.	Unit	Remarks
VIN Pin Voltage	V_{IN}	2.4[1]	27[2]	V	SI-3010KD
		[1]	6[2]	V	SI-3033KD
Output Current	I_{OUT}	0	1[2]	A	
Output Voltage	V_{OUT}	1.1	16	V	SI-3010KD
Operating Ambient Temperature	$T_{OP(A)}$	−30	85	°C	
Operating Junction Temperature	$T_{OP(J)}$	−20	100	°C	

[1] Should be set to V_{OUT} + dropout voltage or higher. See Section 4 for dropout voltage.

[2] The following equation shows the relationship between V_{IN}, V_{OUT}, and I_{OUT}. Thus, Dropout Voltage ($V_{IN} - V_{OUT}$) and/or I_{OUT} may be limited in some conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

4. Electrical Characteristics

4.1. SI-3010KD

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C, V_{OUT} = 5 V, R2 = 10 kΩ.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Reference Voltage	V_{REF}	V_{IN} = 7 V, I_{OUT} = 10 mA	0.98	1.00	1.02	V
Line Regulation	ΔV_{LINE}	V_{IN} = 6 V to 15 V, I_{OUT} = 10 mA	—	—	30	mV
Load Regulation	ΔV_{LOAD}	V_{IN} = 7 V, I_{OUT} = 0 A to 1 A	—	—	75	mV
Dropout Voltage	ΔV_{DIF}	I_{OUT} = 0.5 A	—	—	0.3	V
		I_{OUT} = 1 A	—	—	0.6	V
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T_A$	T_J = 0 °C to 100 °C	—	±0.5	—	mV/°C
Ripple Rejection Ratio	R_{REJ}	V_{IN} = 7 V, f = 100 Hz to 120 Hz I_{OUT} = 0.1 A	—	55	—	dB
Overcurrent Protection Operating Current [(1)]	I_{S1}	V_{IN} = 7 V	1.1	—	—	A
Quiescent Current	I_Q	V_{IN} = 7 V, I_{OUT} = 0 A, V_C = 2 V	—	—	600	µA
Circuit Current during Regulator Output Off	$I_{Q(OFF)}$	V_{IN} = 7 V, V_C = 0 V	—	—	1	µA
VC Pin Voltage (Output On)	V_{C_IH}		2	—	—	V
VC Pin Voltage (Output Off)	V_{C_IL}		—	—	0.8	V
VC Pin Current (Output On)	I_{C_IH}	V_C = 2.0 V	—	—	40	µA
VC Pin Current (Output Off)	I_{C_IL}	V_C = 0 V	−5	0	—	µA
Overvoltage Protection Voltage	V_{OVP}	I_{OUT} = 10 mA	33	—	—	V

(1) After the Overcurrent Protection is activated, I_{S1} is measured when the output voltage, V_{OUT}, (conditions: V_{IN} = 7 V, I_{OUT} = 10 mA) decreases by 5%.

4.2. SI-3033KD

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, $T_A = 25$ °C.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Setting Output Voltage	V_{OUT}	V_{IN} = 5 V, I_{OUT} = 10 mA	3.234	3.300	3.366	V
Line Regulation	ΔV_{LINE}	V_{IN} = 5 V to 10 V, I_{OUT} = 10 mA	—	—	15	mV
Load Regulation	ΔV_{LOAD}	V_{IN} = 5 V, I_{OUT} = 0 A to 1 A	—	—	50	mV
Dropout Voltage	ΔV_{DIF}	I_{OUT} = 0.5 A	—	—	0.4	V
		I_{OUT} = 1 A	—	—	0.6	V
Output Voltage Temperature Coefficient	$\Delta V_{OUT}/\Delta T_A$	T_J = 0 °C to 100 °C	—	±0.3	—	mV/°C
Ripple Rejection Ratio	R_{REJ}	V_{IN} = 5 V, f = 100 Hz to 120 Hz	—	55	—	dB
Overcurrent Protection Operating Current [(1)]	I_{S1}	V_{IN} = 5 V	1.1	—	—	A
Quiescent Current	I_Q	V_{IN} = 5 V, I_{OUT} = 0 A, V_C = 2 V	—	—	350	µA
Circuit Current during Regulator Output Off	$I_{Q(OFF)}$	V_{IN} = 5 V, V_C = 0 V	—	—	1	µA
VC Pin Voltage (Output On)	V_{C_IH}		2	—	—	V
VC Pin Voltage (Output Off)	V_{C_IL}		—	—	0.8	V
VC Pin Current (Output On)	I_{C_IH}	V_C = 2.0 V	—	—	40	µA
VC Pin Current (Output Off)	I_{C_IL}	V_C = 0 V	−5	0	—	µA

(1) After the Overcurrent Protection is activated, I_{S1} is measured when the output voltage, V_{OUT}, (conditions: V_{IN} = 5 V, I_{OUT} = 10 mA) decreases by 5%.

5. Performance Curves

5.1. SI-3010KD

Unless otherwise specified, T_A = 25 °C, V_{OUT} = 5 V, R2 = 10 kΩ.

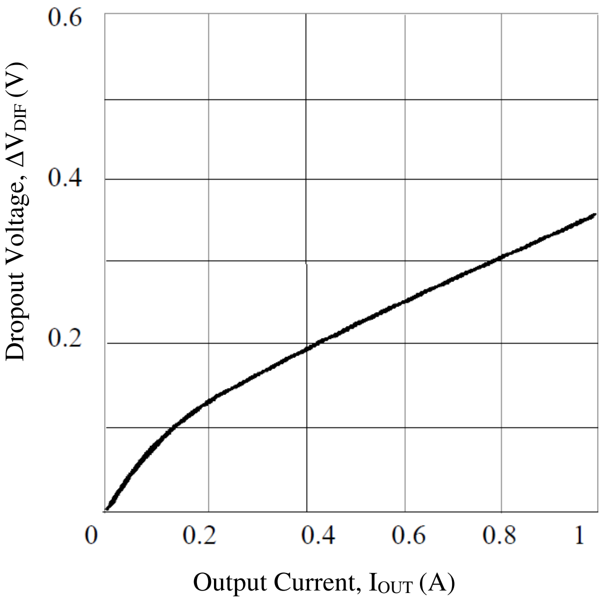


Figure 5-1. Dropout Voltage

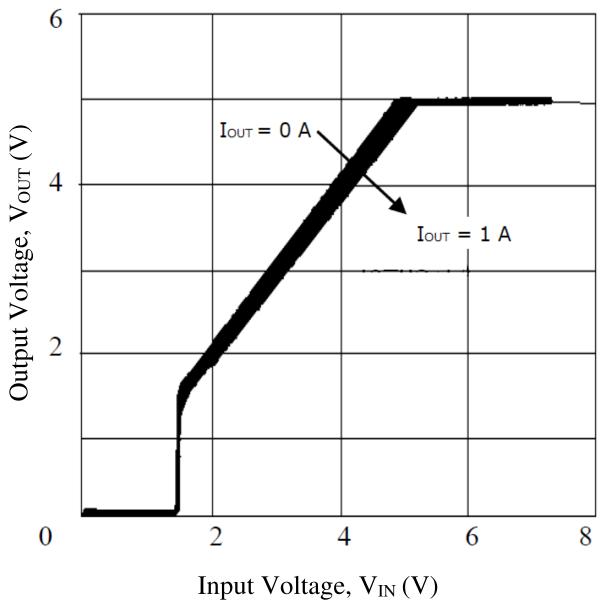


Figure 5-2. Output Rise Characteristics

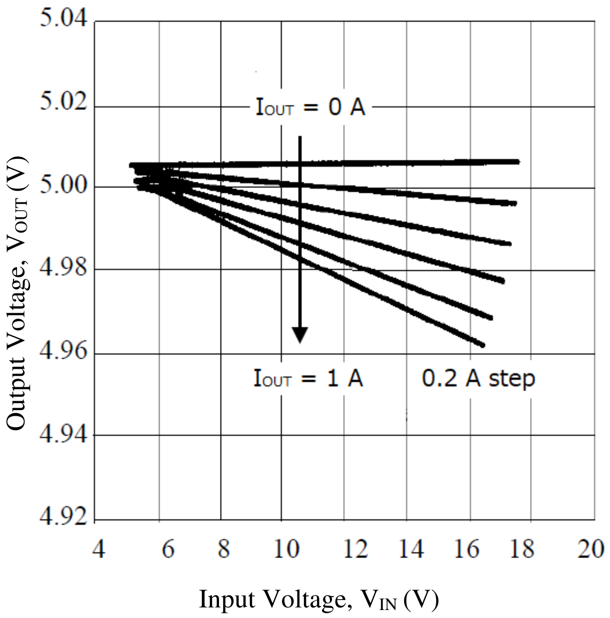


Figure 5-3. Line Regulation

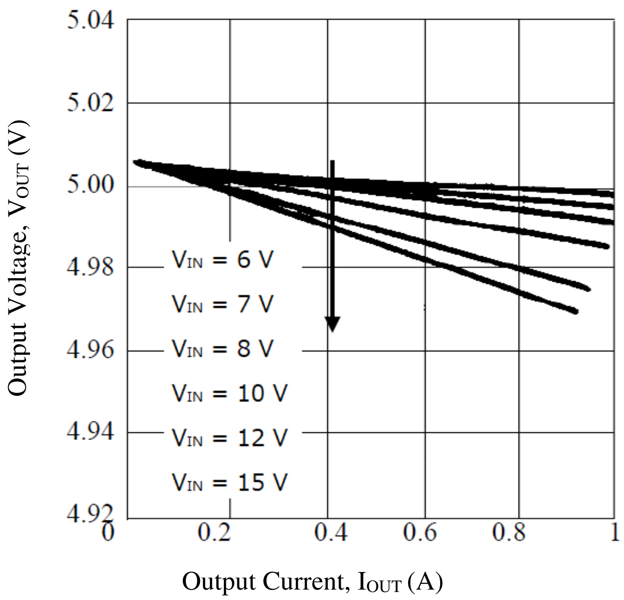


Figure 5-4. Load Regulation

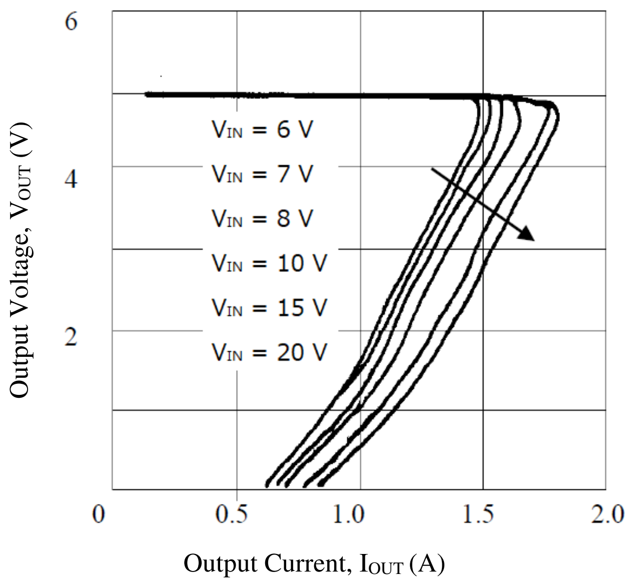


Figure 5-5. Overcurrent Protection Characteristics

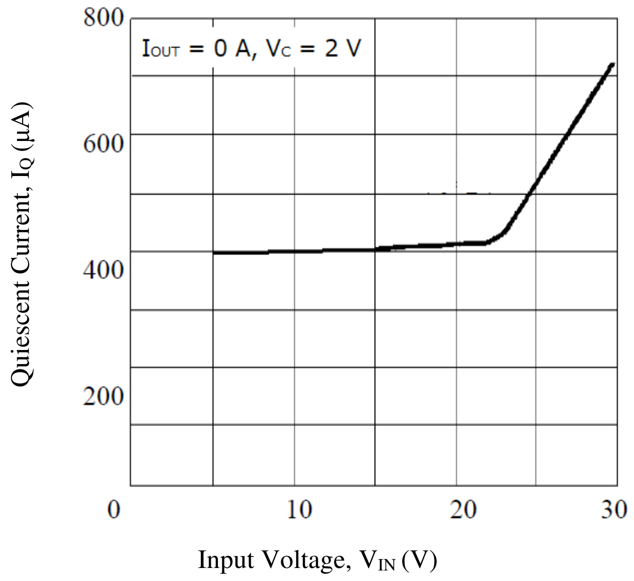


Figure 5-6. $I_Q - V_{IN}$

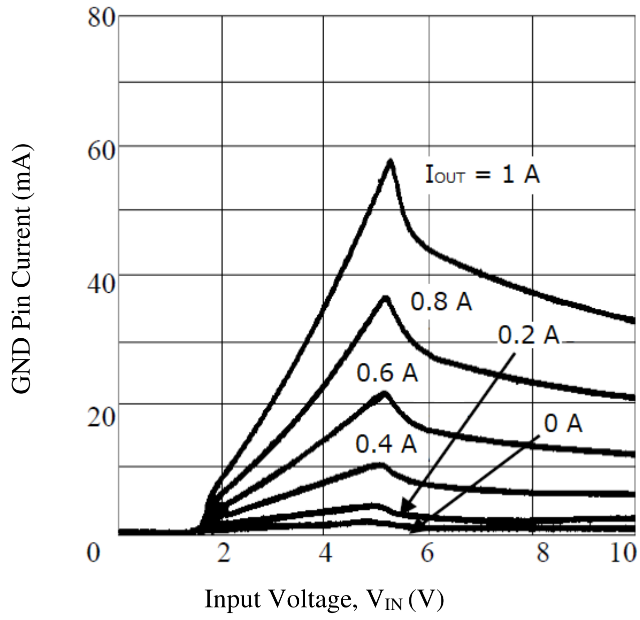


Figure 5-7. GND Pin Current

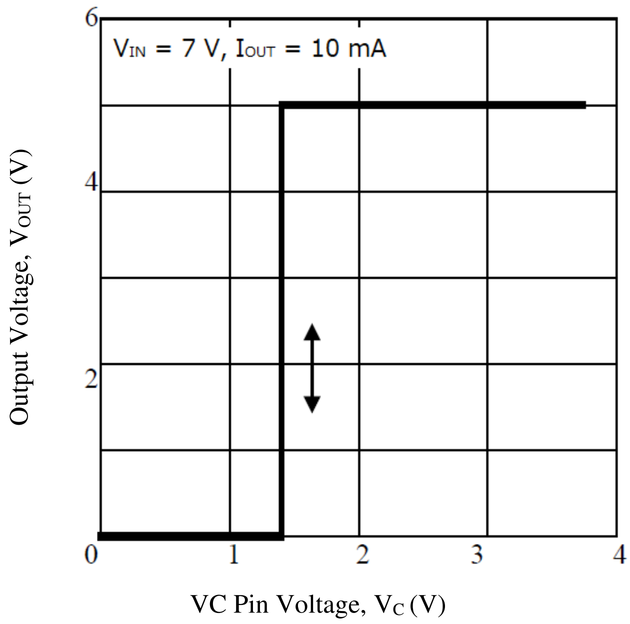


Figure 5-8. $V_{OUT} - V_C$

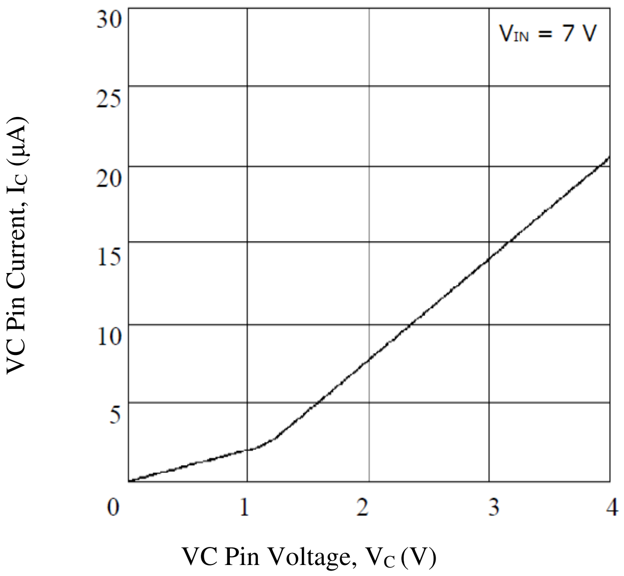


Figure 5-9. I_C – V_C

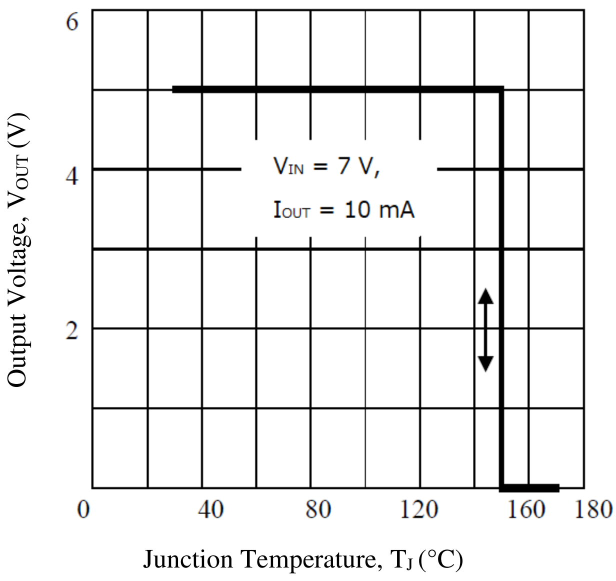


Figure 5-10. Thermal Shutdown Characteristics

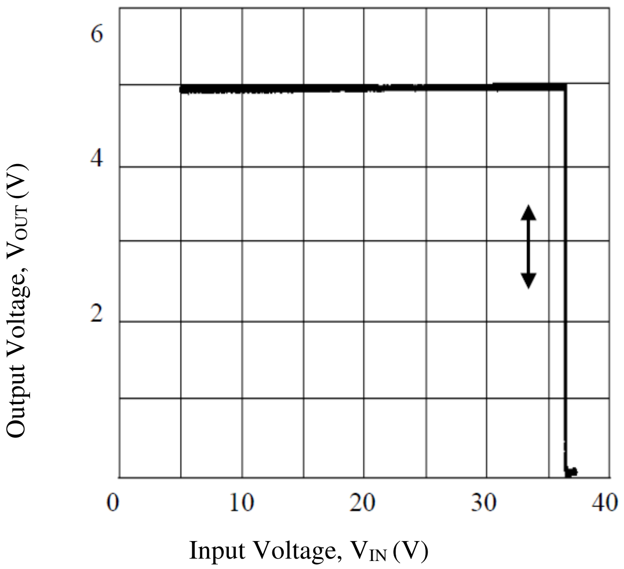


Figure 5-11 Overvoltage Protection Characteristics

5.2. SI-3033KD

Unless otherwise specified, $T_A = 25$ °C.

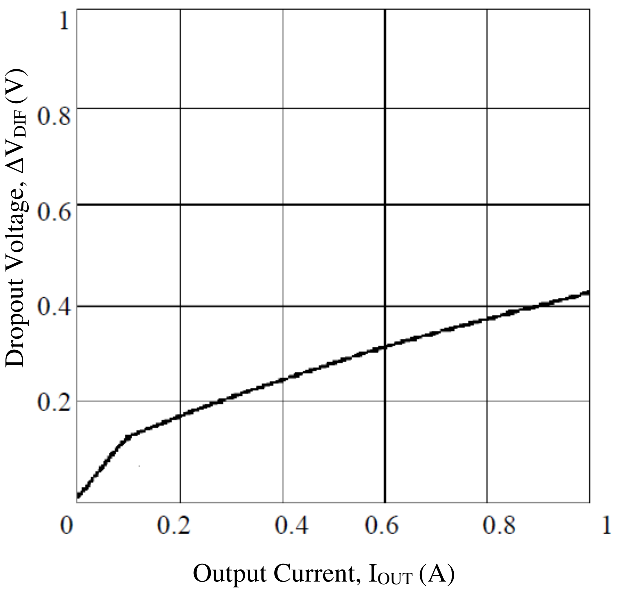


Figure 5-12. Dropout Voltage

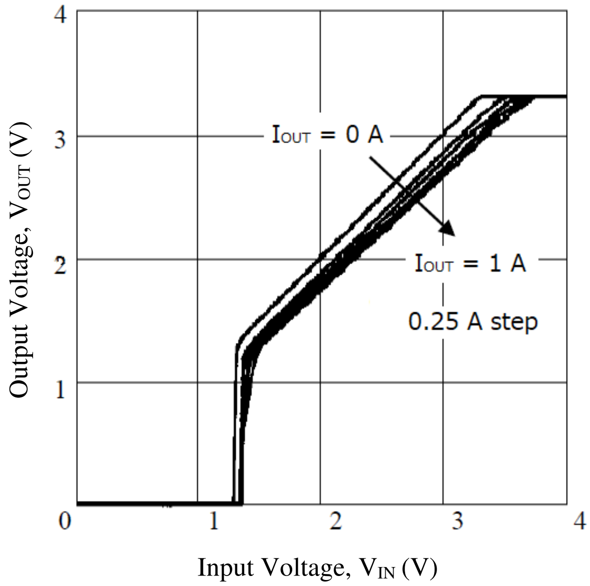


Figure 5-13. Output Rise Characteristics

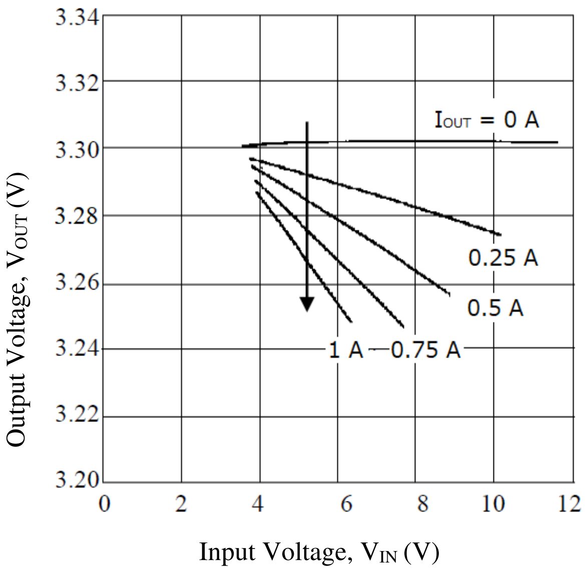


Figure 5-14. Line Regulation

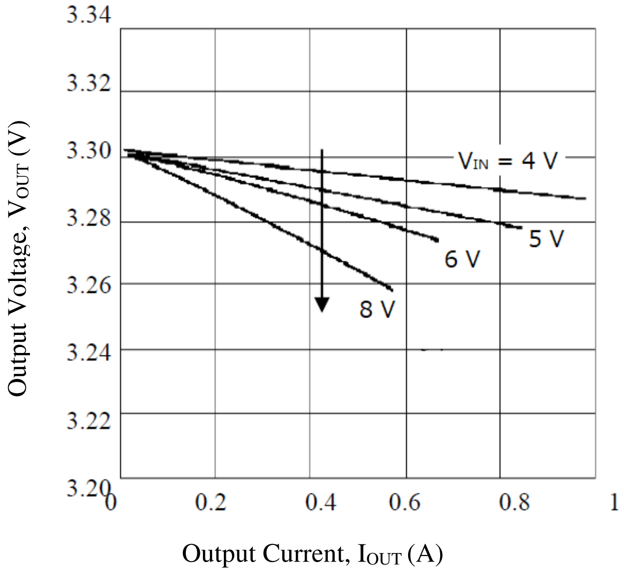


Figure 5-15. Load Regulation

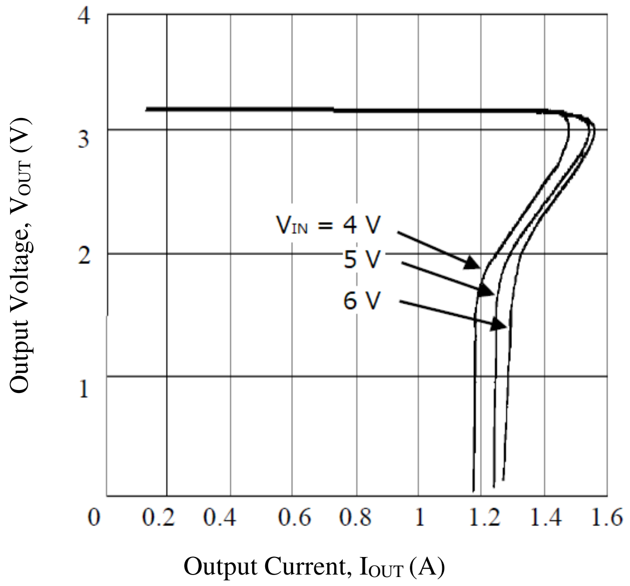


Figure 5-16. Overcurrent Protection Characteristics

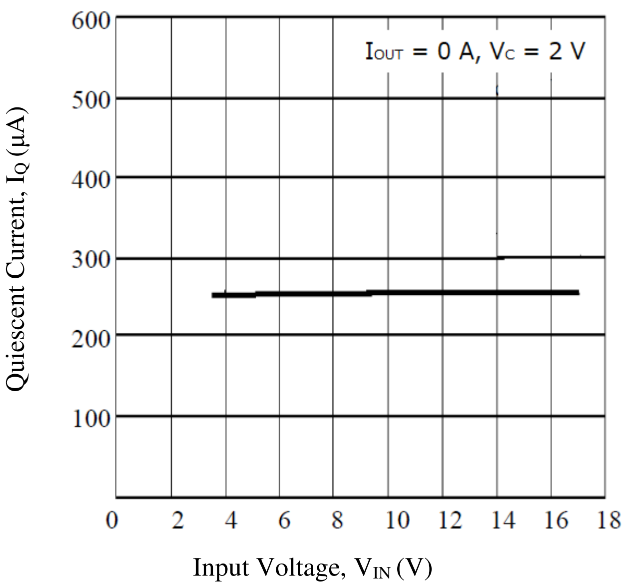


Figure 5-17. I_Q – V_{IN}

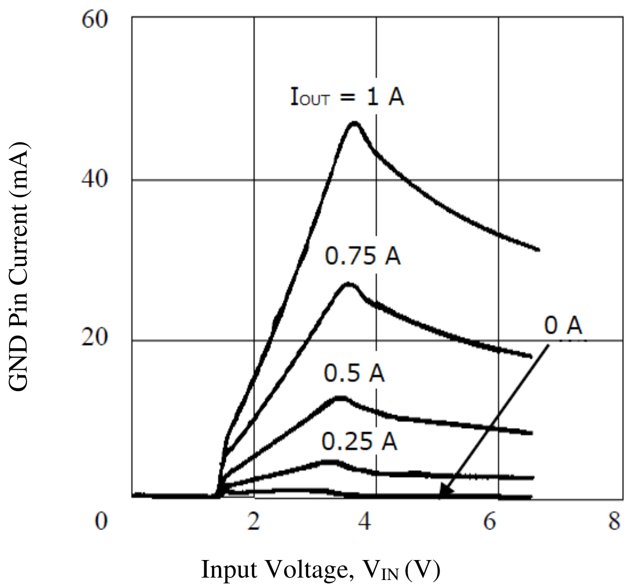


Figure 5-18. GND Pin Current

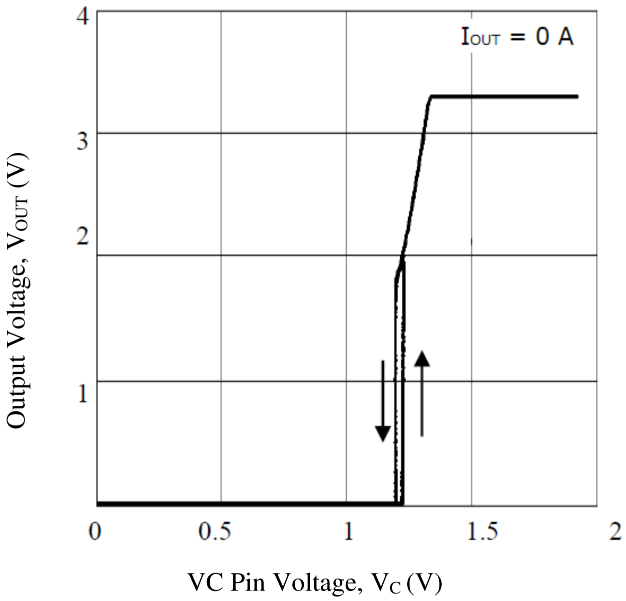


Figure 5-19. V_{OUT} – V_C

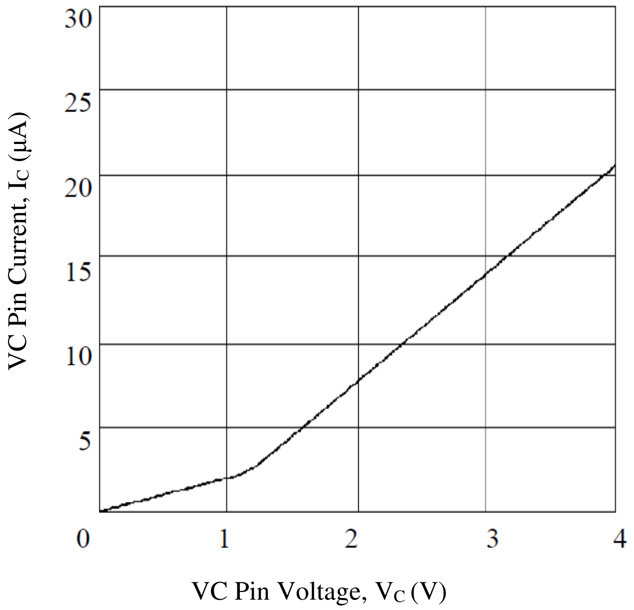


Figure 5-20. $I_C – V_C$

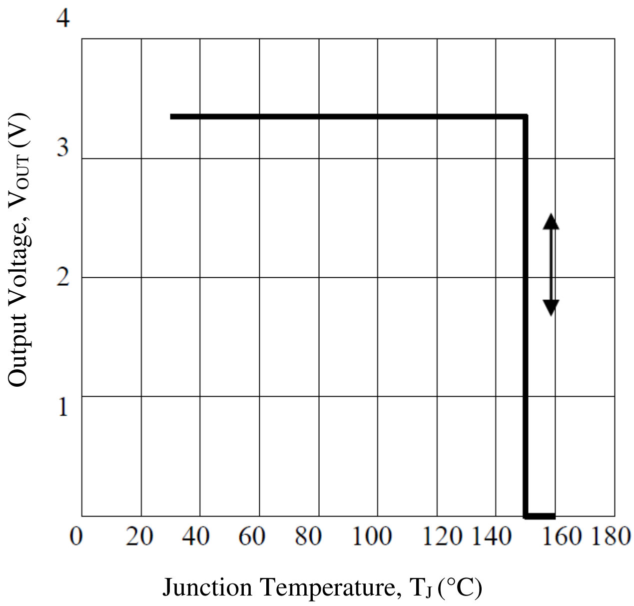


Figure 5-21. Thermal Shutdown Characteristics

6. Derating Curve

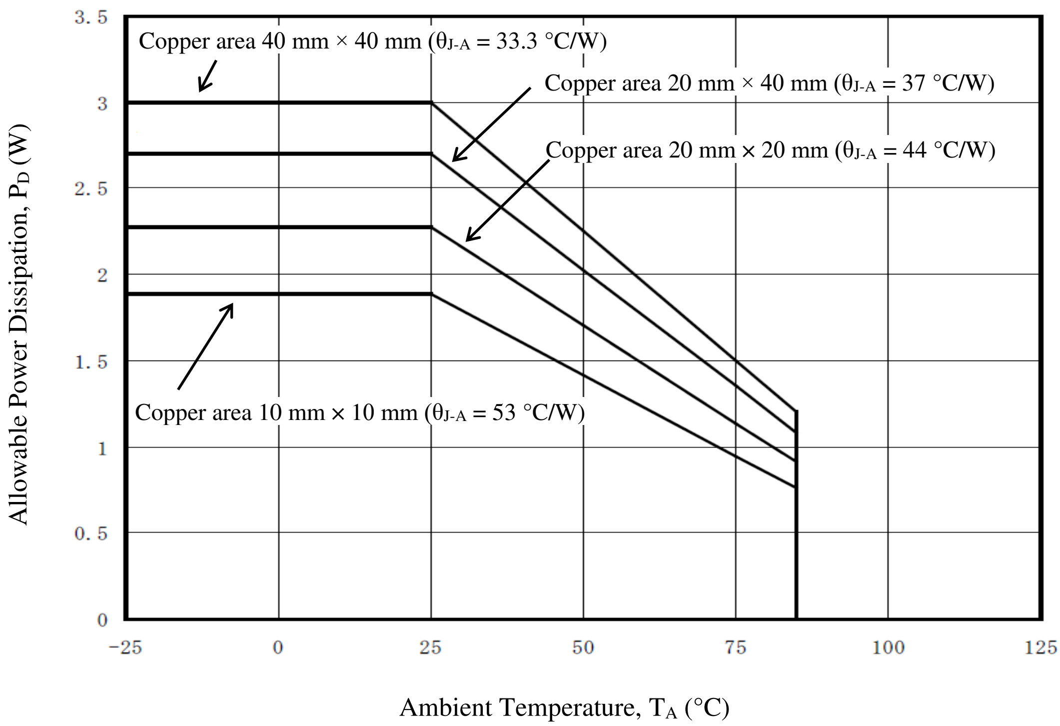


Figure 6-1. Power Dissipation, P_D vs. Ambient Temperature, T_A

7. Block Diagram

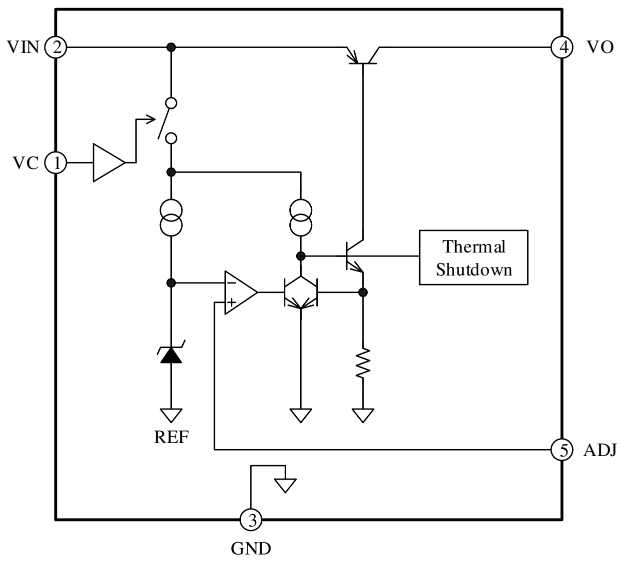


Figure 7-1. SI-3010KD: Block Diagram

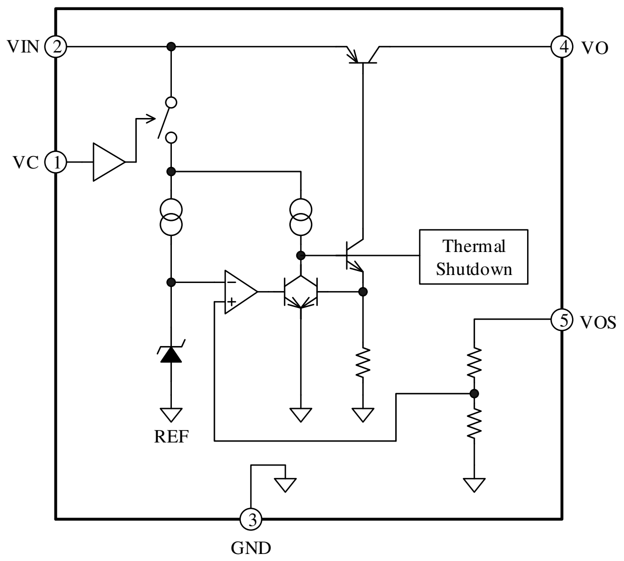
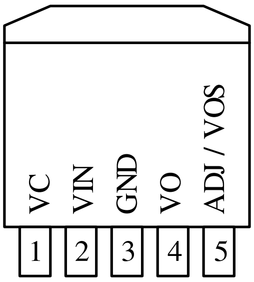


Figure 7-2. SI-3033KD: Block Diagram

8. Pin Configuration Definitions



Pin Number	Pin Name	Function	Remarks
1	VC	On/off signal input	
2	VIN	Voltage input	
3	GND	Ground	
4	VO	Voltage output	
5	ADJ	Output voltage setting resistor connection	SI-3010KD
	VOS	Feedback	SI-3033KD
(Back Side)	—	Heatsink (A heatsink is internally connected to the GND pin. In order to improve heat dissipation, be sure to solder the heatsink of the IC to copper trace on PCB. The copper area should be as wide as possible.)	

9. Typical Application

9.1. SI-3010KD

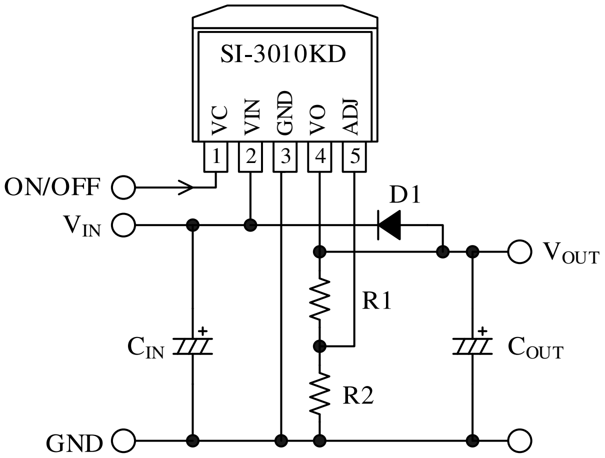


Figure 9-1. Typical Application (V_{OUT} > 1.5 V)

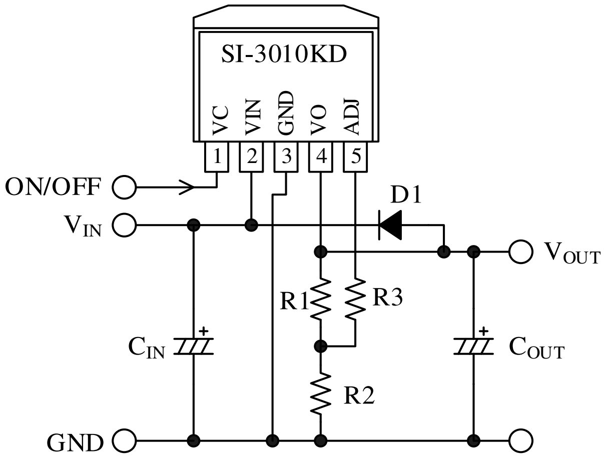


Figure 9-2. Typical Application (V_{OUT} ≤ 1.5 V)

Table 9-1 Reference Value of External Components

Symbol	Part Type	Reference Value	Remarks
C_{IN}	Electrolytic capacitor/ ceramic capacitor	0.47 µF to 22 µF	C_{IN} is required when the input line contains inductance, or the wiring is long. C_{IN} should be connected as close as possible to the VIN and GND pins with a minimal length of traces.
C_{OUT}	Electrolytic capacitor	≥ 47 µF	Ceramic capacitors cannot be used.
R1	Resistor	—	Adjust resistance according to the output voltage. See Section 12.2.
R2	Resistor	10 kΩ	See Section 12.2.
R3	Resistor	10 kΩ	Add R3 when V_{OUT} ≤ 1.5 V.
D1	Diode	—	Add D1 when V_{OUT} > 3.3 V. Select a diode that has sufficient Surge Forward Current tolerance against the discharge current of C_{OUT}. See Section 13.2.

9.2. SI-3033KD

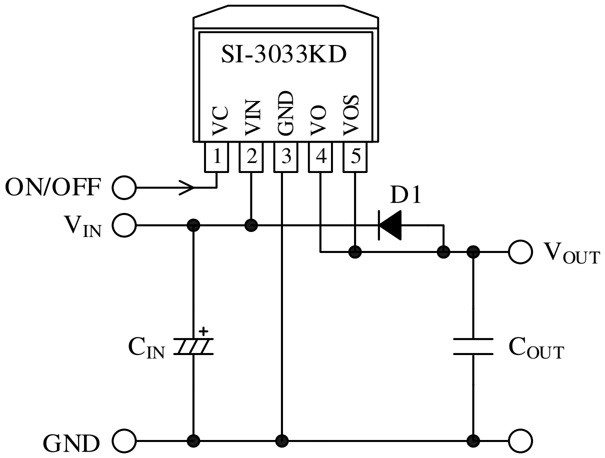


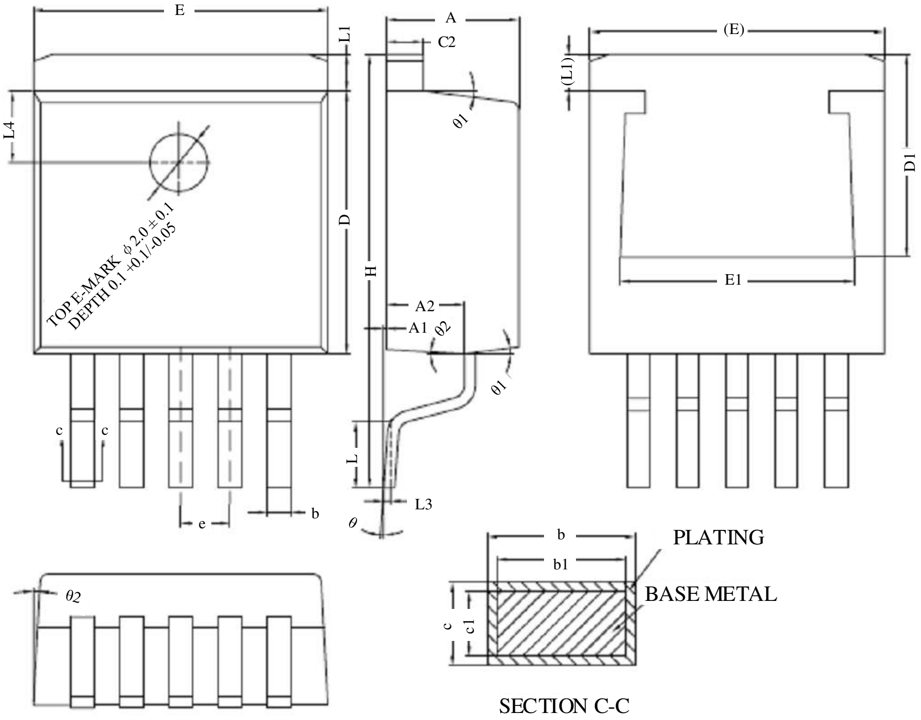
Figure 9-3. Typical Application

Table 9-2 Reference Value of External Components

Symbol	Part Type	Reference Value	Remarks
C_{IN}	Electrolytic capacitor/ ceramic capacitor	0.47 µF to 22 µF	C_{IN} is required when the input line contains inductance, or the wiring is long. C_{IN} should be connected as close as possible to the VIN and GND pins with a minimal length of traces.
C_{OUT}	Ceramic capacitor	≥ 22 µF	Electrolytic capacitors cannot be used.
D1	Diode	—	Select a diode that has sufficient Surge Forward Current tolerance against the discharge current of C_{OUT}. See Section 13.2.

10. Physical Dimensions

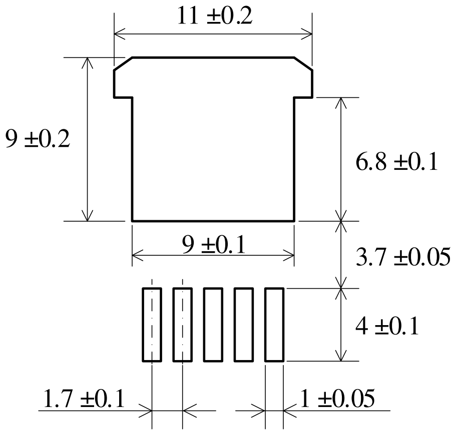
- **TO263-5L**



Symbol	Min.	Nom.	Max.
A	4.40	4.57	4.70
A1	0	0.10	0.25
A2	2.59	2.69	2.79
b	0.77	—	0.90
b1	0.76	0.81	0.86
c	0.34	—	0.47
c1	0.33	0.38	0.43
C2	1.22	—	1.32
D	9.05	9.15	9.25
D1	6.86	—	7.50
E	10.06	10.16	10.26
E1	7.50	—	8.30
e		1.70 BSC	
H	14.70	15.10	15.50
L	2.00	2.30	2.60
L1	1.17	1.27	1.40
L3	0.25 BSC		
L4	2.00 REF		
θ	0°	—	8°
θ1	5°	7°	9°
θ2	1°	3°	5°

NOTES:
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Dimensions do not include mold burrs.

10.1. Land Pattern Example



Dimensions in millimeters.

11. Marking Diagram

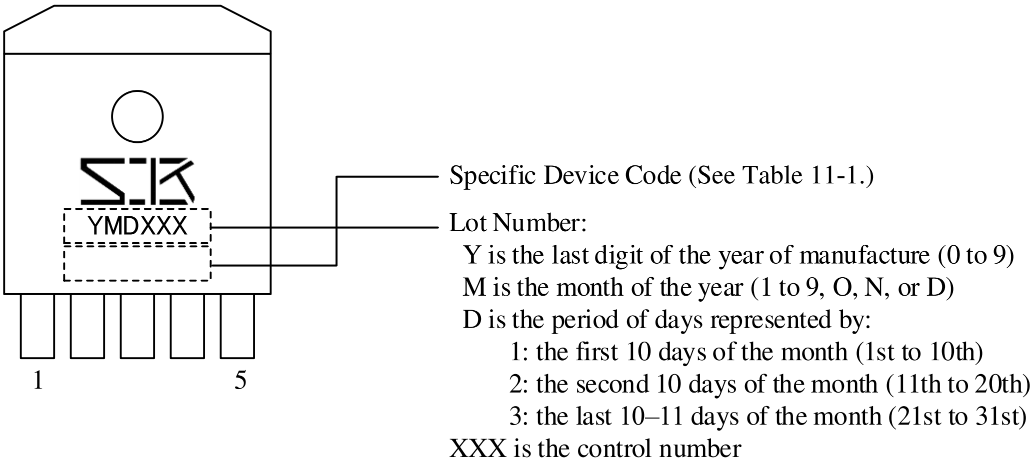


Table 11-1 Specific Device Code

Specific Device Code	Part Number
3010KD	SI-3010KD
3033KD	SI-3033KD

12. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. See Figure 9-1, Figure 9-2 and Figure 9-3 for symbols used in the description.

12.1. Constant Voltage Control

The IC consists of some circuit such as a reference voltage, an error amplifier, and a PNP transistor.

The SI-3010KD compares the ADJ pin voltage with the reference voltage by the error amplifier (see Figure 7-1). The SI-3033KD compares the output voltage, V_{OUT} divided by the detection resistors and the reference voltage by the error amplifier (see Figure 7-2). To regulate the output voltage, the emitter-to-collector voltage of the PNP transistor is linear controlled so that the compared voltages are the same.

The thermal design must be taken into account, because the product of the emitter-collector voltage (Dropout Voltage) and the output current result in the loss of the IC.

12.2. Output Voltage Setting (Only SI-3010KD)

The output voltage is adjusted by external resistors, R1 and R2 (see Figure 9-1 and Figure 9-2). The ADJ pin is for feedback signal input to set the output voltage. Do not apply any voltage other than this feedback signal to the ADJ pin.

The feedback current flowing through R1 and R2 is set to about 100 µA. The reference voltage of the ADJ pin, V_{REF}, is 1.00 V. R2 is calculated by Equation (1).

$$R2 = \frac{V_{REF}}{100\ (\mu A)} = \frac{1.10\ (V)}{100\ (\mu A)} = 11\ (k\Omega) \tag{1}$$

The output voltage, V_{OUT}, is calculated by Equation (2).

$$V_{OUT} = \frac{R1 + R2}{R2} \times V_{REF} \tag{2}$$

Thus, R1 is calculated by using Equation (3).

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

$$= \frac{10\ k\Omega \times (V_{OUT} - 1.10\ V)}{1.10\ V} \tag{3}$$

If the calculation result does not match the value defined by the E series, adjustment resistors should be added in series or parallel to R1.

When setting the output voltage to ≤ 1.5 V, add R3 as shown in Figure 9-2. R3 is about 10 kΩ.

12.3. Overcurrent Protection Function (OCP)

● **SI-3010KD**

The IC has Overcurrent Protection (OCP) with the fold-back characteristic that the output current at the short circuit load (V_{OUT} = 0 V) is smaller than that at OCP activation (see Figure 5-5). In the short circuit load, the loss ($V_{IN} \times I_{OUT}$) of a fold-back system is less than the loss of the constant current or fold-forward system.

When the voltage across the output capacitor is 0 V at IC startup, the IC gradually increases the output voltage while limiting the output current with OCP.

● **SI-3033KD**

The IC has the Overcurrent Protection (OCP) with the drooping characteristic as shown in Figure 5-16. Note that the drooping type keeps a large output current flowing even after the OCP operates and the output voltage is short-circuited.

12.4. Thermal Shutdown (TSD)

The IC has the Thermal Shutdown (TSD). When the junction temperature of the IC increases to 130 °C or more, TSD is activated, and turns off the internal PNP transistor to shutdown the load current.

The TSD does not have temperature hysteresis. When the junction temperature falls below 130 °C, the IC automatically returns to normal operation.

The TSD protects the IC against the heat generation when the loss of the IC increases due to the instantaneous short-circuit of the load. This does not guarantee the operation including the reliability in the short-circuit state for long period or the state where the heat generation continues.

12.5. Output On/Off Function

The output is turned on/off by the input signal to the VC pin. When the VC pin voltage, V_C, is 2 V or more, the output is supplied. When V_C is 0.8 V or less, the output is turned off. When the VC pin is open, the output is turned off.

Since the VC pin input is equivalent to the low power Schottky TTL circuit (LS-TTL), the VC pin can be driven directly by LS-TTL.

Note that the voltage applied to the VC pin should not exceed the maximum rating.

13. Design Notes

13.1. Considerations in Circuit Configuration (Only SI-3010KD)

The overcurrent protection of the SI-3010KD has the fold-back characteristic. To avoid startup failure, do not use the circuit configurations as follows:

- Constant current circuit is connected to the IC.
- CV/CC circuit is connected to the IC.
- Load 2 is stacked on Load 1 (see in Figure 13-1).
- The output voltage setting resistor is connected between the GND pin and Ground (see Figure 13-2).

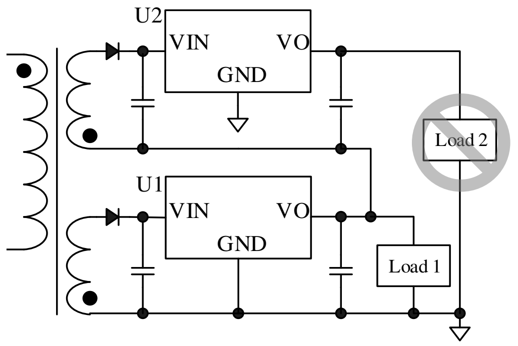


Figure 13-1 Stacked on Loads
(Do not connect Load 2.)

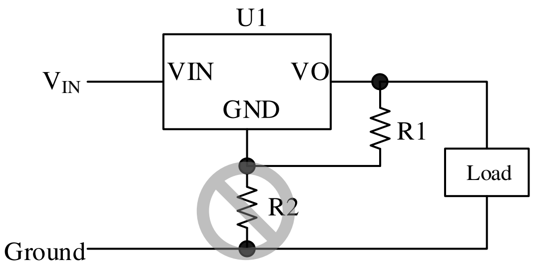


Figure 13-2 Output Voltage Setting
(Do not connect R2.)

13.2. External Components

- **Input Capacitor, C_{IN}**

The capacitor, C_{IN}, connected to the VIN pin is a bypass capacitor for suppressing noise and stabilizing voltage. Use electrolytic or ceramic capacitor for C_{IN}. The capacitance is about 0.47 µF to 22 µF.

- **Output Capacitor, C_{OUT}**

The output capacitor, C_{OUT}, is connected to the VO pin.

SI-3010KD

C_{OUT} is a capacitor for phase compensation and is an electrolytic capacitor of ≥ 47 µF. Select an electrolytic capacitor with a series equivalent resistance (ESR) in the range of 0.2 Ω to 2 Ω.

If a low ESR type capacitor such as a ceramic capacitor is used for the output capacitor, the output voltage may oscillate.

SI-3033KD

C_{OUT} is a capacitor for phase compensation and is a ceramic capacitor of ≥ 22 µF. Select a ceramic capacitor with a series equivalent resistance (ESR) of > 0.2 Ω.

If a high ESR type capacitor such as an electrolytic capacitor is used for the output capacitor, the output voltage may oscillate.

- **Protection Diode for Reverse Biasing**

If the output voltage is 3.3 V or higher, connect the diode, D1, for reverse bias protection. The IC is protected when a reverse bias is applied between input and output such as when the input voltage is turned off. D1 is not required if the output voltage is less than 3.3V.

13.3. PCB Pattern Layout

- **Input/ output Capacitor, C_{IN}, C_{OUT}**

Place C_{IN} and C_{OUT} as close as possible to the IC with a minimum length of traces to the VIN and VO pins.

- **Output Voltage Setting Resistor, R1, R2 (Only SI-3010KD)**

R1 and R2 should be placed as close as possible to the IC. R2 should be connected to the ADJ and GND pins with a minimum length of traces.

- **Ground**

Ground traces should be as wide and short as possible so that EMI levels can be reduced.

13.4. Thermal Design

Generally, the heat dissipation of an IC depends on the size and material of the board and the copper area. To improve the thermal performance, the copper area of the part where the backside of the IC is soldered should be as large as possible.

Figure13-3 shows the derating of the IC. When using the IC, ensure a sufficient margin.

Follow the procedure below to design heat dissipation.

(1) Measure the maximum ambient temperature, $T_{A(MAX)}$ of the IC.

(2) Change the input/output conditions and check the power dissipation, P_D. Calculate the maximum power dissipation, $P_{D(MAX)}$ with the Equation (4).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

(3) Determine the copper area by confirming the intersection of ambient temperature and power dissipation by the thermal derating characteristics shown in Figure13-3.

For reference, Figure13-3 shows the relationship between the copper area and thermal resistance of a single-sided copper foil board, FR-4.

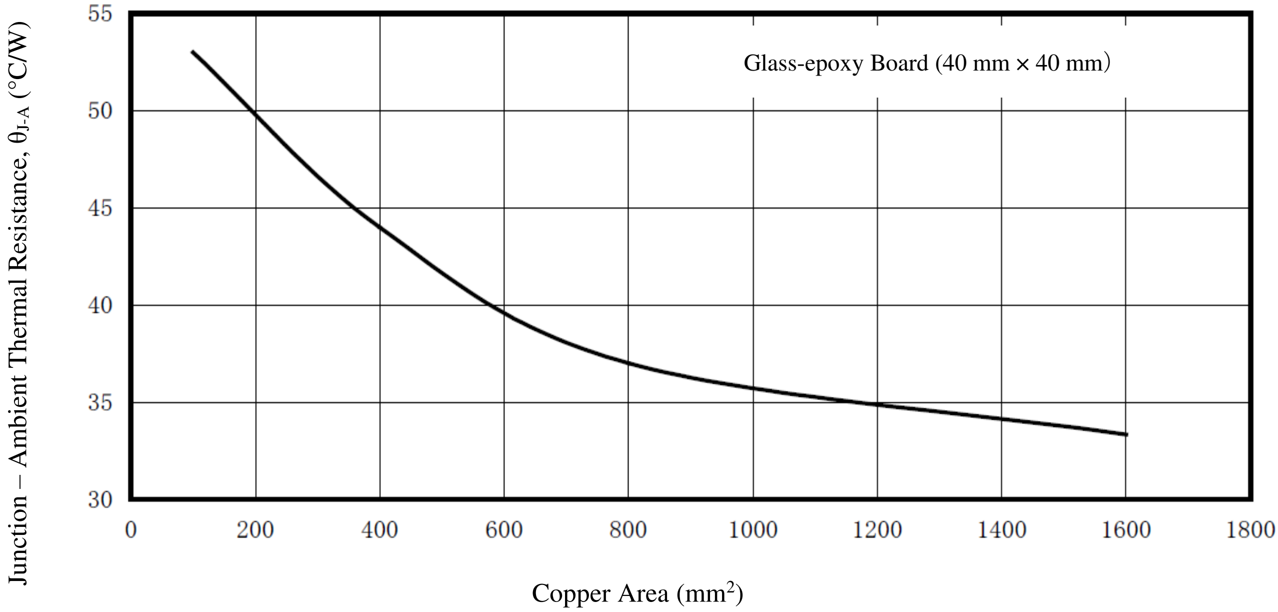


Figure13-3 Thermal Resistance – Copper Area Reference Characteristics (Single-sided Copper Foil Board, FR-4)

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