3 to 5cells lithium-ion / lithium-polimar secondary battery protection IC

MM3474 Series

Description

MM3474 series is an overcharge, overdischarge and overcurrent protection IC for a lithium-ion / lithium-polymer secondary battery. This supports 3 to 5 serial cells, and the number of cells can be switched over by inputting high / low signal to SEL terminal. MM3474 series can protect Lithium ion battery pack of 6-plus serial cells by connecting in cascade. This also provides the control terminals of output overdischarge detection (SDC) and output overcharge detection (SOC), which allows configuring an application with fewer external parts for 6 or more cells connected in series.

We provide many kinds of optional ICs of MM3474 series, which are customizable for the usage by selecting optional functions.

Low cost and small size configuration can be achieved when MM3474 series is combined with MM3220V series which is 2 cells protection IC and used for the applications of 6 cells or 7 cells, etc.

Cell balance control function can be added when MM3513 series which is cell balance control IC is used.

Features

(Unless otherwise specified, Ta=25 degC)

・Detection voltage	Range	Accuracy
Overcharge detection voltage	3.6V to 4.5V, 5mV steps	+/-25mV(Ta=0 to +50 degC)
Overdischarge detection voltage	2.0V to 3.0V, 50mV steps	+/-80mV
Overcurrent detection voltage	50mV to 300mV, 5mV steps	+/-15mV
Short detection voltage	0.2V to 1.0mV, 50mV steps	+/-100mV

・3-, 4-, 5-cell protection switching function

The 3-, 4-, or 5-cell protection can be switched by connecting the SEL1 pin and SEL2 pin to the VDD or VSS2 via a protection resistor. At the time of 4-cell protection, the operation of the overcharge detection circuit and overdischarge detection circuit for the V1 cell is stopped. Therefore, short-circuit the V1 pin and VSS1 pin before use. At the time of 3-cell protection, the operation of overcharge detection circuit and overdischarge detection circuit for V1 and V2 Cell is stopped. Therefore, short-circuit the V2 pin, V1 pin and VSS1 pin before use.

SEL1 pin	SEL2 pin	MM3474 Setting
High (VDD)	High (VDD)	5 cell prptection
High (VDD)	Low (VSS2)	4 cell prptection
Low (VSS2)	High (VDD)	3 cell prptection
Low (VSS2)	Low (VSS2)	prohibite

・Communication function when cascade connected

When using a cascade-connected IC with 6 or more cell protection, an overdischarge detection signal can be transmitted by inputting the DCHG output pin signal to the SDC pin via a resistor. If the current input to the SDC pin exceeds the SDC release current, it is recognized as normal state. If it drops below the SDC detection current or if it is open, it is recognized as overdischarge detection state. In the same way, an overdischarge detection signal can be transmitted by inputting the OV output pin signal to the SOC pin via a resistor.

In addition, charge / discharge is more controllable than inputting a signal into SDC terminal, SOC terminal from the outside independently.

Applications

・Lithium-ion rechargeable battery pack

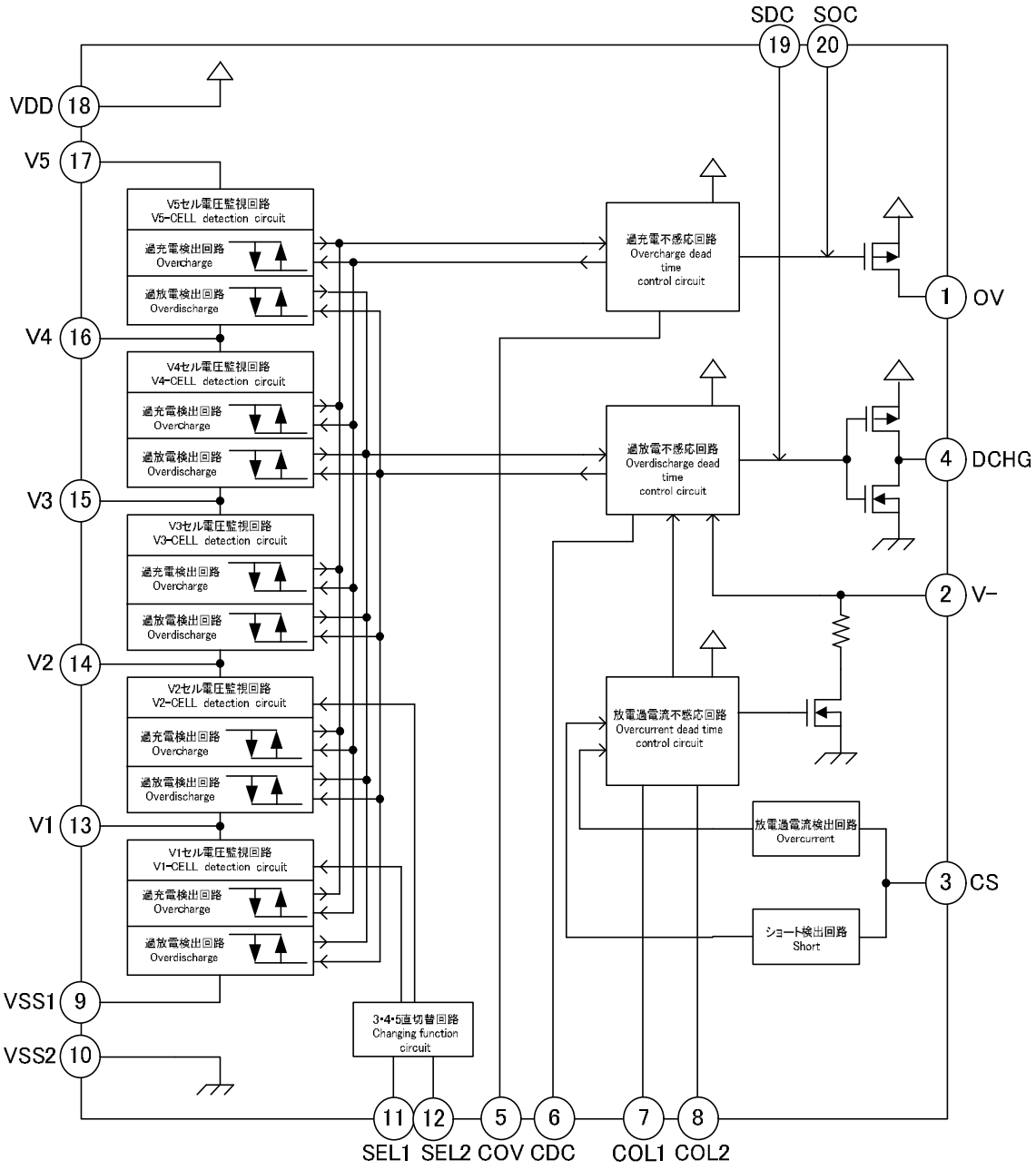
・Lithium polymer rechargeable battery pack

Package type

・TSOP-20C/20D　　6.50 × 6.40 × 1.10 [mm]

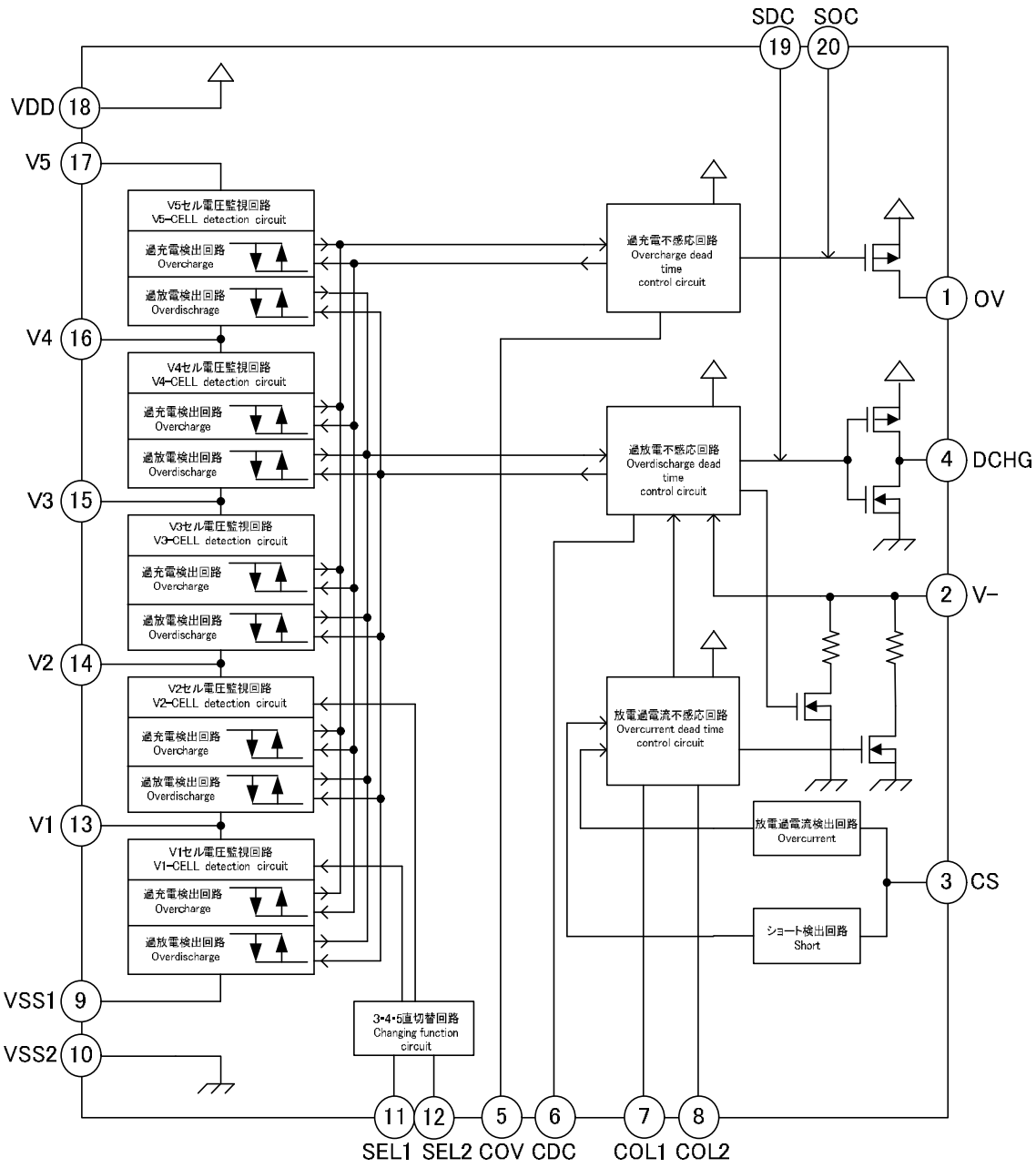
Block diagram

Overdischarge release : 「Voltage release」type



Block diagram

Overdischarge release : 「Load release + Voltage release」type



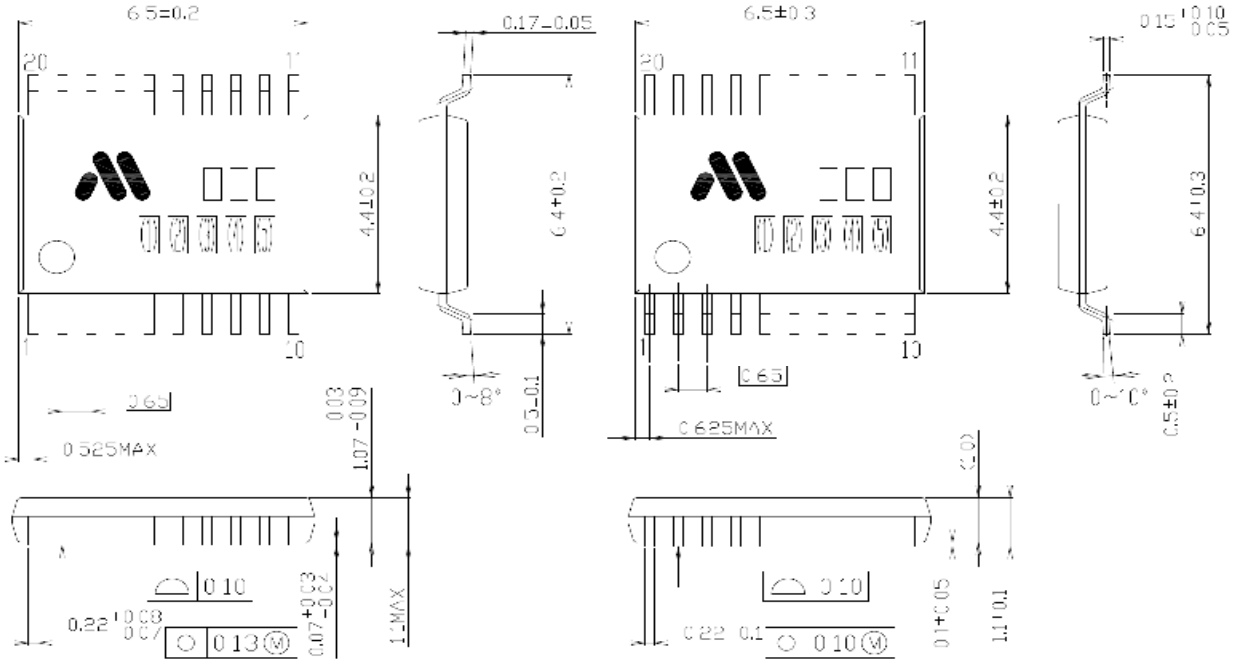
Package and pin configuration

Pin No.	Pin No.	Function
1	OV	Charge control output terminal. Output type is Pch open drain. Active "Hi impedance".
2	V-	Input terminal connected to charger negative voltage. Detected charger connection and load detection.
3	CS	Input of overcurrent detection. The voltage of the sense resistance is observed, and the overcurrent is detect
4	DCHG	Discharge control output terminal. Output type is CMOS. Active "Low".
5	COV	This pin is dead time setting of overcharge detection and release.
6	CDC	This pin is dead time setting of overdischarge detection and release.
7	COL1	This pin is dead time setting of overcurrent detection.
8	COL2	This pin is dead time setting of overcurrent release.
9	VSS1	The input terminal of the negative voltage of V1 cell .
10	VSS2	The input terminal of the ground of IC.
11	SEL1	This pin is for changing function for 3cell in series or 4cell in series , 5cell in series. SEL1 = H , SEL2 = H → 5Cell protection SEL1 = H , SEL2 = L → 4Cell protection SEL1 = L , SEL2 = H → 3Cell protection (SEL1=SEL2=L setting is prohibited.)
12	SEL2	
13	V1	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell .
14	V2	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell .
15	V3	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell .
16	V4	The input terminal of the positive voltage of V4 cell, and the negative voltage of V5 cell .
17	V5	The input terminal of the positive voltage of V5 cell .
18	VDD	The input terminal of the power supply of IC.
19	SDC	The control terminal of output over discharge detection.I $_{SDC}$<I$_{SDC}$L → DCHG=Low
20	SOC	The control terminal of output over charge detection.I $_{SOC}$<I$_{SOC}$L → OV=Hi impedance

Package dimensions

Unit:mm

TSOP-20C



Electrical characteristics

Unless otherwise specified, Topr=+25℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
ABSOLUTE MAXIMUM RATINGS						
VDD pin supply voltage	V_{VDDMAX}		VSS2-0.3	-	+30	V
V5 pin supply voltage	V_{V5MAX}		V4-0.3	-	VDD+0.3	V
Voltage between the input terminals of voltage of battery	$V_{CELLMAX}$		-0.3	-	+10	V
V- pin・OV pin supply voltage	V_{V-MAX}・V_{OVMAX}		VDD-30	-	VDD+0.3	V
CS pin・DCHG pin supply voltage	V_{CSMAX}・$V_{DCHGMAX}$		VSS2-0.3	-	VDD+0.3	V
SEL pin supply voltage	V_{SELMAX}		VSS2-0.3	-	VDD+0.3	V
SDC/SOCpin supply voltage	V_{SDCMAX}		VSS2-0.3	-	VDD+0.3	V
Storage temperature	Tstg		-55	-	+125	degC
Power dissipation	Pd		-	-	300	mW
RECOMMENDED OPERATING CONDITIONS						
Operating Temperature	TOPR		-40.0	-	+85	degC
Supply Voltage	VOPR		VSS2+3.5	-	VSS2+22.5	V
CURRENT CONSUMPTION						
Consumption current1（Vdd)	I_{DD1}	V_{CELL}=4.4V	-	10.0	20.0	uA
Consumption current2（Vdd)	I_{DD2}	V_{CELL}=3.5V	-	5.0	10.0	uA
Consumption current3（Vdd)	I_{DD3}	V_{CELL}=1.8V	-	1.5	3.0	uA
Consumption current1（V5)	I_{1V5}	V_{CELL}=4.4V	-	4.0	8.0	uA
Consumption current2（V5)	I_{2V5}	V_{CELL}=3.5V	-	3.0	6.0	uA
Consumption current3（V5)	I_{3V5}	V_{CELL}=1.8V	-	1.5	3.0	uA
V4・V3・V2・V1 input current	I_{V4}・I_{V3}・I_{V2}・I_{V1}	V_{CELL}=3.5V	-	-	±300	nA
SEL input current	I_{SEL}	V_{CELL}=3.5V , SEL=VDD	-	0.5	1.0	uA
SDC input current	I_{SDC}	V_{CELL}=3.5V , R_{SDC}=1MΩ	-	0.8	1.6	uA
SOC input current	I_{SOC}	VCELL=3.5V , R_{SDC}=1MΩ	-	0.8	1.6	uA
DETECTION/RELEASE VOLTAGE/CURRENT						
Overcharge detection voltage	V_{CELL}U	Ta=±0℃～+50℃	Typ-0.025	V_{CELL}U	Typ+0.025	V
Overcharge release voltage	V_{CELL}O		Typ-0.050	V_{CELL}O	Typ+0.050	V
Overdischarge detection voltage	V_{CELL}S		Typ-0.080	V_{CELL}S	Typ+0.080	V
Overdischarge release voltage	V_{CELL}D		Typ-0.100	V_{CELL}D	Typ+0.100	V
Overcurrent detection voltage	V_{OC}		Typ-0.015	V_{OC}	Typ+0.015	V
V- pin overcurrent release voltage	V_{VM}		Typ-0.030	V_{VM}	Typ+0.030	V
Short detection voltage	V_{SHORT}		Typ-0.100	V_{SHORT}	Typ+0.100	V
SDC detection current	I_{SDC}L	V_{CELL}=3.5V	-	-	0.1	uA
SDC release current	I_{SDC}H	V_{CELL}=3.5V	0.5	-	-	uA
SOC detection current	I_{SOC}L	V_{CELL}=3.5V	-	-	0.1	uA
SOC release current	I_{SOC}H	V_{CELL}=3.5V	0.5	-	-	uA
DETECTION DEAD TIME						
Overcharge detection dead time	t_{OV1}	C_{COV}=0.1uF	0.50	1.00	1.50	sec
Overcharge release dead time	t_{OV2}	C_{COV}=0.1uF	0.05	0.10	0.15	sec
Overdischarge detection dead time	t_{DC1}	C_{CDC}=0.1uF	0.50	1.00	1.50	sec
Overdischarge release dead time	t_{DC2}	C_{CDC}=0.1uF	-	-	15.0	msec
Overcurrent detection dead time	t_{OC1}	C_{COL1}=0.001uF	5.0	10.0	15.0	msec
Overcurrent release dead time	t_{OC2}	C_{COL2}=0.001uF	5.0	10.0	15.0	msec
Short detection dead time	t_{SHORT}		100	300	600	usec

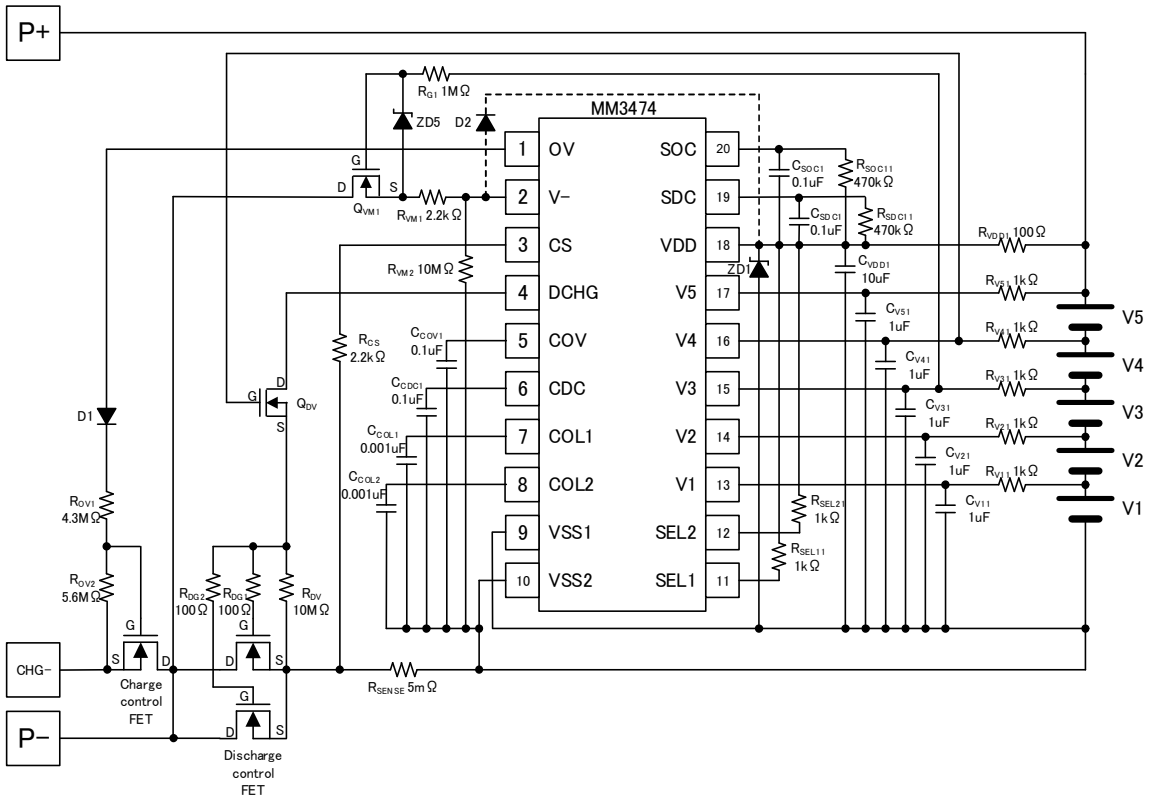
※1 Dead time can be set by external capacitor.

Electrical characteristics

Unless otherwise specified, Topr=+25℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	unit
OUTPUT PIN / SEL PIN						
DCHG source current	$I_{SO}D_{CHG}$	V_{DCHG}=VDD-0.5V	-	-	-20	uA
DCHG sink current	$I_{SI}D_{CHG}$	V_{DCHG}=0.5V	20	-	-	uA
DCHG output voltage H	$V_{TH}D_CH$	I_{SO}=-20uA	VDD-0.5	-	-	V
DCHG output voltage L	$V_{TH}D_CL$	I_{Si}=20uA	-	-	0.5	V
OV source current	$I_{SO}O_V$	V_{OV}=VDD-0.5V	-	-	-20	uA
Ov leak current	$I_{LEAK}O_V$	V_{OV}=VSS2	-	-	0.1	uA
SEL input voltage L	$V_{SEL}L$		-	-	0.5	V
SEL input voltage H	$V_{SEL}H$		VDD-0.5	-	-	V
V- pin pulldown resistance	V_{PD}	V_{CELL}=3.5v , V-=1V	15	30	60	kΩ

Typical application circuit



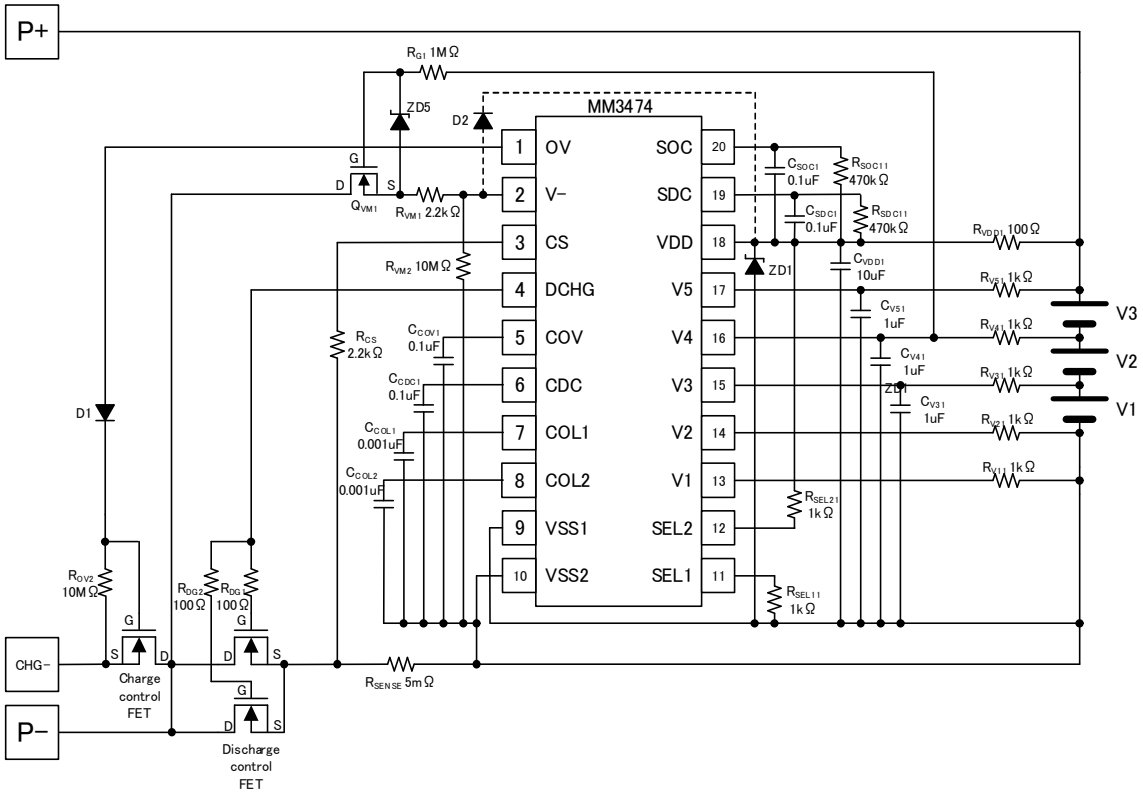
Parts name	Roles of parts
R_{VDD1}・R_{V51}・R_{V41}・R_{V31}・R_{V21}・R_{V11}	CR low-pass filter to stabilize a supply ripple of VDD pin･V5pin･V4pin･V3pin･V2pin･V1pin.
C_{VDD1}・C_{V51}・C_{V41}・C_{V31}・C_{V21}・C_{V12}	
R_{SEL11}・R_{SEL21}	Resistor to protect terminal.
R_{SDC11}・R_{SOC11}	Current limitation resistor. (The voltage signal is converted into the current signal by this resistor at the cascading connection.)
C_{COV1}	Capacitor to sets overcharge detection/release dead time.
C_{CDC1}	Capacitor to sets overdischarge detection/release dead time.
C_{COL1}	Capacitor to sets overcurrent detection dead time.
C_{COL2}	Capacitor to sets overcurrent release dead time.
R_{SENSE}	Sense resistance to observe discharging current.
R_{CS}	Resistor to protect terminal.
R_{VM1}	Resistor to protect terminal.
R_{DG1}・R_{DG2}	Resistor for preventing the gate destruction due to parasitic oscillation.
Q_{DV}・R_{DV}	The voltage between gate and source of FET must not exceed the absolute maximum rating. Therefore, The output voltage is clamped by FET or divided with a resistor.
R_{OV1}・R_{OV2}	
Q_{VM1}・R_{VM2}	FET to prevent voltage input to V-pin from rising more than voltage of VDD pin.
ZD5・R_{G1}	Zener diode and resistor to prevent VGS of Q_{VM1} from exceeding maximum rating.
D1	Diode to turn off FET quickly by discharging charge of parasitic capacitance of FET.
D2	When a V-pin becomes more than it in VDD pin voltage, it is Schottky barrier diode to bypass the electric current so that an electric current does not flow through the IC inside.
ZD1	Zener diode to prevent destruction of IC by surge voltage.
Charge control FET	Nch MOS FET to control charging current.
Discharge control FET	Nch MOS FET to control discharging current.

Examples of application circuit

Examples of 3 cells application circuit

Circuit condition

- Number of cells : 3 cells
- Charge and discharge route : Separated
- Overdischarge release method : Voltage release
- Optional functions : Nothing

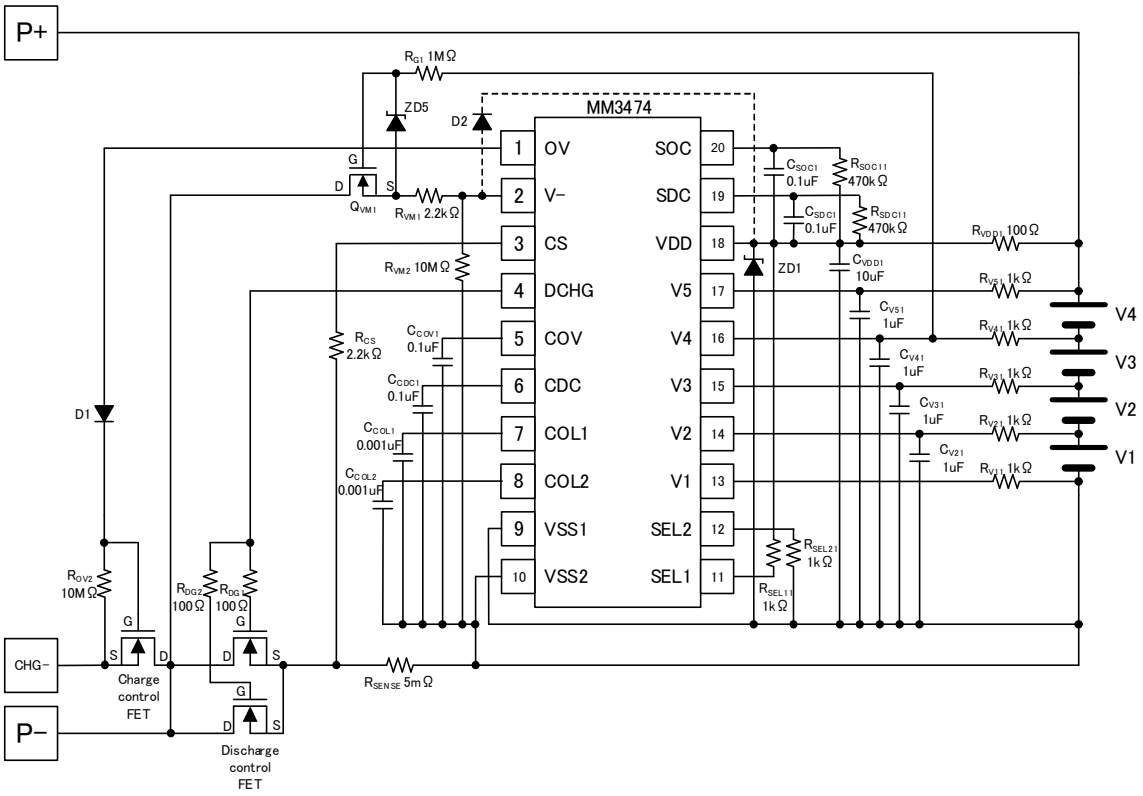


Examples of application circuit

Examples of 4 cells application circuit

Circuit condition

- Number of cells : 4 cells
- Charge and discharge route : Separated
- Overdischarge release method : Voltage release
- Optional functions : Nothing

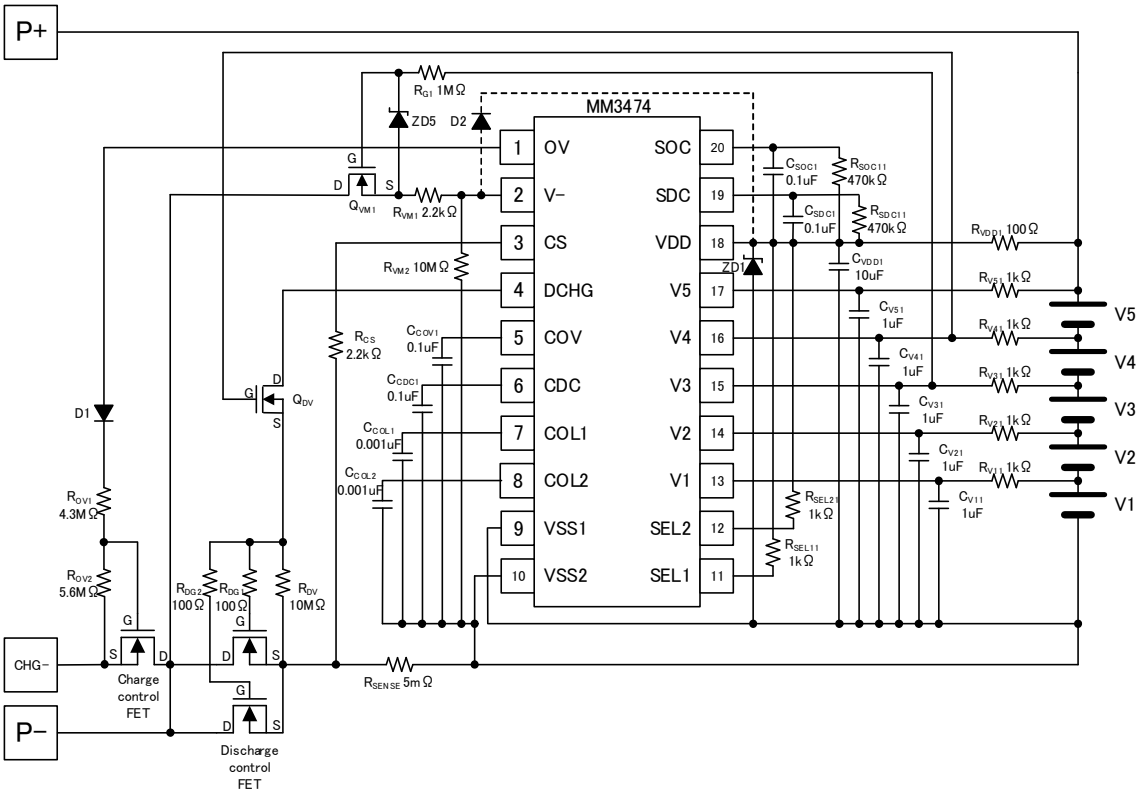


Examples of application circuit

Examples of 5 cells application circuit

Circuit condition

- Number of cells : 5 cells
- Charge and discharge route : Separated
- Overdischarge release method : Voltage release
- Optional functions : Nothing

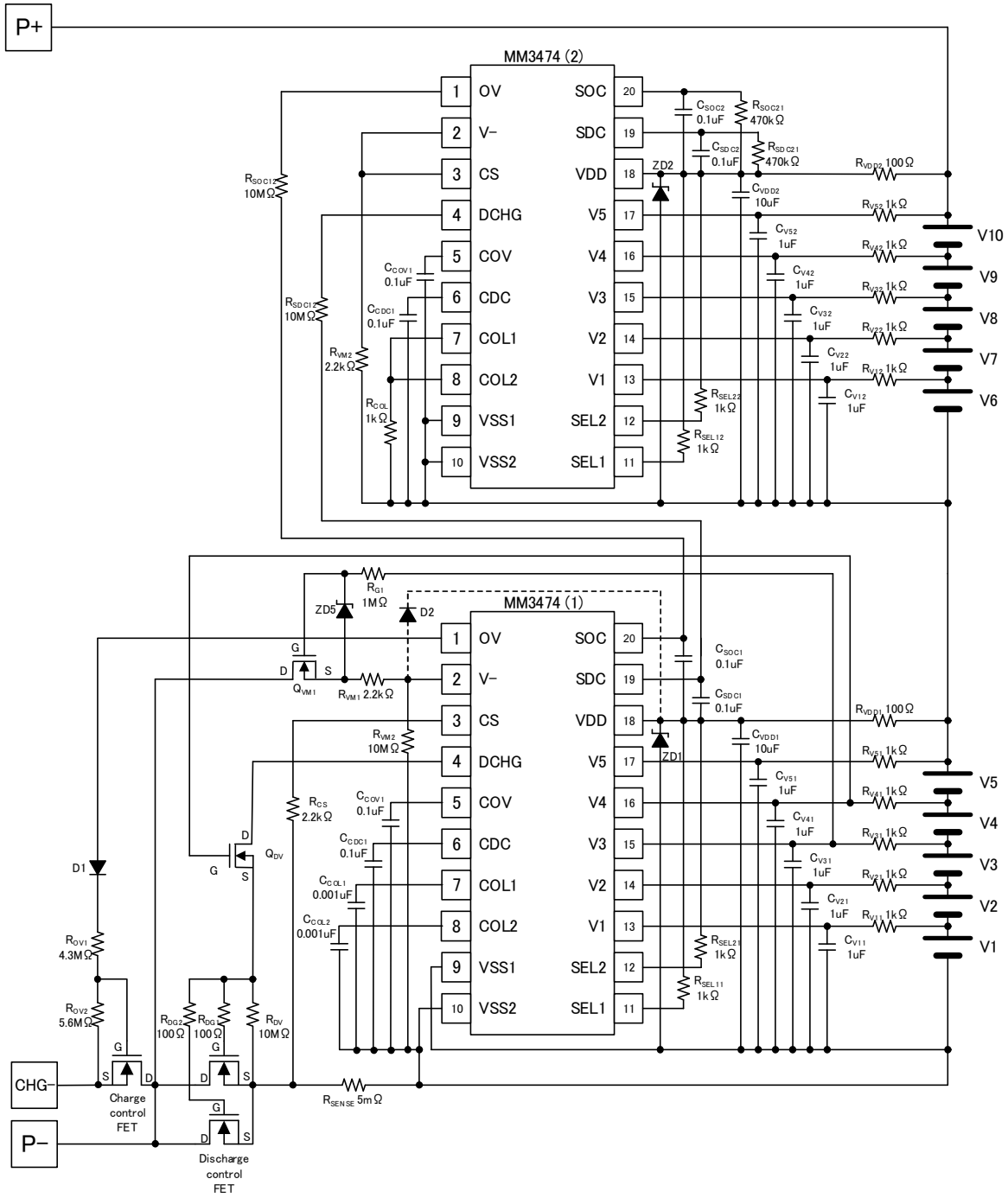


Examples of application circuit

Examples of 10 cells application circuit

Circuit condition

- Number of cells : 10 cells (5cells + 5cells)
- Charge and discharge route : Separated
- Overdischarge release method : Voltage release
- Optional functions : Nothing



Lineup

Product name (MM3474)	Detection / Release voltage						Detection / Release voltage						function
	Overcharge detection voltage	Overcharge release voltage	Overdischarge detection voltage	Overdischarge release voltage	Overcurrent detection voltage	Short detection voltage	Overcharge detection dead time	Overcharge release dead time	Overdischarge detection dead time	Overdischarge release dead time	Overcurrent detection dead time	Overcurrent release dead time	Overdischarge release
	$V_{CELL}U$	$V_{CELL}O$	$V_{CELL}S$	$V_{CELL}D$	V_{OC}	V_{SHORT}	t_{OV1}	t_{OV2}	t_{DC1}	t_{DC2}	t_{OC1}	t_{OC2}	※1
	V	V	V	V	mV	V	sec	msec	sec	msec	msec	msec	
C01VBE	4.250	4.150	2.800	3.000	250	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
C02VBE	4.250	4.150	2.400	2.600	250	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
C03VBE	4.250	4.150	2.800	3.000	250	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
C04VBE	4.250	4.150	2.800	3.000	150	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
C05VBE	4.250	4.150	2.800	3.000	150	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
D01VBE	3.850	3.650	2.300	2.500	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
D03VBE	3.800	3.600	2.000	2.500	150	0.60	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
E01VBE	4.250	4.150	2.800	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
E02VBE	4.200	4.100	2.800	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
E03VBE	4.175	4.100	2.800	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
E04VBE	4.250	4.150	2.800	3.000	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
E05VBE	4.250	4.150	2.800	3.000	50	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F01VBE	4.250	4.150	2.500	3.000	150	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F02VBE	4.200	4.100	2.500	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F03VBE	4.250	4.150	2.500	3.000	100	0.30	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
F04VBE	4.250	4.210	2.500	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F05VBE	4.250	4.150	2.500	3.000	100	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F06VBE	4.225	4.150	2.000	3.000	50	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F08VBE	4.400	4.300	2.500	3.000	120	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F11VBE	4.400	4.300	2.500	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
F12VBE	4.250	4.150	2.500	3.000	200	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G01VBE	4.200	4.100	2.750	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G02VBE	4.250	4.150	2.750	3.000	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G03VBE	4.200	4.100	2.750	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G05VBE	4.250	4.150	2.750	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G06VBE	4.225	4.100	2.750	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
G07VBE	4.250	4.150	2.750	3.000	100	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
J01VBE	4.250	4.100	2.800	3.000	50	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
K02VBE	4.250	4.100	3.000	3.225	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
K03VBE	4.250	4.190	3.000	3.200	80	0.70	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
K04VBE	4.175	4.100	3.000	3.200	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
L02VBE	3.750	3.550	2.200	2.700	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
L03VBE	3.650	3.500	2.000	2.700	200	0.25	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
L04VBE	3.750	3.550	2.200	2.700	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
M01VBE	4.350	4.150	2.300	3.000	150	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
N01VBE	3.900	3.600	2.000	3.000	100	0.20	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
P03VBE	4.230	4.220	2.800	3.400	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
P04VBE	4.200	4.170	2.750	2.800	100	1.00	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
P05VBE	4.200	4.140	2.750	2.810	100	0.50	1.0	0.1	1.0	Max.15	10.0	10.0	Latch
P06VBE	4.230	4.220	2.800	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
R03VBE ※2	4.225	4.100	2.750	3.000	100	0.80	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch
S01VBE	3.600	3.500	2.800	3.000	100	0.40	1.0	0.1	1.0	Max.15	10.0	10.0	Non Latch

※1 Non Latch : voltage release Latch : voltage release + load remove ※2 0V charge disable

NOTES

【Safety Precautions】

- Though Mitsumi Electric Co., Ltd. (hereinafter referred to as "Mitsumi") works continually to improve our product's quality and reliability, semiconductor products may generally malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of this product could cause loss of human life, bodily injury, or damage to property, including data loss or corruption. Before customers use this product, create designs including this product, or incorporate this product into their own applications, customers must also refer to and comply with (a) the latest versions or all of our relevant information, including without limitation, product specifications, data sheets and application notes for this product and (b) the user's manual, handling instructions or all relevant information for any products which is to be used, or combined with this products. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. Mitsumi assumes no liability for customers' product design or applications.

- This product is intended for applying to computers, OA units, communication units, instrumentation units, machine tools, industrial robots, AV units, household electrical appliances, and other general electronic units.

【Precautions for Product Liability Act】

- No responsibility is assumed by us for any consequence resulting from any wrong or improper use or operation, etc. of this product.

【ATTENTION】

- This product is designed and manufactured with the intention of normal use in general electronics. No special circumstance as described below is considered for the use of it when it is designed. With this reason, any use and storage under the circumstances below may affect the performance of this product. Prior confirmation of performance and reliability is requested to customers.
  Environment with strong static electricity or electromagnetic wave
  Environment with high temperature or high humidity where dew condensation may occur

- This product is not designed to withstand radioactivity, and must avoid using in a radioactive environment.

- This specification is written in Japanese and English. The English text is faithfully translated into the Japanese. However, if any question arises, Japanese text shall prevail.