A17700

Pressure Sensor Interface and Signal Conditioning IC with Polynomial Signal Compensation and Advanced Diagnostics

FEATURES AND BENEFITS

- Directly interfaces with strain gauge or other transducer in Wheatstone bridge configuration for low noise and high accuracy measurements
- On-chip Poly(4,4) compensation for improved accuracy over temperature, compensating both IC and bridge
- Offering from Poly(1,1) to Poly(4,4) polynomial compensation including any possible degree between 0 and 4 like Poly(2,4) and Poly(3,3).
- Ratiometric analog output for legacy applications
- High bandwidth option to support fast response time applications
- PWM (Pulse-Width Modulated) output with optional diagnostics to identify fault conditions
- SENT (Single-Edge Nibble Transmission) output configurable for temperature or diagnostic reporting in addition to pressure data
- Fast SENT provides increased data rates to support fast response time applications
- Manchester interface for programming through single OUT pin
- Internal device temperature available on output via SENT protocol (or volatile registers)
- Suite of diagnostics to allow for safety-critical systems fault detection
  - Broken wire detection
  - Under- and overvoltage detection
  - Under- and overtemperature detection

Continued on next page...

DESCRIPTION

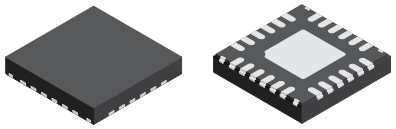
The A17700 is a sensor interface IC designed to connect directly to a strain gauge or other sensor in a Wheatstone bridge configuration. The A17700 amplifies and converts the analog input from the bridge to the digital domain, low-pass filters the signal, and outputs a ratiometric analog signal or a digital SENT/PWM protocol. Digital signal processing functions, including temperature compensation and gain/offset trim, provide an accurate and linear output. A Manchester programming interface for configurations is also available. It includes on-chip EEPROM technology capable of supporting up to 100 read/write cycles for programming of calibration parameters.

The A17700 incorporates advanced diagnostic functions to support safety-critical application designs.

The A17700 is available in a 24-pin 4 mm × 4 mm QFN package with wettable flank and exposed thermal pad.

PACKAGE:

24-pin wettable flank QFN
with exposed thermal pad (suffix ES)



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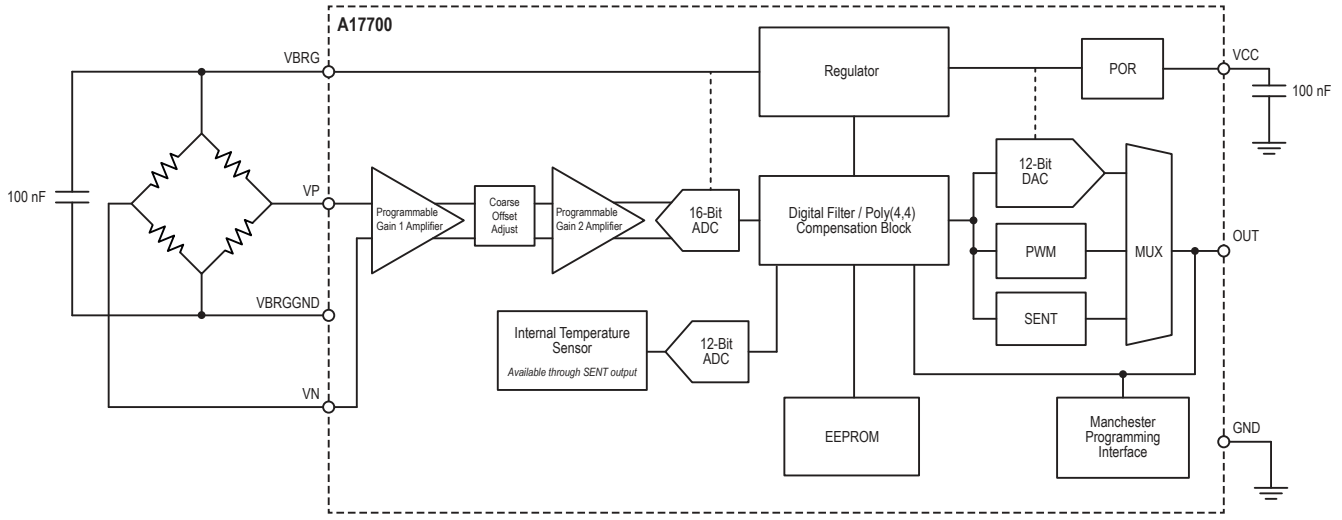

Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (continued)

- ○ Bridge diagnostics
- ○ Input signal Out-of-Range detection
- EEPROM with Error Correction Control (ECC) for trimming capability and product traceability
- AEC-Q100 Grade 0
- Wide operating temperature range: –40°C to 150°C
- QFN package with redundant bridge supply pins for PCB board space optimization
- Wettable flanks enabling visual inspection of solder joints

SELECTION GUIDE

Part Number	Output	Packing	Packing
A17700LESBTR-AO	Analog Output	24-pin QFN with wettable flank and exposed thermal pad	1500 pieces per 7-inch reel
A17700LESBTR-DO	Digital Output (SENT/PWM)	24-pin QFN with wettable flank and exposed thermal pad	1500 pieces per 7-inch reel

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		24	V
Reverse Supply Voltage	V_{RCC}	Voltage delta between supply and output must not exceed 24 V	–18	V
Output Pin Forward Voltage	V_{OUT}	Voltage delta between supply and output must not exceed 24 V	24	V
All Other Pins Forward Voltage [2]	V_{IN}		3.6	V
Output and All Other Pins Reverse Voltage [2]	V_R		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] Stresses beyond the Absolute Maximum Ratings may result in permanent device damage.
[2] “All Other Pins” refer to the pins that are driven by the device and should not be connected to external supplies.

THERMAL CHARACTERISTICS: May require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB based on JEDEC standard	136	°C/W
		Four-layer PCB based JEDEC standard	37	°C/W

[3] Additional thermal information available on the Allegro website.

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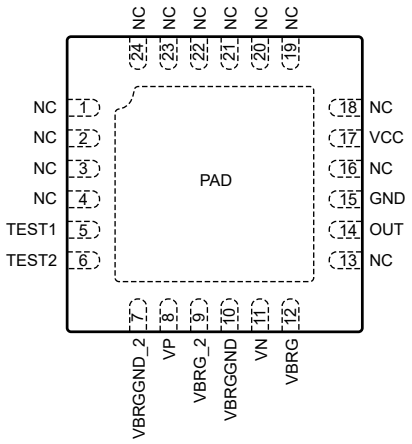
PINOUT DIAGRAMS AND TERMINAL LIST



Package ES, 24-Pin QFN Pinout Diagram

Terminal List Table

Number	Name	Function
1 to 4	NC	No internal connection [1]
5	TEST1	Factory Test Pin 1; connect to GND
6	TEST2	Factory Test Pin 2; connect to GND
7	VBRGGND_2	2nd GND pin for the bridge [2]
8	VP	Positive bridge output
9	VBRG_2	2nd bridge supply pin [3]
10	VBRGGND	GND pin for the bridge
11	VN	Negative bridge output
12	VBRG	Bridge supply
13	NC	No internal connection [1]
14	OUT	Analog / open drain output
15	GND	Ground
16	NC	No internal connection [1]
17	VCC	Supply voltage
18 to 24	NC	No internal connection [1]
–	PAD	Exposed thermal pad

[1] For increased ESD performance, connect NC (no connection) pins to GND.
[2] This is a second ground pin for the bridge intended for single layer PCB design. Internally connected to VBRGGND. Connect to GND if not used.
[3] This is a second bridge supply pin intended for single layer PCB design. Internally connected to VBRG. Leave floating if not used.

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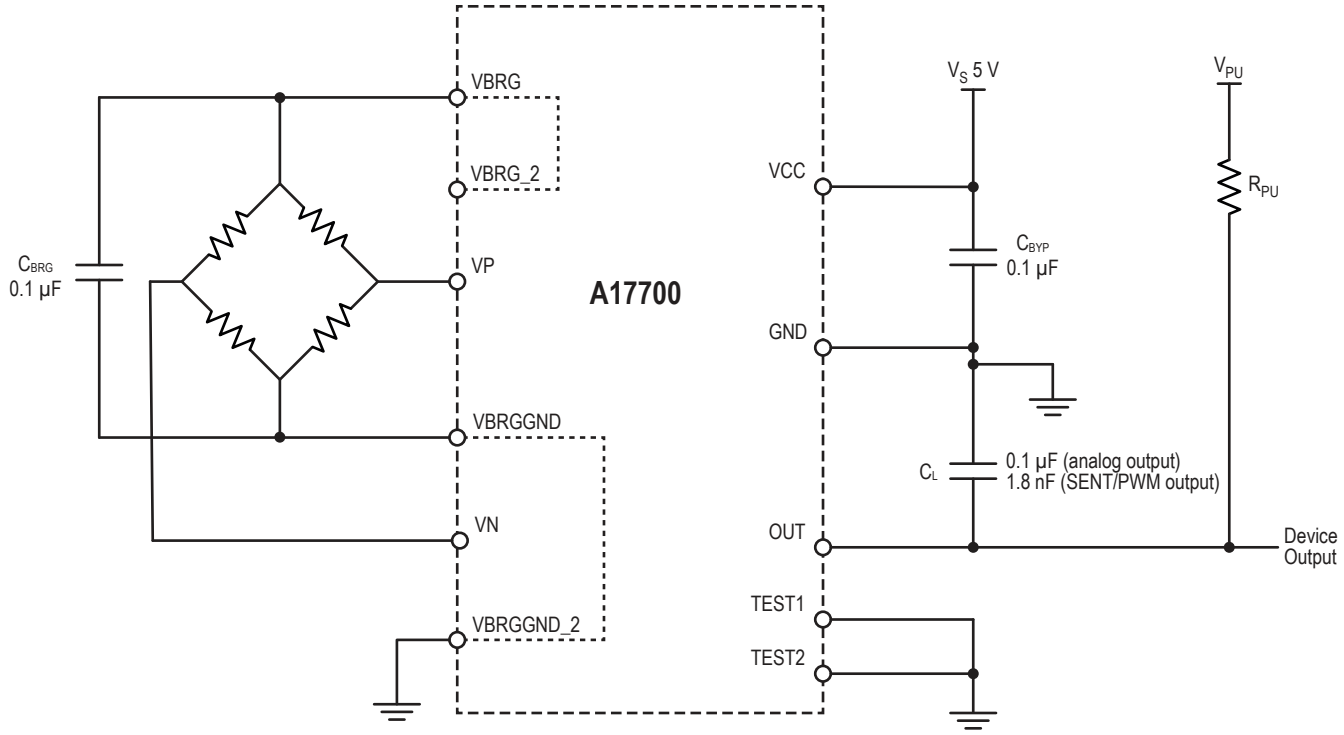

Figure 2: Typical Application Circuit

Note: VBRG and VCC decoupling caps must be mounted as close as possible to device package.
For increased ESD performances, connect NC (no connection) pins to GND.

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OPERATING CHARACTERISTICS: Valid over the full supply voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	Excluding external bridge and output load	–	6	10	mA
Supply Zener Clamp Voltage	V_{Zsup}	$I_{CC} = I_{CC(max)}$ + 30 mA; T_A = 25°C	24	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RZsup}	I_{CC} = –25 mA; T_A = 25°C	–	–	–18	V
Power-On Time [1]	t_{PO}	Time between min V_{CC} reached and analog output reaches 90% of final value; bandwidth (BW) >1.2 kHz	–	–	1	ms
Power-On Reset Voltage	$V_{POR(R)}$	V_{CC} rising; see Figure 3	3.6	–	4.0	V
	$V_{POR(F)}$	V_{CC} falling; see Figure 3	3.3	–	3.8	V
	$V_{POR(hys)}$	Hysteresis	100	–	500	mV
Undervoltage Detection	$V_{UVD(R)}$	V_{CC} rising, T_A = 25°C; see Figure 3	4.1	–	4.5	V
	$V_{UVD(F)}$	V_{CC} falling, T_A = 25°C; see Figure 3	4.0	–	4.4	V
	$V_{UVD(hys)}$	Hysteresis	70	–	500	mV
Overvoltage Detection	$V_{OVD(R)}$	V_{CC} rising, T_A = 25°C; see Figure 3	5.7	–	6	V
	$V_{OVD(F)}$	V_{CC} falling, T_A = 25°C; see Figure 3	5.5	–	5.8	V
	$V_{OVD(hys)}$	Hysteresis	100	–	500	mV
Initial Bandwidth [1]	$BW_{2.5}$	Default bandwidth setting	–	2.5	–	kHz
Programmable Operating Bandwidth Range [1][2]	BW_{prog}	Set by programming the digital low-pass filter	0.3	–	20	kHz
Initial Output Response Time [2]	$t_{resp\text{-}Init}$	Bandwidth option: $BW_{2.5}$	–	250	–	µs
BRIDGE ELECTRICAL CHARACTERISTICS						
Bridge Supply Voltage	V_{BRG}	Voltage supplied to transducer bridge	3.15	3.3	3.45	V
Bridge Resistance	R_{BRG}	Resistance of transducer bridge	1.5	–	10	kΩ
Bridge Bypass Capacitor	C_{BRG}	Bypass capacitor	80	100	150	nF
ANALOG FRONT END CHARACTERISTICS						
Differential Input (V_P-V_N)	V_{IN}	Gain1 = 3×, Gain2 = 1×, $Offset_{coarse}$ = 0, V_{BRG} = 3.3 V	–290	–	290	mV
ADC Input Range [3]	ADC_{IN}		–263	–	263	mV/V
Bridge Sensitivity [1][3]	BRG_{sens}	V_P-V_N at maximum input stimulus	10	–	80	mV/V
Bridge Sensitivity Programming Bits	–	Gain1 Trim bits	–	2	–	bits
		Gain2 Trim bits	–	4	–	bits
Bridge Offset [1][3]	$OFFSET_{coarse}$	Differential output offset, V_P-V_N, no input stimulus; Scales with Gain1; Gain1 = 3×; see Table 4	–80	–	80	mV/V
Bridge Offset Programming Bits	–	Number of Offset trim bits	–	6	–	bits
Bridge Offset Programming Step Size	$OFFSET_{stp}$	Scales with Gain1; Gain1 = 3×; see Table 4	–	2.667	–	mV/V
Polarity Bit	pol_bit	Inverts the polarity of bridge input, in digital domain	–	1	–	bit

[1] Guaranteed by design. Not tested in production.
[2] See Bandwidth selection in Functional Description section for details.
[3] Analog front end gain and differential offset can be adjusted to adapt the bridge signal to the chip ADC input range. Note that offset scales with Gain 1 (Table 4). See Front End Gain and Offset Adjustment or Input Signal range calculation sections for details.

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OPERATING CHARACTERISTICS: Valid over the full supply voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG OUTPUT CHARACTERISTICS						
Analog Output Effective Resolution [1]	RES_{OUT}	Across entire code range, theoretical noise-free input, BW = 2.5 kHz; Gain1 = 3× (default)	–	12.8	–	bits
Analog Output Clamp Range [1]	$V_{CLAMP(HIGH)}$	V_{CC} = 5 V, R_{PD} ≥ 4.4 kΩ or R_{PU} ≥ 4.4 kΩ; see Table 7	70	–	96	% V_{CC}
	$V_{CLAMP(LOW)}$	V_{CC} = 5 V, R_{PU} ≥ 4.4 kΩ or R_{PD} ≥ 4.4 kΩ; see Table 7	4	–	30	% V_{CC}
Analog Output Clamp Programming Step Size [1]	$V_{CLAMP(STP)}$	Valid for $V_{CLAMP(HIGH)}$ and $V_{CLAMP(LOW)}$	–	1	–	% V_{CC}
Analog Output Clamp Low Value	$V_{LIMCLAMP(LOW)}$	V_{CC} = 5 V, 1.1 mA forced to output, Clamp_Low code 0 (default)	0.1	0.2	0.3	V
Analog Output Clamp High Value	$V_{LIMCLAMP(HIGH)}$	V_{CC} = 5 V, 1.1 mA forced to output, Clamp_High code 0 (default)	4.7	4.8	4.9	V
Analog Output Load Capacitance [2]	C_L		10	100	120	nF
Maximum Sourcing Current	I_{source}		10	–	30	mA
Maximum Sink Current	I_{sink}		10	–	30	mA
Output Slew Rate [1]	SR	I_{source} = 10 mA, C_L = 100 nF	–	–	100	V/ms
Analog Output Load Resistance	R_{PU}	Pull-up or pull-down resistor	4.4	10	–	kΩ
Output Noise [1]	$V_{OUTnoise}$	V_{DD_DAC} = 5.0 V, BW = 2.5 kHz, T_A = 25°C, C_L = 100 nF; DC input signal; V_P = V_N; Gain1 = 3× (default) and Gain2 = 7× (max)	–	0.65	–	mV_{RMS}
DC Output Impedance [1][3]	R_{OUT}	T_A = 25°C	–	1	–	Ω
Analog Output Ratiometry Error [1]	Rat_{Err}	Across specified V_{CC} range; relative to V_{CC} = 5 V; output range from 10% to 90% V_{CC}; Gain1 = 3× (default)	–	±0.2	–	%
Output Linearity [1]	Lin_{ERR}	Full-Scale Linearity Error (INL); output range from 10% to 90% V_{CC}; Gain1 = 3× (default), Gain2 = 1×	–	±0.2	–	%V_{CC}
Overall Accuracy [1][4]	–	Over lifetime and temperature—Full signal path; Gain1 = 3× (default), Gain2 = 1×	–	±0.3	–	%V_{CC}
Pull-Up Voltage	V_{PU}	Connected as per typical application circuit	–	–	V_{CC}	V
BROKEN WIRE CHARACTERISTICS						
Analog Output Diagnostic Saturation Voltage (Broken Wire Detection)	$V_{sat\_diag\_H}$	V_{CC} = 5 V, broken GND, $I_{OUT(source)}$ = 1.1 mA	4.7	4.9	5.0	V
	$V_{sat\_diag\_L}$	V_{CC} = 5 V, broken VCC, $I_{OUT(sink)}$ = 1.1 mA	0.0	0.1	0.3	V

[1] Guaranteed by design. Not tested in production.
[2] Larger output load capacitance up to 330 nF is not tested in production but can be handled by the device with DAC Output Cap driver EEPROM parameter set to code 2 (See EEPROM MAP).
[3] Output impedance given for frequencies < 400 Hz.
[4] Overall accuracy considers ideal compensation over temperature and full Wheatstone bridge (all four resistors changing depending on sensed stress).

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PWM / SENT OUTPUT						
Output Load Resistance	R_{PU}	Pull-up resistor; output current ≥ –10 mA	1.2	–	–	kΩ
External Load Capacitor	C_L	Open-drain output mode	–	–	4.7	nF
Output Low Saturation Voltage	$V_{OUT(Sat)LOW}$	Output current = –4.7 mA, V_{CC} = 5 V, Output FET on	–	–	0.35	V
Output Leakage Current	–	Output voltage ≤ 5.5 V, output FET off, Open-drain output mode	–	–	10	µA
Output High Saturation Voltage	$V_{OUT(Sat)HIGH}$	Output current = 4.7 mA, V_{CC} = 5 V, Output FET Push-pull output mode	4.3	–	–	V
Output Current Limit	I_{LIMIT}		18	25	35	mA
Pull-Up Voltage	V_{PU}		–	–	V_{CC}	V
Overall Digital Output Accuracy	–		–	0.3	–	%
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	Programmable through EEPROM; See description section	0.25	–	16	kHz
PWM Clamp Programming Range	$PWM_{CLAMP(H)}$		–	–	96	%DC
	$PWM_{CLAMP(L)}$		4	–	–	%DC
PWM Resolution [1]	RES_{PWM}	Noise-free input, f_{PWM} ≤ 2.67 kHz	–	12	–	bits
		Noise-free input, f_{PWM} ≤ 16 kHz	–	9	–	bits
PWM Output Jitter [1]	PWM_{JIT}	Noise-free input, f_{PWM} ≤ 2.67 kHz	–	0.025	–	%DC
		Noise-free input, f_{PWM} ≤ 16 kHz	–	0.18	–	%DC
PWM Carrier Frequency Tolerance	$f_{PWM-tol}$		–10	–	10	%
SENT INTERFACE SPECIFICATIONS						
SENT Tick Time [2]	t_{TICK}	Programmable through EEPROM; see description section	0.5	–	5	µs
SENT Tick Time Tolerance	TOL_{tick}		–10	–	10	%
SENT Message Duration	t_{SENT}	Tick time = 3 µs	–	–	1	ms
Fast SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks	–	96	–	µs
INTERNAL TEMPERATURE OUTPUT THROUGH SENT						
Internal Temperature Range	$T_{SENT-Range}$	12-bit digital temperature	–256	–	255	°C
Internal Temperature Resolution	$T_{SENT-step}$	Internal temperature sensor output digital step	–	0.125	–	°C

[1] Guaranteed by design. Not tested in production.
[2] See Table 6 in Functional Description section for details.

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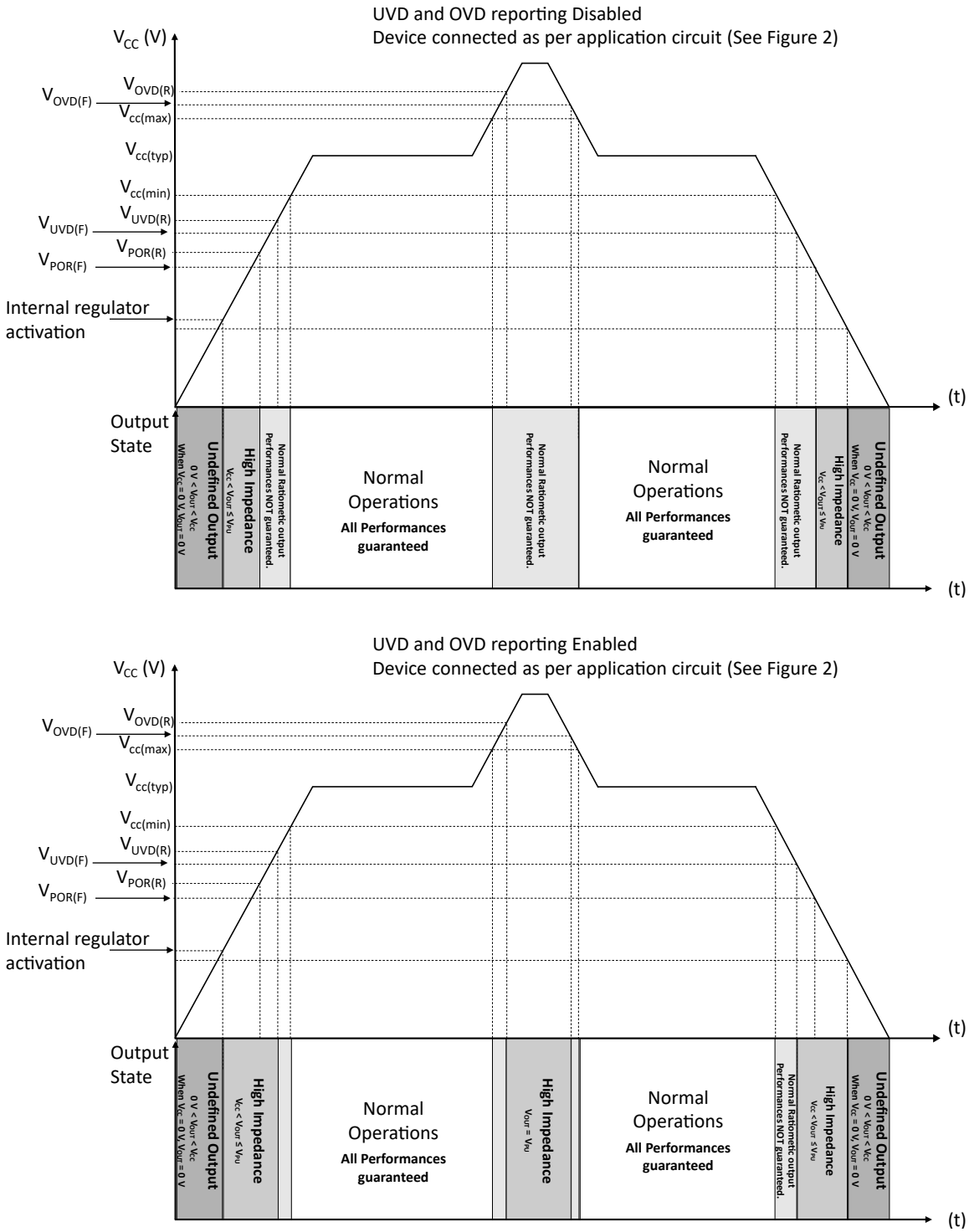

Figure 3: Output Behavior Under V_{CC} Ramp Conditions

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FUNCTIONAL DESCRIPTION

The A17700 is a signal conditioning IC that accepts a differential Wheatstone bridge input. The bridge signal is amplified with a programmable gain amplifier, and a coarse offset is applied. The purpose of this front end is to fill the ADC range as much as possible, but also ensure that the ADC is not saturated over temperature and operating conditions. The DSP logic will then provide a filter to reduce noise (also setting the effective operating bandwidth of the device) to the application bandwidth and apply fine signal adjustments and temperature compensation through polynomial equation (up to $poly_{4,4}$). The output can be selected between ratiometric analog output, SENT, or PWM.

Bandwidth Selection

The internal filter bandwidth can be adjusted to minimize output noise and improve resolution in function of the system bandwidth. The choice of bandwidth will be a compromise between response time and system resolution. Table 1 is provided to help define better option for the system.

Table 1: Bandwidth Selection Table

Bandwidth Code	Bandwidth	Typical Response Time	Ideal Noise-Free Resolution at Given Bandwidth (2.2 kΩ bridge and 25 mV/V sensitivity)
0 (Default)	2.5 kHz	250 µs	13.7 bits
1	0.3 kHz	1350 µs	15.0 bits
2	0.6 kHz	750 µs	14.6 bits
3	1.0 kHz	470 µs	14.4 bits
4	2.5 kHz	250 µs	13.7 bits
5	5.0 kHz	170 µs	12.7 bits
6	10 kHz	130 µs	11.8 bits
7	20 kHz	110 µs	10.6 bits

Output Response Time

The output response time is the time interval between a) when input stimulus reaches 80% of its final value and b) the sensor reaches 80% of its final output, input signal being a step impulse (square signal).

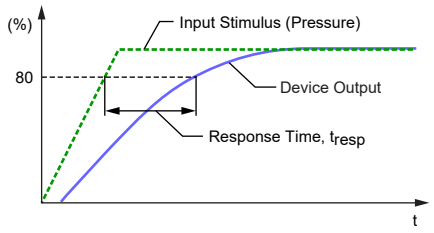

Figure 4: Output Response Time Definition

Power-On Time

Power-On Time is defined as the time it takes for the output to settle within ±10% of its steady-state value under an applied stimulus (pressure), after the power supply has reached its minimum specified operating voltage, V_{CC}(min).

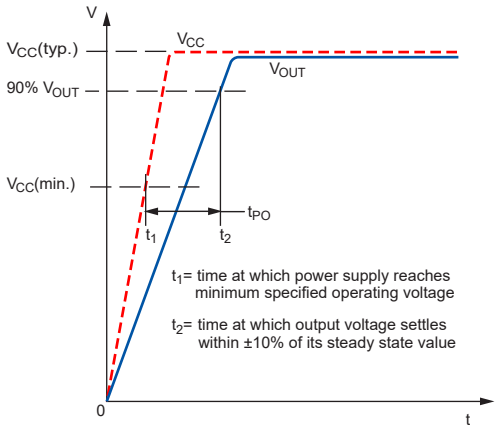

Figure 5: Power-On Time Definition

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Front End Gain Adjustment

GAIN 1

The front end gain 1 amplifier can be adjusted with 2 bits to optimize the ADC input range and offset differential step.

Table 2: Front End Gain 1 Selection

Coarse Gain Code	Gain 1
0 (Default)	3
1	6
2	9
3	12

GAIN 2

The front end gain 2 amplifier can be adjusted with 4 bits to further optimize ADC input range.

Table 3: Front End Gain 2 Selection

Coarse Gain Code	Gain 2
0 (Default)	1.0
1	1.4
2	1.8
3	2.2
4	2.6
5	3.0
6	3.4
7	3.8
8	4.2
9	4.6
10	5.0
11	5.4
12	5.8
13	6.2
14	6.6
15	7.0

Front End Differential Offset Adjustment

The Differential signal offset can also be programmed with 6 bits to center signal to ADC input range. Differential ADC Input Voltage (V_{IN_ADC}) can be derived from Equation 1.

The offset is also expressed in the function of bridge sensitivity for ease of use (See Table 4).

Table 4: Front End Offset selection

Coarse Offset Code	Differential Offset (mV/V)			
	Gain 1 = 3×	Gain 1 = 6×	Gain 1 = 9×	Gain 1 = 12×
0 (default)	0.0	0.0	0.0	0.0
1	2.7	1.3	0.9	0.7
2	5.4	2.7	1.8	1.3
3	8.0	4.0	2.7	2.0
...	...	...	...	...
30	80.3	40.2	26.8	20.1
31	83.0	41.5	27.7	20.8
32	–85.7	–42.8	–28.6	–21.4
33	–83.0	–41.5	–27.7	–20.8
...	...	...	...	...
61	–8.0	–4.0	–2.7	–2.0
62	–5.4	–2.7	–1.8	–1.3
63	–2.7	–1.3	–0.9	–0.7

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Input Signal Range Calculation

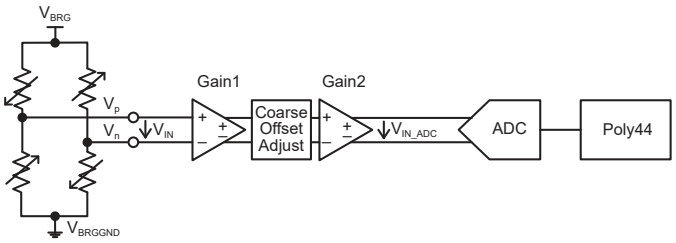

Figure 6

ADC input range (V_{IN_ADC} in Figure 6) can be calculated in function of differential input signal (V_{IN} in Figure 6) with the following Equation 1.

Equation 1:

$$V_{IN\_ADC} = Gain1 \times Gain2 \times [(V_{IN} + V_{BRG} \times OFFSET_{coarse}) \times (-1)^{polarity\_bit}]$$

where

Gain1 and Gain2 are respectively defined in Table 2 and Table 3,

Pol_bit is the polarity bit,

$OFFSET_{coarse}$ is defined in Table 4 (mV/V), $OFFSET_{coarse}$ scales with Gain1

$V_{IN} = V_p - V_n$ (mV), and

V_{BRG} is bridge supply from A17700 (3.3 V typ).

V_{IN_ADC} could also be expressed in function of ADC_{IN}:

$$V_{IN\_ADC} = ADC_{IN} \times V_{BRG}.$$

EXAMPLE OF SIGNAL RANGE CALCULATIONS

Considering a bridge of the following characteristics:

Sensitivity: +35 mV/V

Offset: +10 mV/V

Maximum differential input value can be calculated as:

$$V_{IN\_MAX} = (BRG_{sens} + BRG_{off}) \times V_{BRG}$$

BRG_{sens} being the bridge sensitivity (mV/V);
BRG_{off} being the bridge offset (mV/V).

$$V_{IN\_MAX} = (0.035 + 0.010) \times 3.3 = 148.5 \text{ mV}$$

$$V_{IN\_MIN} = (0 + 0.01) \times 3.3 = 33 \text{ mV}$$

Therefore, V_{IN} will vary from 33 to 148.5 mV.

EXAMPLE OF COARSE GAIN AND OFFSET CALCULATIONS

Gain is calculated first:

Equation 2:

$$Gain1 \times Gain2 = V_{IN\_ADC} / [(V_{IN} + V_{BRG} \times OFFSET_{coarse}) \times (-1)^{polarity\_bit}]$$

Default $OFFSET_{coarse}$ value is 0, therefore:

$$Gain1 \times Gain2 = (V_{IN\_ADC(range)}) / (V_{IN} \times (-1)^{pol\_bit})$$

Focusing on signal range, where in this example, signal is unidirectional and anticipating for offset step size:

$$V_{IN\_ADC(range)} = V_{IN\_ADC(max)} - V_{IN\_ADC(min)} - Offset_{STP} \times V_{BRG}$$
$$= 2 \times V_{IN\_ADC(max)} - Offset_{STP} \times V_{BRG}$$
$$= (2 \times ADC_{IN(max)} - Offset_{STP}) \times V_{BRG}, \text{ and}$$

$$V_{IN(range)} = V_{IN(max)} - V_{IN(min)}$$

Then:

$$Gain1 \times Gain2 = 2 \times ADC_{IN}(max) \times V_{BRG} / [V_{IN(range)} \times (-1)^{pol\_bit}]$$
$$= ((2 \times 0.263 - 0.0027) \times 3.3) / (0.1485 - 0.033) \times 1 = 14.9$$

This number can be obtained with default Gain1 code, thus:

Gain1 = 3×, Gain 2 = 14.9 / 3 = 4.97 (code 9 is the matching lowest value).

Using this Gain configuration (Gain1 = 3×, Gain2 = 4.6×) with $OFFSET_{coarse}$ = 0 gives the following ADC_{IN} min/max values:

$$ADC_{IN}(max) = Gain1 \times Gain2 \times V_{IN\_MAX} / V_{BRG} = 621 \text{ mV/V}$$
$$ADC_{IN}(min) = Gain1 \times Gain2 \times V_{IN\_MIN} / V_{BRG} = 138 \text{ mV/V}$$

Gained-up signal must be centered to ADC input range using coarse offset compensation:

Total Offset = (621 + 138) / 2 = 379.5 mV/V,
$OFFSET_{coarse}$ code = (–379.5 / (3 × 4.6)) / 2.667 = –10.3 ↔ code –10.

Therefore, ADC_{IN} min/max values become:

ADC_{IN} (max) = 253 mV/V
ADC_{IN} (min) = –230 mV/V

Fine Adjustment and Temperature Compensation

The A17700 uses an internal DSP to fine adjust offset and sensitivity and to compensate for nonlinearity over temperature. The compensation algorithm takes as inputs the pressure as sensed by the external pressure sensor (Wheatstone bridge) and the temperature as sensed by the internal temperature sensor. The DSP compensates the pressure with a polynomial function up to 4th order that also includes temperature.

Note that a_{00} is implicitly used to fine adjust the Offset and a_{10} is

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implicitly used to fine adjust the Sensitivity.

$$f(P_{SENSED}, T_{SENSED}) = a_{00} + a_{10} P_{SENSED} + a_{01} T_{SENSED} + a_{20} P^2_{SENSED} + a_{11} P_{SENSED} T_{SENSED} + a_{02} T^2_{SENSED} + a_{30} P^3_{SENSED} + a_{21} P^2_{SENSED} T_{SENSED} + a_{12} P_{SENSED} T^2_{SENSED} + a_{03} T^3_{SENSED} + a_{40} P^4_{SENSED} + a_{31} P^3_{SENSED} T_{SENSED} + a_{22} P^2_{SENSED} T^2_{SENSED} + a_{13} P_{SENSED} T^3_{SENSED} + a_{04} T^4_{SENSED}$$

This function uses 15 coefficients for full flexibility and therefore at least 15 calibration points are also required. A lower degree polynomial compensation can also be used (Poly(3,3), Poly(2,4), etc.); in such cases, the higher degree coefficients must receive a 0 value.

Note that all coefficients are calculated externally and fed into A17700. A least-squares fit technique can be used to calculate coefficient. All coefficients should be a number between –1 and 1. To load a coefficient to the EEPROM, it must be multiplied by the fractional length (2^{15}) and converted to a 16-bit two complement register.

Note: For optimized compensation, internal device temperature sensor input must be used.

EXAMPLE OF POLYNOMIAL COEFFICIENT CALCULATIONS

As input data, measurements at various temperatures and pressures must be performed. At each calibration point, the following two registers must be sampled with correct format:

Table 5

Name	Address	Register structure	Number of bits	Fractional length
adc_comp_reg	[15:0] at 0x52	Signed	16	15
tt_comp_reg	[11:0] at 0x62	Signed	12	11

Example: adc_comp_reg 0b1110 0011 1111 0010 → –0.219177246093750
tt_comp_reg 0b0000 1010 0000 → 0.078125000000000

Denote the adc_comp_reg samples as p_i, tt_comp_reg samples as t_i, and the applied pressure [bar] as P_i.

Then define variables for the least square fitting:

Matrix A:

$$A = \begin{bmatrix} 1 & p_1 & t_1 & p_1^2 & p_1 \cdot t_1 & t_1^2 & p_1^3 & p_1^2 \cdot t_1 & p_1 \cdot t_1^2 & t_1^3 & p_1^4 & p_1^3 \cdot t_1 & p_1^2 \cdot t_1^2 & p_1 \cdot t_1^3 & t_1^4 \\ 1 & p_2 & t_2 & p_2^2 & p_2 \cdot t_2 & t_2^2 & p_2^3 & p_2^2 \cdot t_2 & p_2 \cdot t_2^2 & t_2^3 & p_2^4 & p_2^3 \cdot t_2 & p_2^2 \cdot t_2^2 & p_2 \cdot t_2^3 & t_2^4 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \end{bmatrix}$$

Vector b:

$$b = \begin{bmatrix} b_1 \\ b_2 \\ \dots \end{bmatrix}$$

where $b_i = 2 \cdot \left(\frac{V(P2)-V(P1)}{4.6} \cdot \frac{P_i - P1}{P2-P1} + \frac{V(P1)-0.2}{4.6} \right) - 1$

where P1 and P2 are the operating pressures limit in bar, and V(P1) and V(P2) their corresponding voltages in volt.

The coefficients c are then derived by a bounded least square algorithm ($-1 \le c \le 1$):

$$c = \mathrm{lsqr}(A,b)$$

The second element in c, corresponding to a_{10}, must be decreased by a unity amount:

$$c(2) = c(2) - 1$$

Then, all the coefficients must be rescaled:

$$c = 0.0625 \times c$$

The coefficients are ready to be written to EEPROM with correct format:

Table 6

Name	Address	Signedness	Number of bits	Fractional length
press_coeff_aXX	See memory map	Signed	16	15

Example: press_coeff_a00 –0.001770019531250 → 0b1111 1111 1100 0110

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Output Protocols

ANALOG OUTPUT MODE

The A17700 features an analog output, with the output voltage mapped proportionally to the compensated Wheatstone bridge output (V_P-V_N).

The analog output is ratiometric with V_{CC} for a more accurate reading and it includes programmable clamps for easy diagnostics.

Clamps

The output voltage clamps, $V_{CLAMP(HIGH)}$ and $V_{CLAMP(LOW)}$, are set in digital domain and limit the operating range of the applied input in which the device provides a linear output. Clamps can be programmed as per Table 7.

Table 7: Clamp Programming

Clamp-High Code	$V_{CLAMP(HIGH)}$	Unit		Clamp-Low Code	$V_{CLAMP(Low)}$	Unit
0 (Default)	96	$\%V_{CC}$		0 (Default)	4	$\%V_{CC}$
1	95	$\%V_{CC}$		1	5	$\%V_{CC}$
2	94	$\%V_{CC}$		2	6	$\%V_{CC}$
3	93	$\%V_{CC}$		3	7	$\%V_{CC}$
4	92	$\%V_{CC}$		4	8	$\%V_{CC}$
5	91	$\%V_{CC}$		5	9	$\%V_{CC}$
6	90	$\%V_{CC}$		6	10	$\%V_{CC}$
7	89	$\%V_{CC}$		7	11	$\%V_{CC}$
8	88	$\%V_{CC}$		8	12	$\%V_{CC}$
9	87	$\%V_{CC}$		9	13	$\%V_{CC}$
10	86	$\%V_{CC}$		10	14	$\%V_{CC}$
11	85	$\%V_{CC}$		11	15	$\%V_{CC}$
12	84	$\%V_{CC}$		12	16	$\%V_{CC}$
13	83	$\%V_{CC}$		13	17	$\%V_{CC}$
14	82	$\%V_{CC}$		14	18	$\%V_{CC}$
15	81	$\%V_{CC}$		15	19	$\%V_{CC}$
16	80	$\%V_{CC}$		16	20	$\%V_{CC}$
17	79	$\%V_{CC}$		17	21	$\%V_{CC}$
18	78	$\%V_{CC}$		18	22	$\%V_{CC}$
19	77	$\%V_{CC}$		19	23	$\%V_{CC}$
20	76	$\%V_{CC}$		20	24	$\%V_{CC}$
21	75	$\%V_{CC}$		21	25	$\%V_{CC}$
22	74	$\%V_{CC}$		22	26	$\%V_{CC}$
23	73	$\%V_{CC}$		23	27	$\%V_{CC}$
24	72	$\%V_{CC}$		24	28	$\%V_{CC}$
25	71	$\%V_{CC}$		25	29	$\%V_{CC}$
26	70	$\%V_{CC}$		26	30	$\%V_{CC}$
27-31	70	$\%V_{CC}$		27-31	30	$\%V_{CC}$

Values outside of the mapping range are used as the diagnostic signal indicating a malfunction of the device. When an external pull-up or pull-down is used, and an invalid mode is detected (i.e. short/broken bridge wire, under/overvoltage, ECC memory error, etc.) while diagnostics are enabled, the output will go to a high-impedance state.

With appropriate poly coefficients programmed to the device, the output can be set so that over-pressure or under-pressure can be diagnosed in addition to open/short wire or diagnostic detection. For example, a device could be trimmed so that output at P1 gives 10% V_{CC} and output at P2 equals 90% V_{CC}, while the clamps are set to 4 to 96%. In this case, output between 4 and 10% V_{CC} would reveal under-pressure (pressure < P1) fault, while output between 90 and 96% V_{CC} would reveal over-pressure (pressure > P2) fault. Output higher than 96% V_{CC} or lower than 4% V_{CC} informs that an open/short event occurred or that a diagnostic flag was raised (assuming diagnostic enabled). This is illustrated in Figure 7.

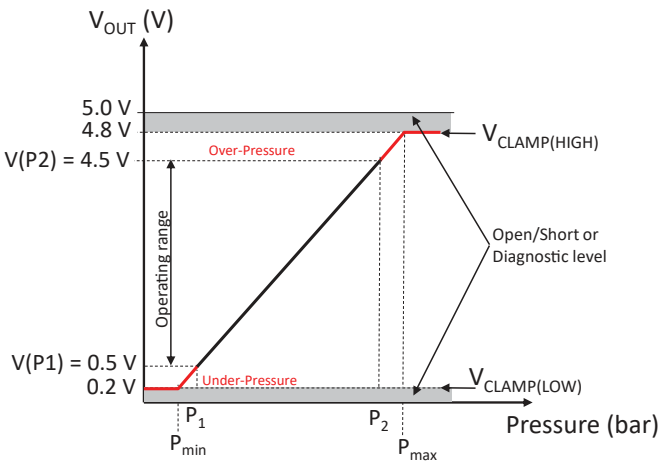

Figure 7: Output Level and Diagnostic Description

Ratiometry Error

The A17700 device features ratiometric output. This means that the Output and Clamp voltages are proportional to the supply voltage. When the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V and the measured change in each characteristic.

The ratiometric error in voltage output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

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$$Rat_{ERRVOUT(Q)} = \left(\frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V} \right) \times 100\ (\%)$$

where $V_{OUT(Q)}$ is the output when the bridge doesn't output differential signal.

The ratiometric error in clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRCLP} = \left(\frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V} \right) \times 100\ (\%)$$

where V_{CLP} is either $V_{CLAMP(HIGH)}$ or $V_{CLAMP(LOW)}$.

Linearity Sensitivity Error

The A17700 is designed to provide a compensated linear output in response to a ramping differential signal at pins V_P-V_N.

INL, Integral Non-Linearity, is a common performance measurement for DACs. It is the deviation between the ideal output values and the actual measured value once offset and gain have been accounted for. The equation below shows how this value was calculated:

$$INL = \frac{(V_{OUT}(c_i) - V_{OUT}(c_{min}) - (c_i - c_{min}) \times RefStep)}{RefStep}$$

where c_i is the input code and c_{min} is the minimum input code.

Reference step (RefStep) is the step size of the DAC in terms of analog value per bit. It is calculated as shown below.

$$RefStep = \frac{(V_{OUT}(c_{max}) - V_{OUT}(c_{min}))}{(c_{max} - c_{min})}$$

PWM OUTPUT MODE

PWM involves converting the output signal amplitude to a series of constant-frequency binary pulses, with the percentage of the high portion of the pulse directly proportional to the signal amplitude.

PWM carrier frequency is programmable from 0.250 kHz to 16 kHz for easier detection (refer to Table 8 for available options).

PWM uses clamps similarly to the analog output to limit the output range and for diagnostic purpose. Devices can be tuned to a maximum $PWM_{CLAMP(H)}$ value of 96% and a minimum $PWM_{CLAMP(L)}$ value of 4% DC (see Figure 8).

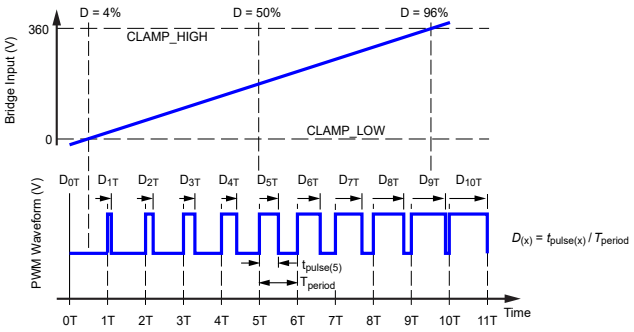

Figure 8: PWM Output Mode – Duty-Cycle-Based Waveform

SENT OUTPUT MODE

The SENT output mode converts the input bridge signal to a binary value mapped to the Full-Scale Output, FSO, for a range of 0 to 4095 as shown in Figure 9. This data is inserted into a binary pulse message, referred to as a frame, which conforms to the SENT data transmission specification (SAEJ2716). Certain parameters for configuration of the SENT messages can be set in EEPROM.

The SENT output modes are selected using the dig_out_mode EEPROM parameters:

- dig_out_mode = 2: SENT output as per SAEJ2716 (no Pause Pulse)
- dig_out_mode = 3: SENT output with Pause Pulse

SENT Message Structure

A SENT message is a series of nibbles with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low interval, SENT_FIXED, is defined as 5 SENT ticks. The high interval contains information and is variable in duration to indicate the data payload of the nibble.

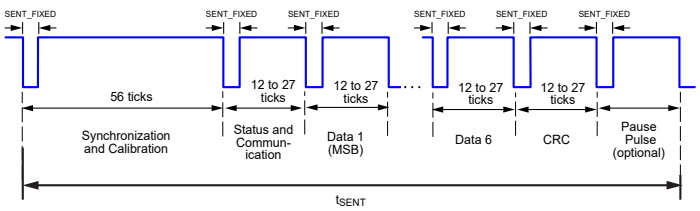

Figure 9: SENT Message

The duration of a nibble is denominated in clock ticks. The period of a tick is set by the Out_freq_rate parameter defined in Table 8.

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The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The nibbles of a SENT message are arranged in the following required sequence:

1. Synchronization and Calibration: flags the start of the SENT message
2. Status and Communication: provides A17700 status and the format of the data
3. Data: pressure and optional data
4. CRC: error checking
5. Pause Pulse (optional): sets timing relative to A17700 updates

Table 8: SENT/PWM rate parameters

Out_freq_rate Code	SENT Tick Time (µs)	PWM Carrier Frequency (Hz)	PWM Resolution (bits)
0 (default)	3	1000	12
1	5	250	12
2	2.5	500	12
3	2	1600	12
4	1.5	2667	12
5	1	4000	11
6	0.75	8000	10
7	0.5	16000	9

Synchronization and Calibration Pulse

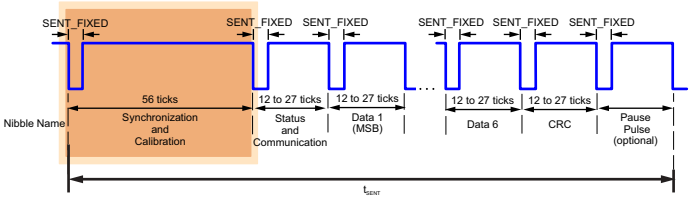

Figure 10: Synchronization and Calibration Pulse in SENT Message

The Synchronization and Calibration pulse is 56 ticks wide, measured from falling edge to falling edge, and delineates the start of a new message frame. The host microcontroller uses this pulse to rescale the subsequent nibble values to correct for clock variation between the controller and the sensor.

Status and Communication Nibble

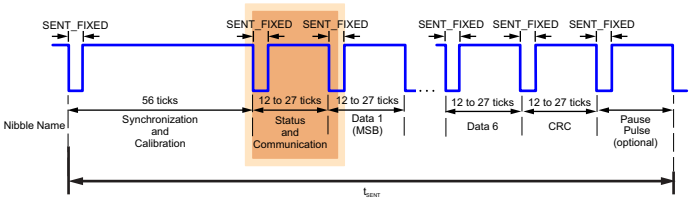

Figure 11: SCN Nibble in SENT Message

The Status and Communication Nibble (SCN) provides diagnostic information along with optional other data from the short serial message. Nibble contents are controlled via the SCN_MODE field within EEPROM (See Table 9).

By default, contents of the SCN are not included in the 4-bit CRC at the end of each SENT frame. The SENT_SCN_CRC bit within EEPROM enables CRC coverage of the SCN contents. It should be noted that this option is not specified in the SAEJ2716 SENT standard. With the SENT_SCN_CRC bit set, the CRC is no longer compliant with that outlined in the SENT specification.

Table 9: Status and Communication Nibble (SCN) modes

SCN Mode	Bit 3	Bit 2	Bit 1	Bit 0
0 (default)	0	0	Err	0
1	Serial sync	Serial data	Err	0
2	Serial sync	Serial data	0	0
3	0	0	0	0

The SCN has two different types of bit values that may be present, depending on the SCN_MODE setting. These are:

Error Bit

This bit is latched to 1 temporarily, and is cleared on the following SENT frame, unless fault is still asserted and considering that any of the following diagnostics are enabled: Undervoltage, Overvoltage, Overtemperature, Undertemperature, Signal out of Range, Open/Short Bridge.

Note that multi-bit EEPROM fault will trigger high-impedance output state.

Serial Data

Two bits, consisting of the SerialSync and SerialData bits. Together they form the Short Serial Message (per SAEJ2716 Section 5.2.4.1).

SerialSync: Indicates the start of a 16-bit serial message.

SerialData: Serial data, transmitted one bit at a time, MSB first.

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Optional Short Serial Message

The A17700 SENT output supports an optional mode to transmit additional data: the slow serial mode. It enables transmission of additional data by encoding information in the Status and Communication (SCN) nibbles. A 16-bit data packet is transmitted one bit at a time over consecutive SENT message frames, starting with the MSB. The beginning of each 16-bit packet is indicated by a "1" in the SerialSync bit. The message data is transmitted bit-by-bit via the SerialData bit (See Table 10 for Short Serial Message Format).

The slow serial mode is enabled when the EEPROM parameter SCN_mode is set to 1 or 2. Following a reset, the first message transmitted is 0, following in order of the message ID until message 4, and then repeating. Table 11 identifies the data sent with each message ID. The CRC for the Short Serial Message is derived for the Message ID and data, and is the same checksum algorithm used for the SENT CRC.

Table 10: Short Serial Message Format in SCN Nibble

SNC Bit	Frame #															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SerialSync	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SerialData	MessageID			Data									CRC			

Table 11: Serial Output Data

Message ID	Data
0	9-bit diagnostics, MSB always 0
1	9-bit internal temperature
2	9-bit customer scratch [8:0]
3	9-bit customer scratch [17:9]
4	9-bit customer scratch [25:18], MSB always 0

SENT Data Nibble Format

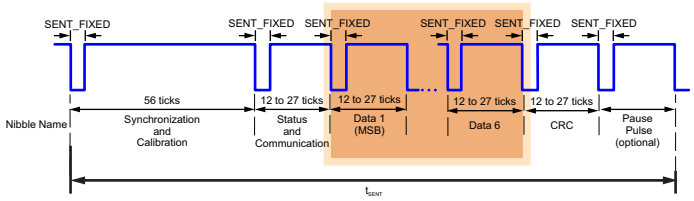

Figure 12: Data Nibble in SENT message

The A17700 supports options for the message data nibble format. The data nibble format is determined by the EEPROM parameter sent_data_cfg. The options for a minimum 3 or maximum 6 nibbles are defined in SENT data table (Table 12). For each option, data to be transmitted is sampled at the end of the SCN nibble.

Note that sent_data_cfg = 3 has the same effect as sent_data_cfg = 2.

Table 12: SENT Data Config

sent_data_cfg	Data Nibble #1	Data Nibble #2	Data Nibble #3	Data Nibble #4	Data Nibble #5	Data Nibble #6	# of Nibbles
0 (default)	Pressure [11:8]	Pressure [7:4]	Pressure [3:0]	–	–	–	3
1	Pressure [11:8]	Pressure [7:4]	Pressure [3:0]	Diag [7:4]	Diag [3:0]	–	5
2	Pressure [11:8]	Pressure [7:4]	Pressure [3:0]	IntTemp [11:8]	IntTemp [7:4]	IntTemp [3:0]	6

SENT CRC Nibble

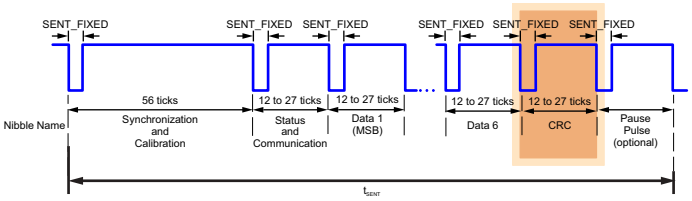

Figure 13: CRC Nibble in SENT message

The CRC nibble is a 4-bit error checking code, implemented per the SAEJ2716 SENT "recommended" specification.

The CRC is calculated using the polynomial $x^4 + x^3 + x^2 + 1$, initialized to 0101.

By default, the checksum covers only the contents of the data nibbles (3-6 nibbles). By setting the SENT_SCN_CRC bit within EEPROM, the contents of the SCN are included within the CRC nibble which deviates from the SENT standard.

SENT Pause Pulse

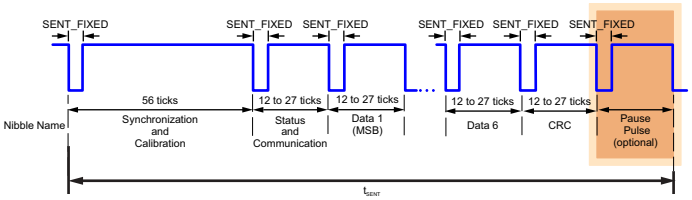

Figure 14: Pause Pulse in SENT message

The Pause Pulse is an optional addition to the SENT message frame, transmitted following the CRC nibble. It acts to "fill-in" the frame until the beginning of the next SENT transmission in order to have constant output rate. The inserted Pause Pulse is a minimum of 12 Ticks in length. The frame duration is always:

$$\text{Frame Duration (ticks)} = 56 + (N + 2) \times 27 + 12$$

where N is the number of data nibbles in the frame.

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Digital Output Mode Selection

Digital Output mode can be selected according to Table 13.

Table 13: Digital Output Modes Selection

dig_out_mode code	Output Type Description
0 (default)	PWM output with PWM level diagnostic reporting
1	PWM output with high impedance diagnostic reporting
2	SENT output (no pause pulse)
3	SENT output with pause pulse

Digital Output Driver Fall Time Selection

User is allowed to change the fall time of the output digital signal using the EEPROM parameter Out_drive_sel. User must ensure that "Sent_ftc_e_n" bit is set to 0 so that the changes to output driver apply.

Table 14: Digital Output Driver Selection

Out_drive_sel	Time from 90% to 10%, C_L = 100 pF (µs)
0 (default)	0.11
1	0.18
2	0.27
3	0.35
4	0.7
5	1.24
6	2.42
7	3.55

Broken Wire Detection

The A17700 contains circuitry to detect a condition when the ground or supply connection is disconnected. When the device is connected as per the recommended application circuit (Figure 2), the output will go to Vsat_diag_H in case of broken ground and Vsat_diag_L in case of broken VCC.

Diagnostic Features

The A17700 is equipped with diagnostic features enabling the host microcontroller to assess the operational status of sensor and device. These diagnostics can be activated through individual EEPROM bits and are summarized in Table 15.

DIAGNOSTIC REPORTING

When the device detects one of the fault given in Table 15 (except for Memory ECC fault), it will set a flag in a volatile register that can be cleared when the fault is removed through a register read (or reset) or after being sent out through the output protocol. This volatile register can be accessed through Manchester protocol. Reporting to device output depends on output protocol.

In analog output mode or in PWM mode with dig_out_mode = 1, the device output will hold the diagnostic state (high impedance) until the fault is removed or for a minimum of 4 ms to allow for appropriate detection.

High impedance state is factory configurable and could be adjusted on customer demand. Contact Allegro for further information.

Table 15: Output Diagnostics

Diagnostic Detection	Conditions	Analog Output State	PWM Output State dig_out_mode = 0 (Reporting Priority)	PWM Output State dig_out_mode = 1	SENT Data Nibble #4 and #5 SENT_data_cf = 1 dig_out_mode = 2 or 3	SENT SCN Nibble All SENT_data_cf options dig_out_mode = 2 or 3 SCN mode = 0 or 1
Memory ECC	Multi-bit EEPROM Error	High Impedance	High Impedance (1)	High Impedance	High Impedance	High Impedance
Undervoltage Condition	Undervoltage detection is enabled	High Impedance	1/2 carrier frequency, 20% DC (2)	High Impedance	xxxx xx1x	xx1x
Overvoltage Condition	Overvoltage detection is enabled	High Impedance	1/2 carrier frequency, 30% DC (3)	High Impedance	xxxx x1xx	xx1x
Overtemperature Condition	Overtemperature detection is enabled	High Impedance	1/2 carrier frequency, 40% DC (4)	High Impedance	xxxx 1xxx	xx1x
Undertemperature Condition	Undertemperature detection is enabled	High Impedance	1/2 carrier frequency, 60% DC (5)	High Impedance	xxx1 xxxx	xx1x
Input Signal Out of Range	Input Signal Out of Range is enabled	High Impedance	1/2 carrier frequency, 70% DC (6)	High Impedance	xx1x xxxx	xx1x
Short/Broken Bridge Connection	Bridge Short/Open detection is enabled	High Impedance	1/2 carrier frequency, 80% DC (7)	High Impedance	x1xx xxxx	xx1x
DAC interpolator error	DAC interpolator detection is enabled	High Impedance	Not applicable	Not applicable	Not applicable	Not applicable

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In PWM output mode with dig_out_mode = 0, the device output will hold the diagnostic state until the fault is removed or for a minimum of 5 ms to allow for appropriate detection. If PWM carrier frequency was set to 500 Hz or lower, the fault state will be maintained for a minimum of 16 ms to allow for diagnostic reporting for at least 2 cycles.

The reporting priority in PWM mode with dig_out_mode = 0 refers to the situation where multiple faults are detected at the same time. In this case, only the fault with highest priority (i.e., number 1 is the highest) will be reported.

In SENT output mode, depending on selected SENT configuration, the diagnostic flags can be reported through SCN bit 1, through the short serial message, or through the SENT data nibble 4 and 5 (sent_data_cfg = 1). When fault is removed, the error flag register is cleared when the flag is transmitted through SENT message. Each of these three SENT reporting modes have individual flag registers so that they can be cleared independently.

DIAGNOSTIC DESCRIPTION

Undervoltage Detection (UVD)

The A17700 contains circuitry to continuously check if the supply voltage drops below the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{UVD(R)} - V_{UVD(F)}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} drops below $V_{UVD(F)}$, and assuming this diagnostic is activated through the EEPROM bit, V_{OUT} is forced to a state as defined in Table 15. When V_{CC} returns above $V_{UVD(R)}$, V_{OUT} returns to its normal operating state after register read or reporting flags through the output modes, which will clear the error flag. If V_{CC} drops below the internal reset level, $V_{POR(F)}$, the output is forced to a high-impedance state. When V_{CC} returns above the rising reset level, $V_{POR(R)}$, the output responds with the UVD flag if enabled. To avoid setting UVD by incidental supply flickering, entering the UVD state is suppressed for approximately 20 µs.

Overvoltage Detection (OVD)

The A17700 contains circuitry to continuously check if the supply voltage rises above the specified limit. Hysteresis is designed into the circuit to prevent chattering around the threshold. This hysteresis is defined by $V_{OVD(R)} - V_{OVD(F)}$. As an example, initially V_{CC} and V_{OUT} are within the normal operating range. If V_{CC} rises above $V_{OVD(R)}$, and assuming this diagnostic is activated through the EEPROM bit, V_{OUT} is forced to a state as defined in Table 15. When V_{CC} returns below $V_{OVD(F)}$, V_{OUT} returns to its normal operating state after register read or reporting flags through the output modes, which will clear the error flag. To avoid setting OVD by incidental supply flickering, entering the OVD state is suppressed for approximately 20 µs.

In the case where OVD is disabled (EEPROM bit set to 0) but MANCH_TRIGGER_DIS = 00 or 01 and output is in digital mode, an OVD event will bring the device to communication mode and output will be forced to high impedance.

OVD threshold can be adjusted through EEPROM bit as per Table 16.

Table 16: OVD Level Config

OVD_CFG	OVD Rising Threshold (typ) (V)	OVD Falling Threshold (typ) (V)
0 (Default)	5.8	5.6
1	6.3	6.1
2	6.8	6.6
3	6.8	6.6

Overtemperature Detection (OTD)

The OTD flag is set if the temperature sensor output saturates high, which indicates the ambient temperature is greater than 165°C (default value). This assumes diagnostic reporting was activated through EEPROM bit. If this condition occurs, the OTD flag will be set and the device will go into a state as defined in Table 15. If the temperature is detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The OTD error can be detected every 8 ms and is never filtered.

Undertemperature Detection (UTD)

The UTD flag is set if the measured temperature is less than –70°C (default value). If this condition occurs, the UTD flag will be set and the device will go into a state as defined in Table 15. If the temperature is detected to recover, a read of the device register or reporting through the output modes will clear the error flag so normal operation can resume. The UTD error can be detected every 8 ms and is never filtered.

OTD and UTD thresholds can be adjusted through EEPROM bit as per Table 17.

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Table 17: OTD/UTD Level Config

OTD_CFG	Overtemperature Threshold (°C)	UTD_CFG	Undertemperature Threshold (°C)
0 (default)	165	0 (default)	–70
1	160	1	–65
2	155	2	–60
3	150	3	–55
4	145	4	–50
5	140	5	–45
6	135	6	–40
7	130	7	–35
8	125	8	–30
9	120	9	–25
10	115	10	–20
11	110	11	–15
12	105	12	–10
13	100	13	–5
14	95	14	0
15	90	15	5

Input Signal Out of Range Detection (OOR)

When activated through EEPROM, OOR continuously checks if the differential input signal is outside of the detectable range of the signal path. This can be detected as a saturation of the ADC and filters, which would indicate a front-end gain too large or a wrong offset from the input signal. If this condition occurs, the OOR flag will be set as defined in Table 15. If the saturation condition is removed, the error flag can be cleared by a read of the device register or through reporting to the applicable output protocol. To avoid setting OOR by incidental signal flickering, entering the OOR state is suppressed for approximately 32 µs.

Short/Broken Bridge Connection (BBC)

When activated through EEPROM, this diagnostic continuously monitors the V_P and V_N signals to ensure that they stay within operating range. Open connection of one of the four bridge pins or short of V_P or V_N to the bridge rails will set the BBC flag. The bridge supply is also monitored to ensure it stays within specified range, allowing detection of shorted VBRG pin. If any of these conditions occur, the BBC flag will be set as defined in Table 15. If the condition is removed, the error flag can be cleared by a read of the device register, or through reporting to the applicable output protocol. To avoid setting BBC by incidental signal flickering, entering the BBC state is suppressed for approximately 20 µs.

DAC Interpolator Error Detection (IED) – Analog Output Only

When device is in analog output mode and the DAC Interpolator error reporting is activated through EEPROM, this diagnostic continuously checks for consistency of the DAC Interpolator values. If the interpolated value does not stay within the expected range, the IED flag will be set and output will go to high impedance for a minimum duration of 4 ms. If the condition is removed, the error flag can be cleared by a read of the device register or when the output reporting timer expires.

Memory ECC (ECC)

Single error correction, double error detection ECC is implemented in EEPROM memory to protect its content. The whole EEPROM content is checked after power-up. Note that during each EEPROM check, any single-bit error in one 26-bit EEPROM word will be automatically corrected by the device and will thus allow a proper operation. When two-bit errors are detected in one 26-bit EEPROM word, Memory ECC diagnostic will be activated, resulting in a permanent high-impedance output state until device is reset.

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PROGRAMMING: MANCHESTER COMMUNICATION

The A17700 uses bidirectional Manchester communication protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Both input and output from the device are handled through the VOUT pin. Four commands are recognized by the A17700:

- Write Access Code
- Write to Volatile Memory
- Write to Non-Volatile Memory (EEPROM)
- Read

After a read command is sent, a Read Acknowledge is returned by the A17700.

The A17700 contains an internal charge-pump, removing the need for external programming pulses.

Table 18: Programming Characteristics

Parameter	Symbol	Description	Limits			
			Min.	Typ.	Max.	Units
Bit Rate	–	Communication Rate	4	–	100	kbps
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	2.8	–	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1.0	V

Table 19: Programming Levels

Parameter	Symbol	Description	Limits			
			Min.	Typ.	Max.	Units
Program Enable Voltage (High)	V_{PRGH}		$V_{OVD(R)}$ (max)	–	–	V
Program Enable Voltage (Low)	V_{PRGL}		–	–	$V_{OVD(F)}$ (min)	V
Output Enable Delay	t_e		–	25	–	µs
Program Time Delay	t_d	Delay between consecutive read/ writes during same Manchester event.	–	–	50	µs
Program Write Delay	t_w	Delay between end of write and time for device to store data in EEPROM.	–	20	–	ms
Bit Time Delay	t_b		–	1.5	–	t_{bit}
Low Level Trigger Pulse Hold Time	t_{hold}	PWM	2 × PWM period	–	–	cycles
		SENT	30	–	–	ticks
Access Code Time Out 1	t_{acc_1}		20	–	–	ms
Access Code	t_{acc_2}		1	–	–	ms

[1] For high Speed Manchester Communication, it is recommended to re-synchronize the sample rate at each period for accurate bit boundaries.

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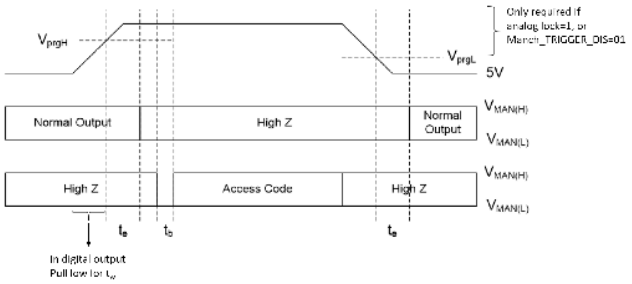

Figure 15: Access Code Write Timing Diagram

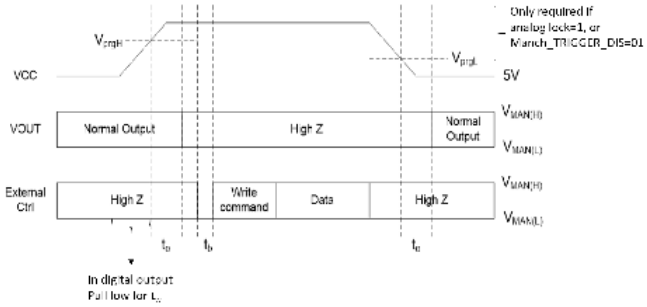

Figure 16: Write to Volatile Memory Timing Diagram

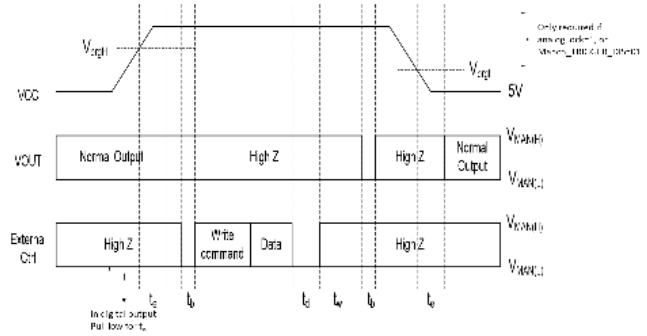

Figure 17: Write to Non-Volatile Memory (EEPROM) Timing Diagram

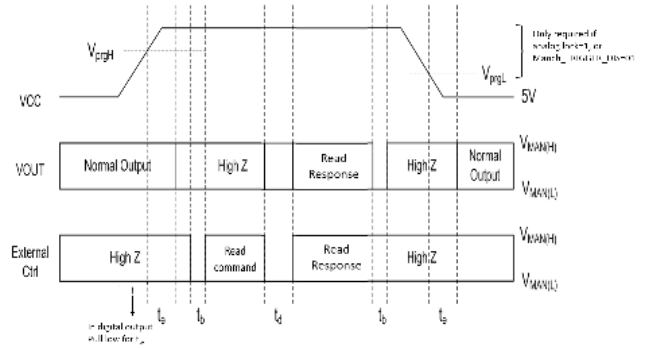

Figure 18: EEPROM/Volatile Memory Read Timing Diagram

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Entering Manchester Coding

To ensure that the same pin can be properly used for both output and Manchester communication, the device must be placed into a programming mode before beginning to send commands over Manchester. The method of activating the Manchester programming mode will be dependent upon selected output protocol and EEPROM options.

ENTERING MANCHESTER CODING WITH ANALOG OUTPUT MODE

In Analog output mode, the user must overdrive the output to enter into Manchester communication. Initiating Manchester communication can be done in two ways, depending on ANALOG_LOCK EEPROM bit:

1. If ANALOG_LOCK = 0 (default configuration), the correct customer access code must be sent within a time t_{acc_1} following power-up.
2. If ANALOG_LOCK = 1, the user must generate an OVD event ($V_{CC} > V_{PRGH}$) before sending the correct access code, before the timeout post power-up expires ($< t_{acc\_1}$). OVD event must be maintained during the first full transaction.

For any of the two above methods, if the timeout expires or an incorrect access code is sent, the device remains locked for communication until a power reset occurs. To ensure that analog noise is not interpreted as Manchester synchronization and the access code is sent correctly, the user should pull the output low during power-up for at least a time t_b.

The LSB of the 32-bit customer access code is used to disable the output and leave the device in communication mode until a reset occurs or until it is set back to 0. When the output is disabled, V_{CC} can be restored to a level below V_{PRGH} without altering the Manchester communication and thus until a reset occurs. If the output remains enabled, the user can still overdrive the output to send the Manchester commands. The start of any Manchester command should begin with holding the output for t_b to ensure reset of Manchester state machine.

To decrease the likelihood of analog noise being interpreted as Manchester during the operation of the device, the UNLOCK_CODE EEPROM bit is used to disable the internal Manchester controller when set to 1. This will prevent any unintended interruption from affecting the output signal of the device.

ENTERING MANCHESTER CODING WITH DIGITAL OUTPUT MODE

In Digital output mode, the two ways to enter programming mode are:

1. Generate an OVD event. This is caused by raising V_{CC} to above V_{PRGH} level. This event must be present during the entire Manchester Read/Write event. If not, the Manchester protocol is reset and transaction aborted.
2. Pull output low for a time specified by t_{hold}, which depends on the type of output protocol (SENT or PWM).

The MANCH_TRIGGER_DIS register is used to determine which trigger is used by the device to enter programming mode. Table 20 shows the register options.

Table 20: MANCH_TRIGGER_DIS Register Map

MANCH_ TRIGGER_DIS	OVD	Pull Output LOW	Description
11	Disabled	Disabled	Communication locked. Must be enabled via special procedure.
10	Disabled	Enabled	
01	Enabled	Disabled	
00 (default)	Enabled	Enabled	Communication is enabled by either option, NOT both.

If communication is locked (MANCH_TRIGGER_DIS = 11), the only way to enable communication mode is through the special procedure, which is as follows:

After POR, the following steps must be performed within a time defined by t_{acc_2}.

- Raise V_{CC} such that the device is in OVD condition.
- Trigger the communication mode through forcing LOW on the output pin.

Once Manchester communication has been initiated through a "pull output low" event, the customer access code must be sent within a defined time t_{acc_2} following communication trigger. If timeout expires or an invalid code is sent, the device goes back to normal PWM/SENT operations. The unlock procedure must be repeated (no reset is required).

In the same manner as for analog output, the LSB of the 32-bit

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customer access code is used to disable the output and leave the device in communication mode until a reset occurs or until it is set back to 0.

If Manchester communication is initiated with an OVD event, there is no timeout limit to send the access code as long as V_{CC} stays above V_{PRGH}. When the device is in communication mode (LSB of the 32-bit customer access code is set to 1), there is no need to generate the OVD event anymore; the PWM/SENT Output will be disabled until a reset occurs or until the LSB of customer access code is set back to 1.

Manchester Interface Message Structure

The general format of a command message frame is shown in Figure 19. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary. The time interval for the bit boundary is determined by the baud rate initiated by the external controller. The A17700 read acknowledge is transmitted at the same rate as the command message frame. For high speed Manchester read, it is recommended to resynchronize the sample rate at each period for accurate bit boundaries. The bits composing a frame are described in Table 21.

For a Write Access command frame, the data consists of 32 bits. For a Read Request frame, the data bits are omitted. For a Read Acknowledge or Write frame the data bits are defined as shown in Figure 19, where bit 0 is the LSB.

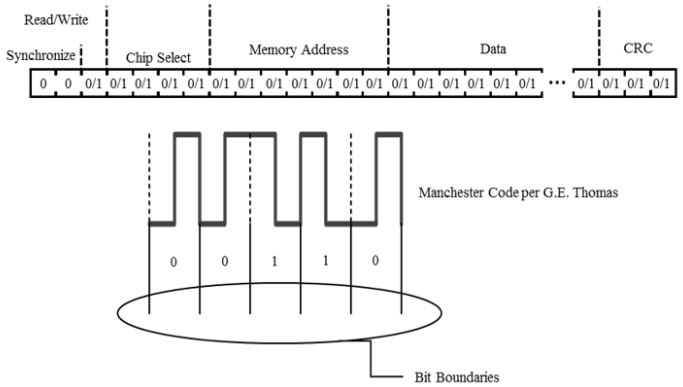

Figure 19: Manchester Bit Stream Definition

Table 21: Manchester Bit Definition

Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
4	Chip Select	0-15	Up to 4 dies connected in parallel (Device ID set in EEPROM): XXX1 = device comm. addr. 0 XX1X = device comm. addr. 1 X1XX = device comm. addr. 2 1XXX = device comm. addr. 3 0000, 1111 = Broadcast
7	Address	0/1	[Read/Write] Serial address (volatile memory or EEPROM)
32	Data	0/1	Write, 32 data bits Write access, 32 bits data
3	CRC	0/1	Bits to check the validity of frame

CRC

The Manchester communication implements a cyclical redundancy check (CRC) for data-bit error checking (synchronization bits are ignored). The CRC algorithm is based on the following polynomial and the calculation is represented graphically in the following figure. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized as 111.

$$CRC = x^3 + x + 1$$

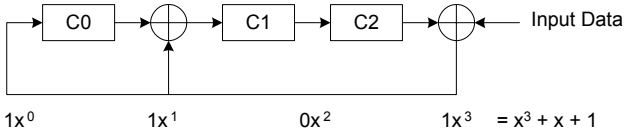

Figure 20: Visual Representation of CRC Implementation

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Device Access

The device contains nonvolatile (EEPROM) and volatile registers that are only accessible by sending an access code within 20 ms after power-on (analog output mode) or within t_{acc_2} or post OVD event (digital output mode). The code is constant, and its value is provided below. For software convenience, the code is provided as a 7-bit "address" and 32-bit "data" field in order to mimic a normal write command format. Note that the LSB also controls output enable/disable bit.

Table 22: Access Code for Manchester Communications

Name	Serial Interface Format	
	Address (Hex)	Data (Hex)
Customer	0x46	0x3A25BAC8

Shadow Registers

Shadow registers are volatile registers that are the exact representation of the EEPROM and are used by the device to read the EEPROM content. After each repower, or after each EEPROM write operation, the EEPROM content is loaded to the shadow registers, ensuring the same data are present to both registers. Shadow registers are accessible to the user for read and write using the same Manchester communication and access code as for EEPROM (see EEPROM map for shadow register address). A write operation to these registers does not require any Program write delay (t_w) and is therefore much faster that EEPROM write. Additionally, many read/write operations can be performed, and a simple power reset cycle erases the register and reloads the EEPROM content, making this feature suitable for test purposes.

Device EEPROM and Register Access Lock

There are 3 different lock modes available in the A17700: EELOCK, WRLOCK, and FLOCK (Table 23). Each of these are separate from access lock which requires a customer unlock code and are valid with any output mode (analog/digital).

EELOCK locks the EEPROM from external write access while still allowing writes to shadow and volatile registers. The entirety of memory can still be read in this mode allowing for a level of customer lock while maintaining debug support.

WRLOCK prevents any write to EEPROM or registers. Factory read support is maintained. Reads from all locations are still allowed, using OVD threshold on VCC for Manchester enable. This is not recommended for any output mode.

The FLOCK mode locks out both reads and writes to EEPROM and all registers. This is the highest level of security but will prevent any access by either customer or factory, removing available support options from the factory.

NOTE: When any of the EEPROM lock options are set, non-destructive factory debug support is limited.

Table 23: Serial Communication Lockout Modes

EEPROM_lock[3:0]	Lock Mode	Description
4'b0000	Default	No additional lock. EEPROM and register access are protected through access codes.
4'b0011	EELOCK	EEPROM Lock: Prevents writes to EEPROM but all volatile registers including shadow can be written. All registers and EEPROM can be read normally.
4'b0110	WRLOCK	Write Lock: Prevents writing anything to either EEPROM or registers. Factory debug support is still available. All registers and EEPROM can still be read but need OVD threshold during communication.
4'b1100	FLOCK	Full Lock: Prevents writing and reading to any register in the device.

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EEPROM MAP

EEPROM Address	Shadow Address	Parameter Name	Description	Register Structure	Size	MSB	LSB
0x0C	0x2C	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a40_lsb	Pressure Poly (4,4) compensation: coefficient a40 bits 7:0	Signed, 2-complement	8	23	16
		press_coeff_a00	Pressure Poly (4,4) compensation: coefficient a00 bits 15:0	Signed, 2-complement	16	15	0
0x0D	0x2D	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a40_msb	Pressure Poly (4,4) compensation: coefficient a40 bits 15:8	Signed, 2-complement	8	23	16
		press_coeff_a10	Pressure Poly (4,4) compensation: coefficient a10 bits 15:0	Signed, 2-complement	16	15	0
0x0E	0x2E	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a31_lsb	Pressure Poly (4,4) compensation: coefficient a31 bits 7:0	Signed, 2-complement	8	23	16
		press_coeff_a01	Pressure Poly (4,4) compensation: coefficient a01 bits 15:0	Signed, 2-complement	16	15	0
0x0F	0x2F	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a31_msb	Pressure Poly (4,4) compensation: coefficient a31 bits 15:8	Signed, 2-complement	8	23	16
		press_coeff_a20	Pressure Poly (4,4) compensation: coefficient a20 bits 15:0	Signed, 2-complement	16	15	0
0x10	0x30	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a22_lsb	Pressure Poly (4,4) compensation: coefficient a22 bits 7:0	Signed, 2-complement	8	23	16
		press_coeff_a11	Pressure Poly (4,4) compensation: coefficient a11 bits 15:0	Signed, 2-complement	16	15	0
0x11	0x31	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a22_msb	Pressure Poly (4,4) compensation: coefficient a22 bits 15:8	Signed, 2-complement	8	23	16
		press_coeff_a02	Pressure Poly (4,4) compensation: coefficient a02 bits 15:0	Signed, 2-complement	16	15	0
0x12	0x32	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a13_lsb	Pressure Poly (4,4) compensation: coefficient a13 bits 7:0	Signed, 2-complement	8	23	16
		press_coeff_a30	Pressure Poly (4,4) compensation: coefficient a30 bits 15:0	Signed, 2-complement	16	15	0
0x13	0x33	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a13_msb	Pressure Poly (4,4) compensation: coefficient a13 bits 15:8	Signed, 2-complement	8	23	16
		press_coeff_a21	Pressure Poly (4,4) compensation: coefficient a21 bits 15:0	Signed, 2-complement	16	15	0
0x14	0x34	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a04_lsb	Pressure Poly (4,4) compensation: coefficient a04 bits 7:0	Signed, 2-complement	8	23	16
		press_coeff_a12	Pressure Poly (4,4) compensation: coefficient a12 bits 15:0	Signed, 2-complement	16	15	0
0x15	0x35	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	2	25	24
		press_coeff_a04_msb	Pressure Poly (4,4) compensation: coefficient a04 bits 15:8	Signed, 2-complement	8	23	16
		press_coeff_a03	Pressure Poly (4,4) compensation: coefficient a03 bits 15:0	Signed, 2-complement	16	15	0

Continued on next page...

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EEPROM MAP (continued)

EEPROM Address	Shadow Address	Parameter Name	Description	Register Structure	Size	MSB	LSB
0x16	0x36	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	1	25	25
		Clamp High	Clamp_high settings	Unsigned, Linear; see Table 7	5	24	20
		Clamp Low	Clamp_low settings	Unsigned, Linear; See Table 7	5	19	15
		Offset_coarse	Front end coarse offset	Signed, 2-complement; see Table 4	6	14	9
		Gain2	Front end coarse sensitivity – Gain2	Unsigned, Linear; see Table 3	4	8	5
		Gain1	Front end coarse sensitivity – Gain1	Unsigned, Linear; see Table 2	2	4	3
		Bandwidth	Bandwidth selection	See Table 1 (BW selection)	3	2	0
0x17	0x37	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	6	25	20
		Lbist_Start-Up_disable	Disables LBIST test at startup. Set to 1 in application.	–	1	19	19
		EEPROM lock	Lock access to EEPROM and or volatile register	See Table 23 (Serial com lock)	4	18	15
		SCN_MODE	SENT status and Communication Nibble modes	See Table 9 (Scn_modes)	2	14	13
		Pol_Bit	Front end Polarity bit	–	1	12	12
		Open_drain_enable	Activates open drain output in digital mode (default: push/pull)	–	1	11	11
		Dig_out_mode	Digital Output Selection mode	See Table 13 (Dig out mode sel)	2	10	9
		Device ID	Device ID used for Manchester communication; see Chip Select in Table 21	–	2	8	7
		Sent_ftc_e_n	Disables digital output fall time control (Out_drive_sel)	–	1	6	6
		Sent_data_cfg	SENT message data type	See Table 12 (Sent Data Cfg)	2	5	4
		Out_freq_rate	Configures PWM output carrier frequency or SENT tick time	See Table 8 (SENT/PWM rates)	3	3	1
		SENT_SCN_CRC	Includes SCN to the CRC calculation	–	1	0	0
0x18	0x38	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		UNLOCK_CODE	Must be set to 0. Setting to 1 prevents all Manchester communications (Analog output mode only).	–	1	25	25
		–	Unused Memory location	–	7	24	18
		DAC interp disable	Disables DAC interpolation in analog output. Set to 0 in application.	–	1	17	17
		Reserved	Allegro_reserved_bit. Must be set to 0.	–	1	16	16
		DAC output cap driver	Value 0 shall be used for OUT decoupling cap of 10 to 150 nF, Value 2 shall be used for OUT decoupling cap of 80 to 330 nF, Other codes are Allegro reserved.	–	2	15	14
		ANALOG_LOCK	In Analog output, requires OVD event for Manchester communication	–	1	13	13
		Reserved	Allegro_reserved_bit. Must be set to 0.	–	1	12	12
		MANCH_TRIGGER_DIS	Configures Manchester communication enable mode in digital output.	See Table 20 (Manch_trigger_dis)	2	11	10
		Out_drive_sel	Configures output slew rate in digital mode.	See Table 14 (Dig Out driver sel)	3	9	7
		IED	Enables DAC Interpolator error reporting (analog output only) as defined in Table 15.	–	1	6	6
		BBC	Enables Short/Broken Bridge reporting as defined in Table 15.	–	1	5	5
		OOR	Enables Input signal out of range reporting as defined in Table 15.	–	1	4	4
		OTD	Enables Overtemperature reporting as defined in Table 15.	–	1	3	3
		UTD	Enables Undertemperature reporting as defined in Table 15.	–	1	2	2
		OVD	Enables Overvoltage reporting as defined in Table 15.	–	1	1	1
		UVD	Enables Undervoltage reporting as defined in Table 15.	–	1	0	0

Continued on next page...

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EEPROM MAP (continued)

EEPROM Address	Shadow Address	Parameter Name	Description	Register Structure	Size	MSB	LSB
0x19	0x39	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	16	25	10
		OTD_CFG	Configures Detection Threshold for overtemperature Diagnostic	See Table 17 (OTD/UTD config)	4	9	6
		UTD_CFG	Configures Detection Threshold for undertemperature Diagnostic	See Table 17 (OTD/UTD config)	4	5	2
		OVD_CFG	Configures Detection Threshold for overvoltage Diagnostic	See Table 16 (OVD config)	2	1	0
0x1A to 0x1D	–	–	Unused Memory locations	–	–	–	–
0x1E	0x3E	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		–	Unused Memory location	–	25	25	1
		BBC_act	Activates internal signals for Bridge diagnostics	–	1	0	0
0x1F	0x3F	EEPROM ECC	EEPROM ECC bits. Should be all 0 on write sequence.	–	6	31	26
		Customer scratch	Available EEPROM bits for customer use	–	26	25	0

VOLATILE REGISTERS MAP

Volatile Register Address	Parameter Name	Description	Register Structure	Size	MSB	LSB
0x4d	Err-status	DAC interpolator error (Analog output mode only).	Read/Write	1	6	6
		Bridge error	Read/Write	1	5	5
		Input signal out of range error	Read/Write	1	4	4
		Over temperature error	Read/Write	1	3	3
		Under temperature error	Read/Write	1	2	2
		Overvoltage error	Read/Write	1	1	1
		Undervoltage error	Read/Write	1	0	0
0x46	Access-code	Access code for Manchester communication. 0x3A25BAC8 → access code output still enabled 0x3A25BAC9 → access code output disabled	Read/Write	32	31	0
0x52	ADC_comp_reg	Digital pressure data before Poly(4,4) compensation	Signed, Read Only	16	15	0
0x5b	Press_comp_clamp	Digital pressure data post compensation, post clamp	Signed, Read Only	12	11	0
0x62	TT-comp_reg	Digital Internal temperature data	Signed, Read Only	12	11	0

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POWER DERATING

The device must operate below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die) through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A = 25°C, V_{CC} = 5 V, I_{CC} [1] = 10 mA, V_{OUT} = 5 V, I_{OUT} = 1.1 mA, and $R_{\theta JA}$ = 136°C/W, then:

$$P_D = V_{CC} \times I_{CC} + V_{OUT} \times I_{OUT} = 55.5 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 55.5 \text{ mW} \times 136°C/W = 7.5°C$$

$$T_J = T_A + \Delta T = 25°C + 7.5°C = 32.5°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)} \times I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A = 150°C, package ES.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 136°C/W, $T_{J(max)}$ = 165°C, $V_{CC(max)}$ = 5.5 V, $I_{CC(max)}$ [1] = 10 mA, V_{OUT} = 5 V, and I_{OUT} = 1.1 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 136°C/W = 110 \text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div (I_{CC(max)} + I_{OUT})$$
$$= 110 \text{ mW} \div (10 + 1.1) \text{ mA}$$
$$= 9.9 \text{ V}$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then a reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these condition.

[1] A bridge current consumption of 2.2 mA is also included in the given I_{CC} value.

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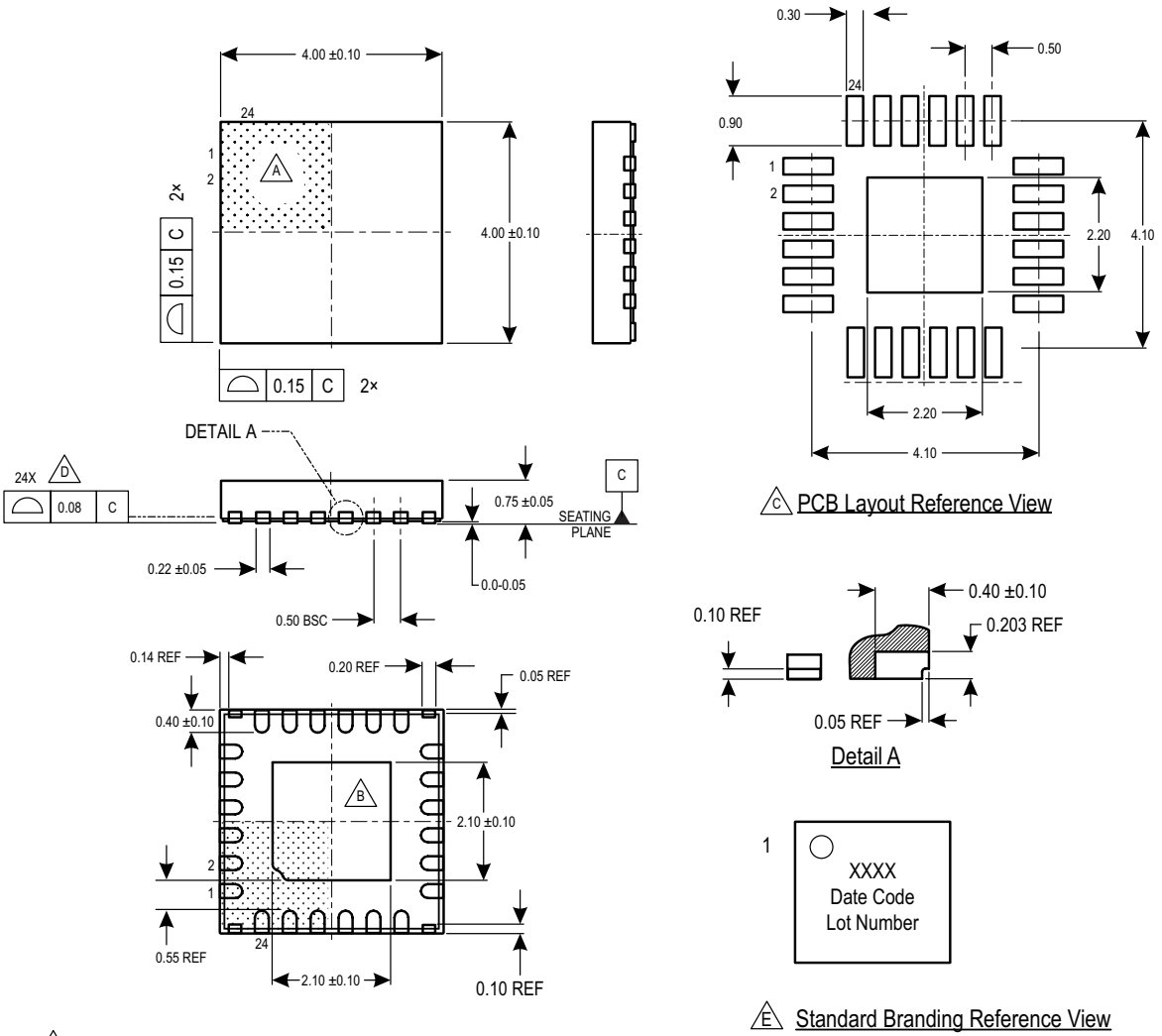
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 6 or JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Line 1: Part Number
Line 2: 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 21: Package ES, 24-pin wettable flank QFN with exposed thermal pad

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Revision History

Number	Date	Description
–	December 4, 2020	Initial release
1	November 30, 2022	Updated package drawing (page 30)

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