



# 74ACQ240, 74ACTQ240 Quiet Series™ Octal Buffer/Line Driver with 3-STATE Outputs

## Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inverting 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24mA
- Faster prop delays than the standard ACT240

## General Description

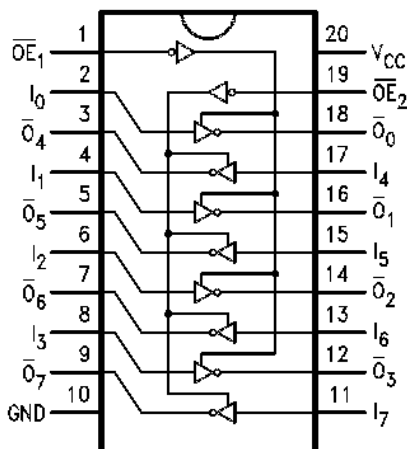
The ACQ/ACTQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes Fairchild's Quiet Series™ technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

## Ordering Information

Order Number	Package Number	Package Description
74ACQ240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACQ240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ240SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACTQ240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ240QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

## Connection Diagram

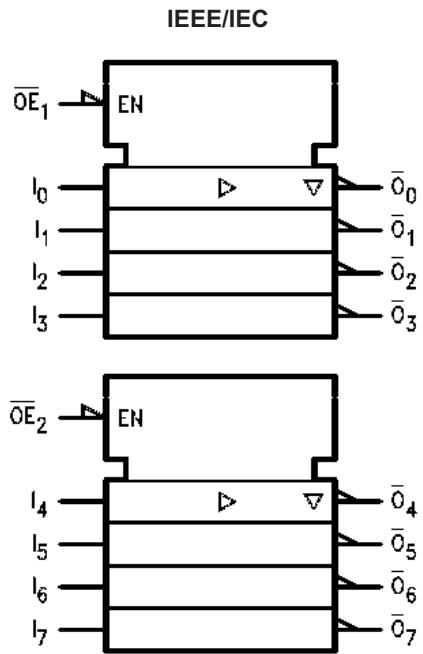


## Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

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### Logic Symbol



### Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_n$	Pins 12, 14, 16, 18
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_n$	Pins 3, 5, 7, 9
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
	DC Latch-Up Source or Sink Current	$\pm 300mA$
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage ACQ ACTQ	2.0V to 6.0V 4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACQ Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.0V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACTQ Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for ACQ

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OH</sub> = -12mA		2.56	2.46			
		4.5		I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5		I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1		V	
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> : I <sub>OL</sub> = 12mA		0.36	0.44			
		4.5		I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5		I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44		
I <sub>IN</sub> <sup>(3)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA	
I <sub>OLD</sub>	Minimum Dynamic	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>	Output Current <sup>(2)</sup>	5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(3)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA	
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>I</sub> = V <sub>CC</sub> , GND; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.25	±2.5		μA	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(4)</sup>	1.1	1.5			V	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(4)</sup>	-0.6	-1.2			V	
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	<sup>(5)</sup>	3.1	3.5			V	
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	<sup>(5)</sup>	1.9	1.5			V	

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
- Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.
- Max number of data inputs (n) switching. (n - 1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1MHz.

## DC Electrical Characteristics for ACTQ

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V	
		5.5		1.5	2.0	2.0			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V	
		5.5		1.5	0.8	0.8			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V	
		5.5		5.49	5.4	5.4			
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OH</sub> = -24mA			3.86	3.76		
		5.5	I <sub>OH</sub> = -24mA <sup>(6)</sup>			4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V	
		5.5		0.001	0.1	0.1			
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> ; I <sub>OL</sub> = 24mA			0.36	0.44		
		5.5	I <sub>OL</sub> = 24mA <sup>(6)</sup>			0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA	
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.25	±2.5		μA	
I <sub>CC</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA	
I <sub>OLD</sub>	Minimum Dynamic	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>	Output Current <sup>(7)</sup>	5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(8)</sup>	1.1	1.5			V	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	Figures 1 & 2 <sup>(8)</sup>	-0.6	-1.2			V	
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	5.0	<sup>(9)</sup>	1.9	2.2			V	
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage	5.0	<sup>(9)</sup>	1.2	0.8			V	

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.
- Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 3V. One Data Input @ V<sub>IN</sub> = GND.
- Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

**AC Electrical Characteristics for ACQ**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(10)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t <sub>PHL</sub>	Propagation Delay, Data to Output	3.3	2.0	7.0	10.0	2.0	10.5	ns
t <sub>PLH</sub>		5.0	1.5	5.0	6.5	1.5	7.0	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	8.0	12.0	2.5	12.5	ns
t <sub>PZH</sub>		5.0	1.5	5.5	8.0	1.5	8.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	1.0	8.5	13.5	1.0	14.0	ns
t <sub>PLZ</sub>		5.0	1.0	6.0	9.0	1.0	9.5	
t <sub>OSSL</sub>	Output to Output Skew, Data to Output <sup>(11)</sup>	3.3		1.0	1.5		1.5	ns
t <sub>OSLH</sub>		5.0		0.5	1.0		1.0	

**Notes:**

10. Voltage range 5.0 is 5.0V ± 0.5V. Voltage range 3.3 is 3.3 ± 0.3V.
11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**AC Electrical Characteristics for ACTQ**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(12)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
t <sub>PHL</sub>	Propagation Delay, Data to Output	5.0	1.5	5.5	7.0	1.5	7.5	ns
t <sub>PLH</sub>								
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	5.0	1.5	6.5	8.5	1.5	9.0	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	5.0	1.0	7.0	9.5	1.0	10.0	ns
t <sub>OSSL</sub>	Output to Output Skew, Data to Output <sup>(13)</sup>	5.0		0.5	1.0		1.0	ns
t <sub>OSLH</sub>								

**Notes:**

12. Voltage range 5.0 is 5.0V ± 0.5V
13. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

**Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN	4.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 5.0V	70	pF

## FACT Noise Characteristics

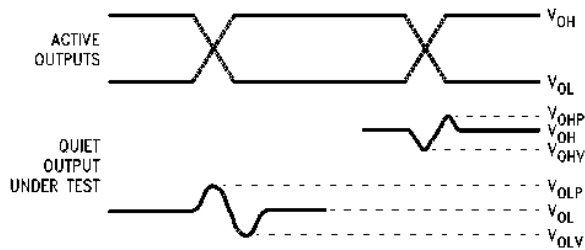
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

- Hewlett Packard Model 8180A Word Generator
- PC-163A Test Fixture
- Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



### Notes:

14.  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference.
15. Input pulses have the following characteristics:  
 $f = 1\text{MHz}$ ,  $t_r = 3\text{ns}$ ,  $t_f = 3\text{ns}$ , skew < 150ps.

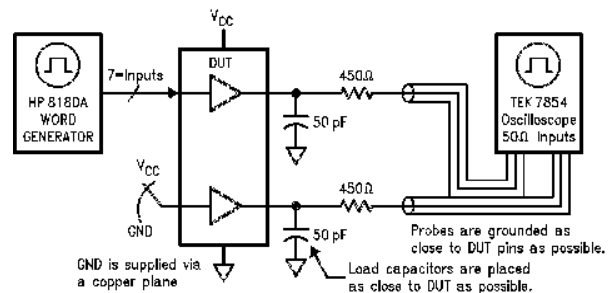
**Figure 1. Quiet Output Noise Voltage Waveforms**

### $V_{OLP}/V_{OLV}$ and $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable. Measure  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

### $V_{ILD}$ and $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.



**Figure 2. Simultaneous Switching Test Circuit**

### Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

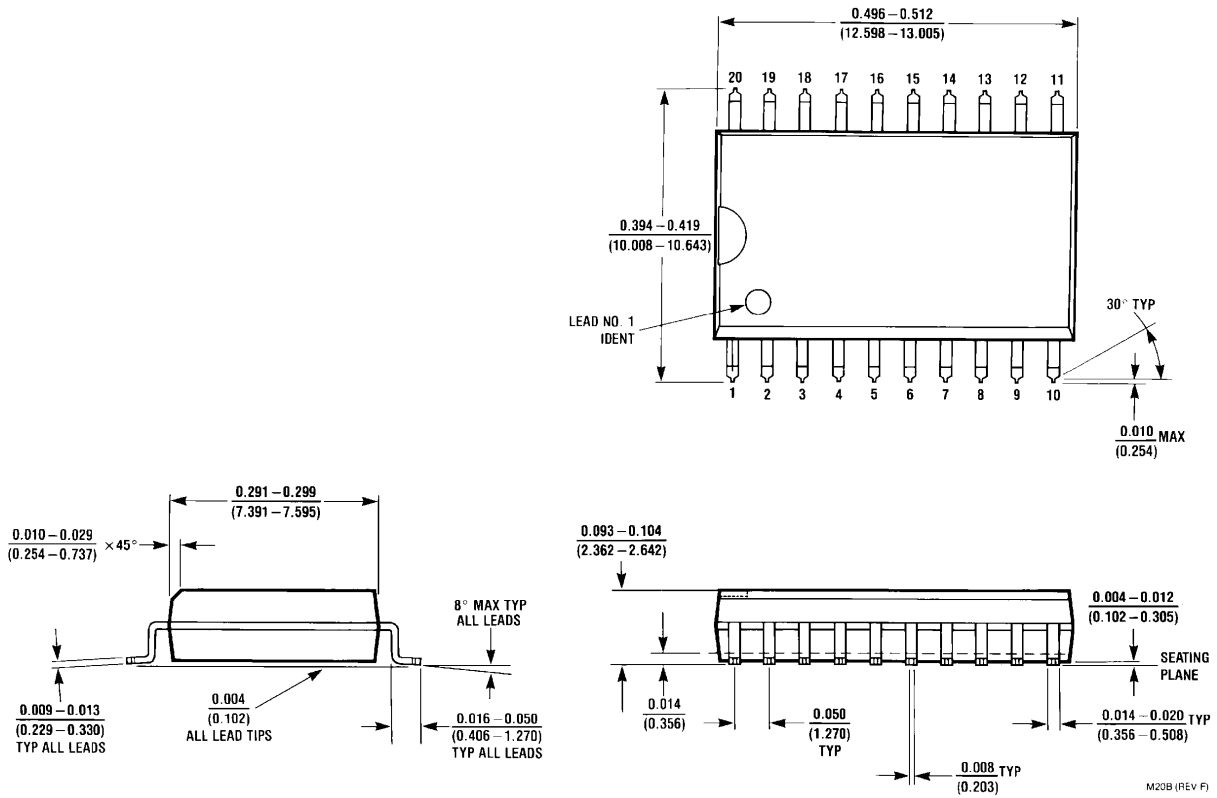
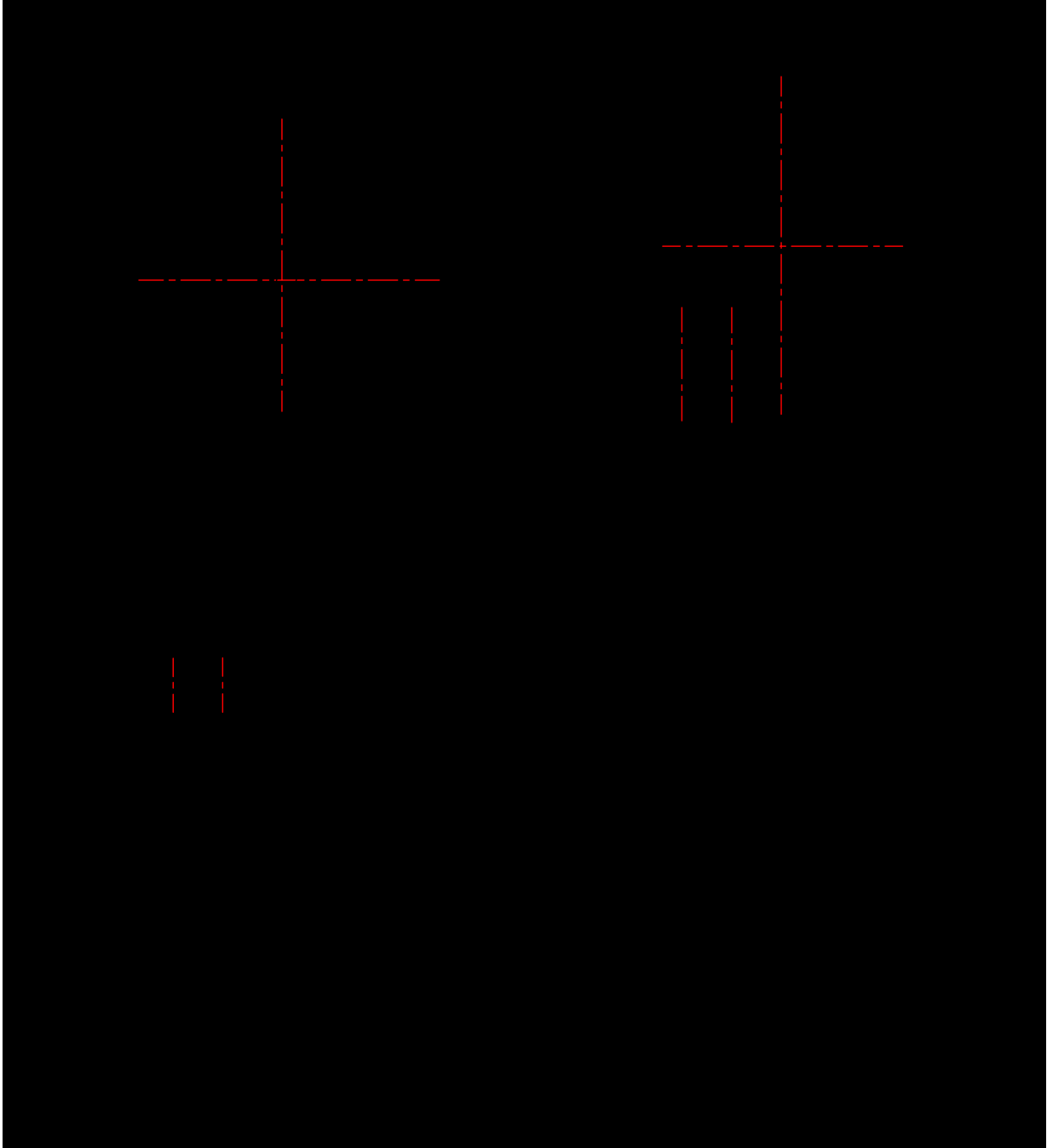


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



**Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**





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