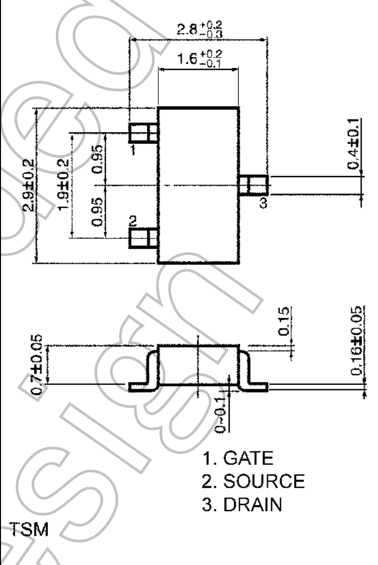
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K01T

High Speed Switching Applications

Unit: mm

- Small Package
- Low on Resistance: R_{on} = 120 mΩ (max) (@V_{GS} = 4 V)
  : R_{on} = 150 mΩ (max) (@V_{GS} = 2.5 V)
- Low Gate Threshold Voltage: V_{th} = 0.6 to 1.1 V
  (@V_{DS} = 3 V, I_D = 0.1 mA)



JEDEC	―
JEITA	―
TOSHIBA	2-3S1A

Weight: 10 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	3.2	A
	Pulse	I_{DP} (Note 2)	6.4	
Drain power dissipation (Ta = 25°C)		P_D (Note 1)	1250	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu pad: 645 mm^2, t = 10 s)

Note 2: The pulse width limited by max channel temperature.

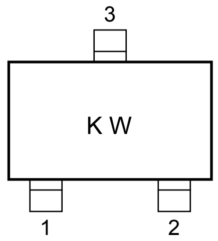
Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

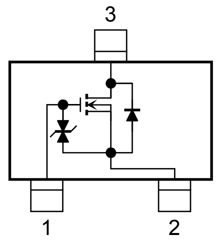
The Channel-to-Ambient thermal resistance $R_{th\ (ch\text{-}a)}$ and the drain power dissipation P_D vary according to the board material, board area, board thickness and pad area, and are also affected by the environment in which the product is used. When using this device, please take heat dissipation fully into account.

Start of commercial production
2000-04

Marking



Equivalent Circuit



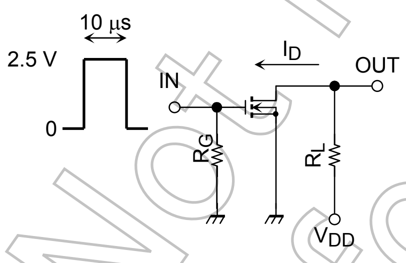
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	30	—	—	V
Drain Cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.6	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 1.6 A (Note3)	2.6	5.2	—	S
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 1.6 A, V_{GS} = 4 V (Note3)	—	85	120	mΩ
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 1.3 A, V_{GS} = 2.5 V (Note3)	—	115	150	mΩ
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	152	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	41	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	102	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 15 V, I_D = 0.5 A V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω	—	45	—	nS
	Turn-off time	t_{off}		—	69	—	

Note3: Pulse test

Switching Time Test Circuit

(a) Test circuit



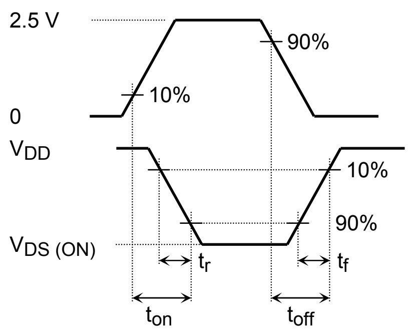
V_{DD} = 15 V
R_G = 4.7 Ω
D.U.≤ 1%
V_{IN}: t_r, t_f < 5 ns
COMMON SOURCE
Ta = 25°C

(b) V_{IN}

V_{GS}

(c) V_{OUT}

V_{DS}

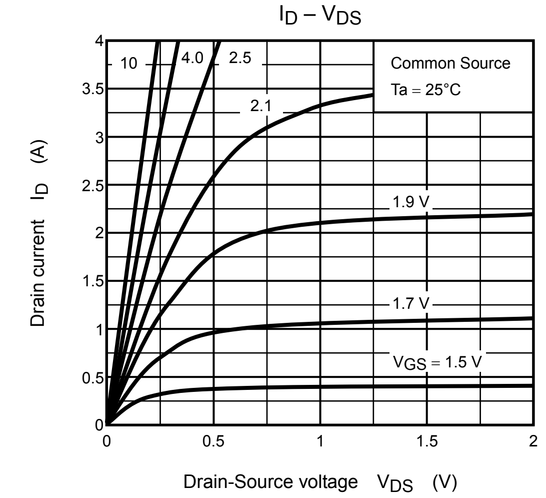


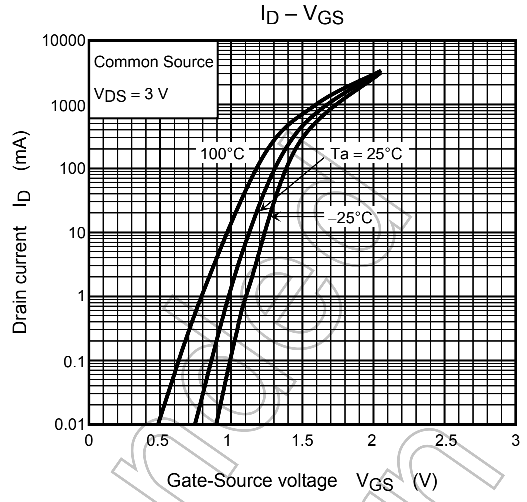
Precaution

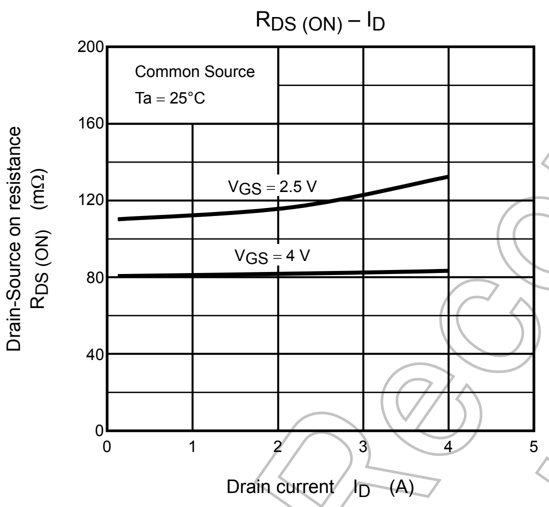
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}.

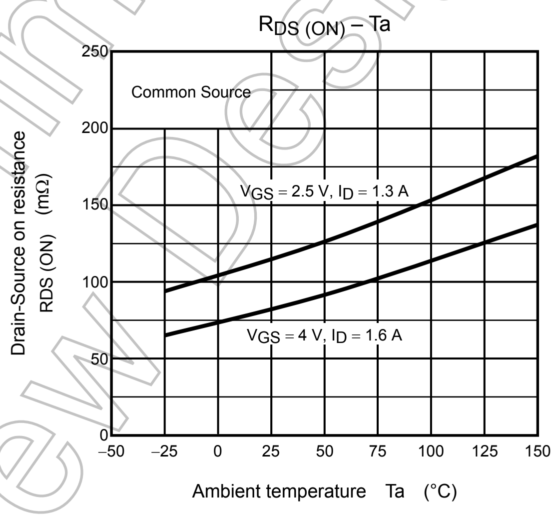
(relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

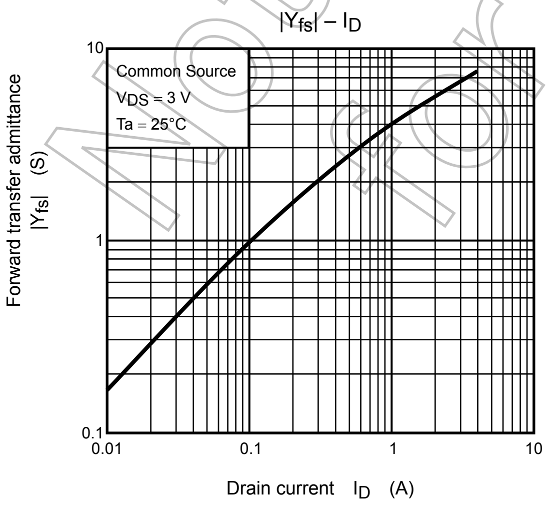
Please take this into consideration for using the device.

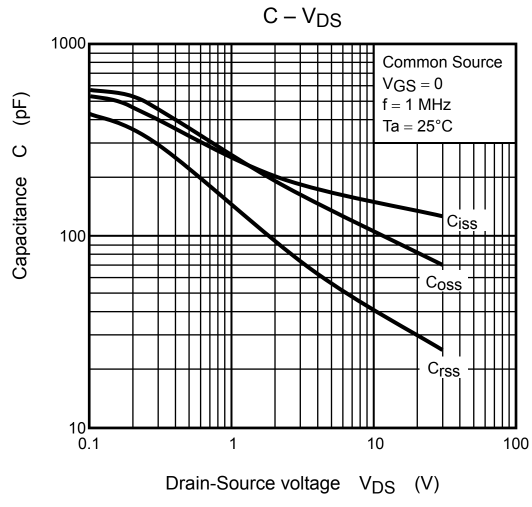

ID – VDS
Common Source
Ta = 25°C
10
4.0
2.5
2.1
1.9 V
1.7 V
VGS = 1.5 V
Drain current ID (A)
Drain-Source voltage VDS (V)

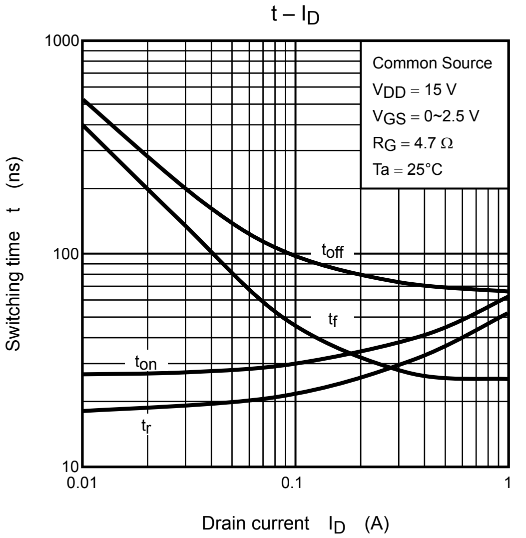

ID – VGS
Common Source
VDS = 3 V
100°C
Ta = 25°C
−25°C
Drain current ID (mA)
Gate-Source voltage VGS (V)

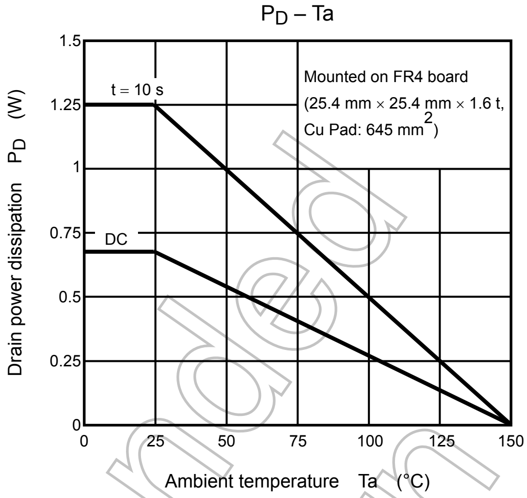

RDS (ON) – ID
Common Source
Ta = 25°C
VGS = 2.5 V
VGS = 4 V
Drain-Source on resistance RDS (ON) (mΩ)
Drain current ID (A)

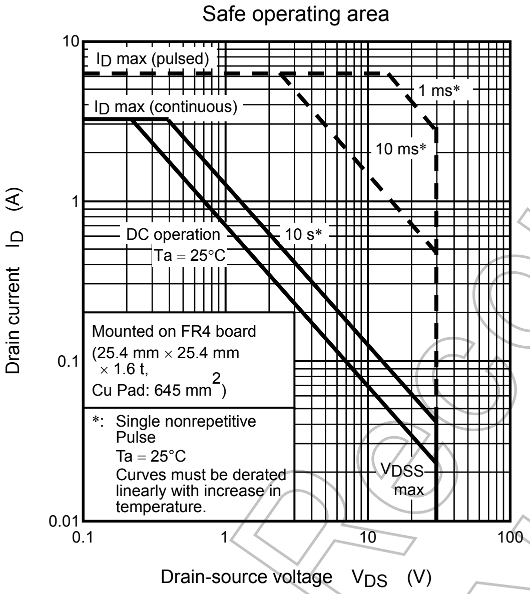

RDS (ON) – Ta
Common Source
VGS = 2.5 V, ID = 1.3 A
VGS = 4 V, ID = 1.6 A
Drain-Source on resistance RDS (ON) (mΩ)
Ambient temperature Ta (°C)

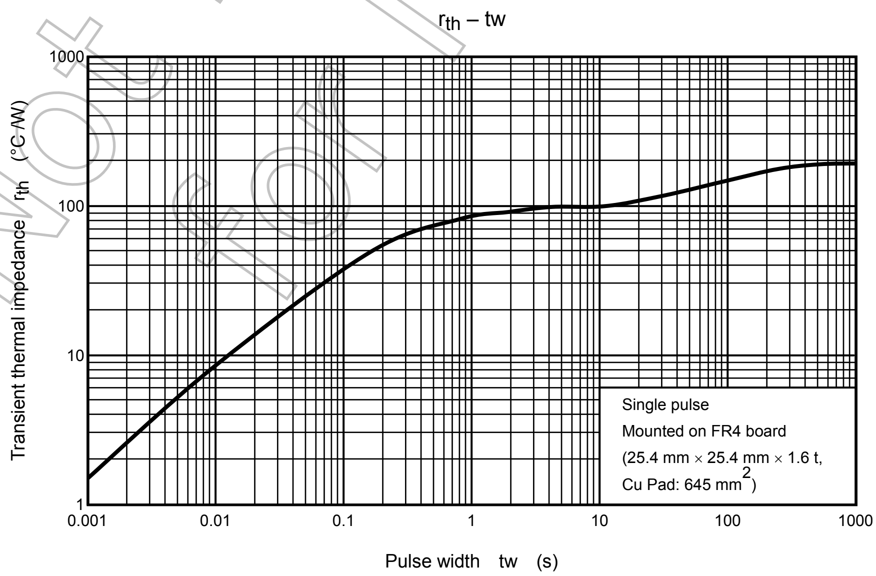

|Yfs| – ID
Common Source
VDS = 3 V
Ta = 25°C
Forward transfer admittance |Yfs| (S)
Drain current ID (A)


C – VDS
Common Source
VGS = 0
f = 1 MHz
Ta = 25°C
Ciss
Coss
Crss
Capacitance C (pF)
Drain-Source voltage VDS (V)


t – ID
Common Source
VDD = 15 V
VGS = 0~2.5 V
RG = 4.7 Ω
Ta = 25°C
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (A)
1000
100
10
0.01
0.1
1


PD – Ta
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu Pad: 645 mm2)
t = 10 s
DC
Drain power dissipation PD (W)
Ambient temperature Ta (°C)
1.5
1.25
1
0.75
0.5
0.25
0
25
50
75
100
125
150


Safe operating area
ID max (pulsed)
ID max (continuous)
1 ms*
10 ms*
DC operation
Ta = 25°C
10 s*
Mounted on FR4 board
(25.4 mm × 25.4 mm
× 1.6 t,
Cu Pad: 645 mm2)
*: Single nonrepetitive
Pulse
Ta = 25°C
Curves must be derated
linearly with increase in
temperature.
VDSS
max
Drain current ID (A)
Drain-source voltage VDS (V)
10
1
0.1
0.01
100


rth – tw
Single pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t,
Cu Pad: 645 mm2)
Transient thermal impedance rth (°C/W)
Pulse width tw (s)
1000
100
10
1
0.001
0.01
0.1
10

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