STK541UC62A-E

Advance Information

Intelligent Power Module (IPM) 600 V, 10 A

The STK541UC62A−E is a fully−integrated inverter power stage consisting of a high−voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless−DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3−phase bridge.

The power stage has a full range of protection functions including cross−conduction protection, external shutdown and under−voltage lockout functions. Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Features

- Three−Phase 10 A / 600 V IGBT Module With Integrated Drivers
- Typical Values (Upper Side at 10 A): V_{CE}(sat) = 1.4 V, V_F = 1.3 V
- 62.0 mm x 21.8 mm Single In−line Package
- Cross−Conduction Protection
- Integrated Bootstrap Diodes and Resistors
- These Devices are Pb−Free and are RoHS Compliant

Certification

- UL1557 (File Number: E339285)

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Heat Pumps, Home Appliances

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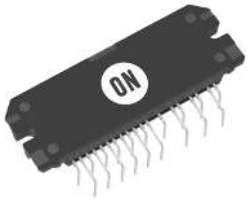


SIP23 62x21.8
CASE 127VB

MARKING DIAGRAM

STK541UC62A = Specific Device Code
A = Year
B = Month
C = Production Plant
D = Ordering Number
Device Marking in on Package Underside

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 13 of this data sheet.

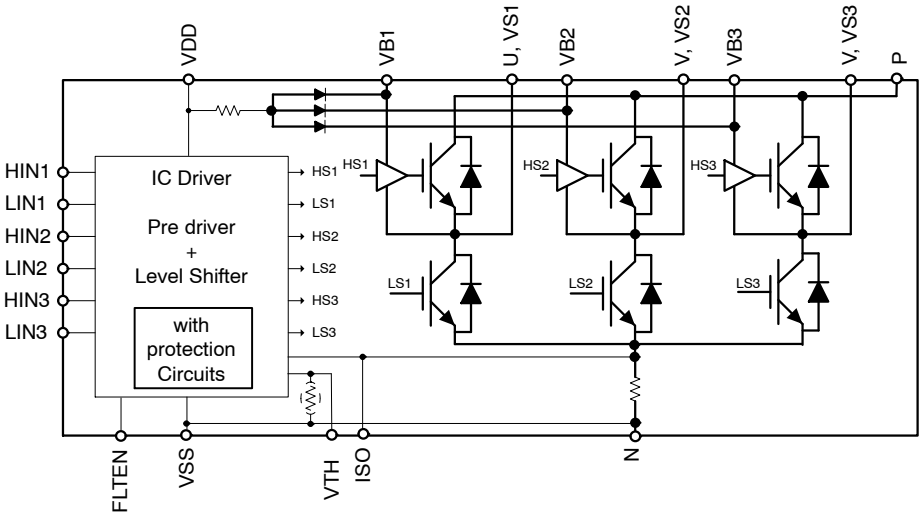


Figure 1. Functional Diagram

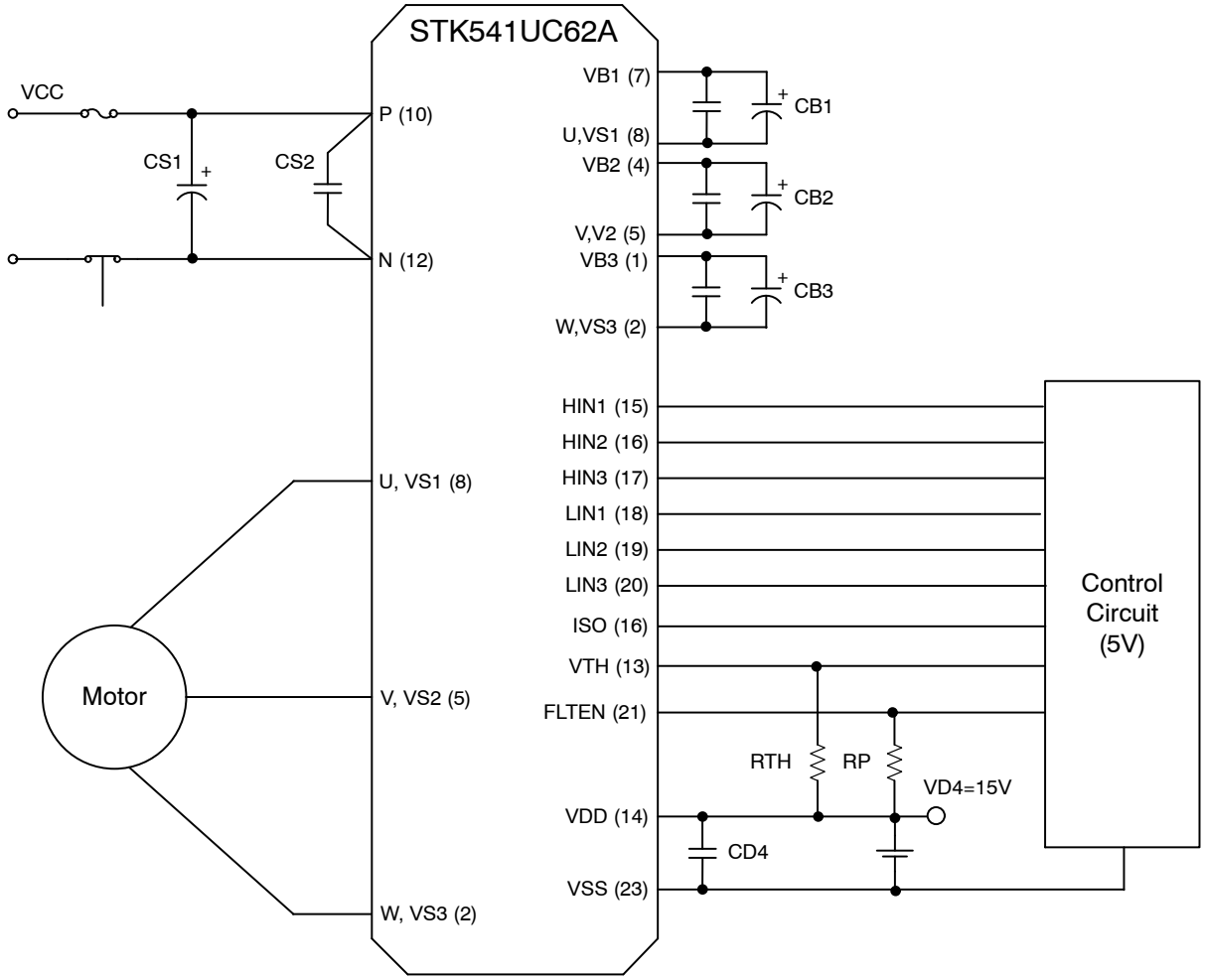


Figure 2. Application Schematic

Function Description

1. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μF.
2. The “FLTEN” terminal (Pin 21) is I/O terminal; Fault output / Enable input. It is used to indicate an internal fault condition of the module and also can be used to disable the module operation.
3. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used.
4. The “ISO” terminal (Pin 22) is current monitor terminal. When the pull−down resister is used, please select it more than 5.6 kΩ
5. As protection of IPM to the unusual current by a short circuit etc. it recommends installing shunt resistors and an over−current protection circuit outside. Moreover, for safety, a fuse on Vcc line is recommended.
6. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.
7. When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

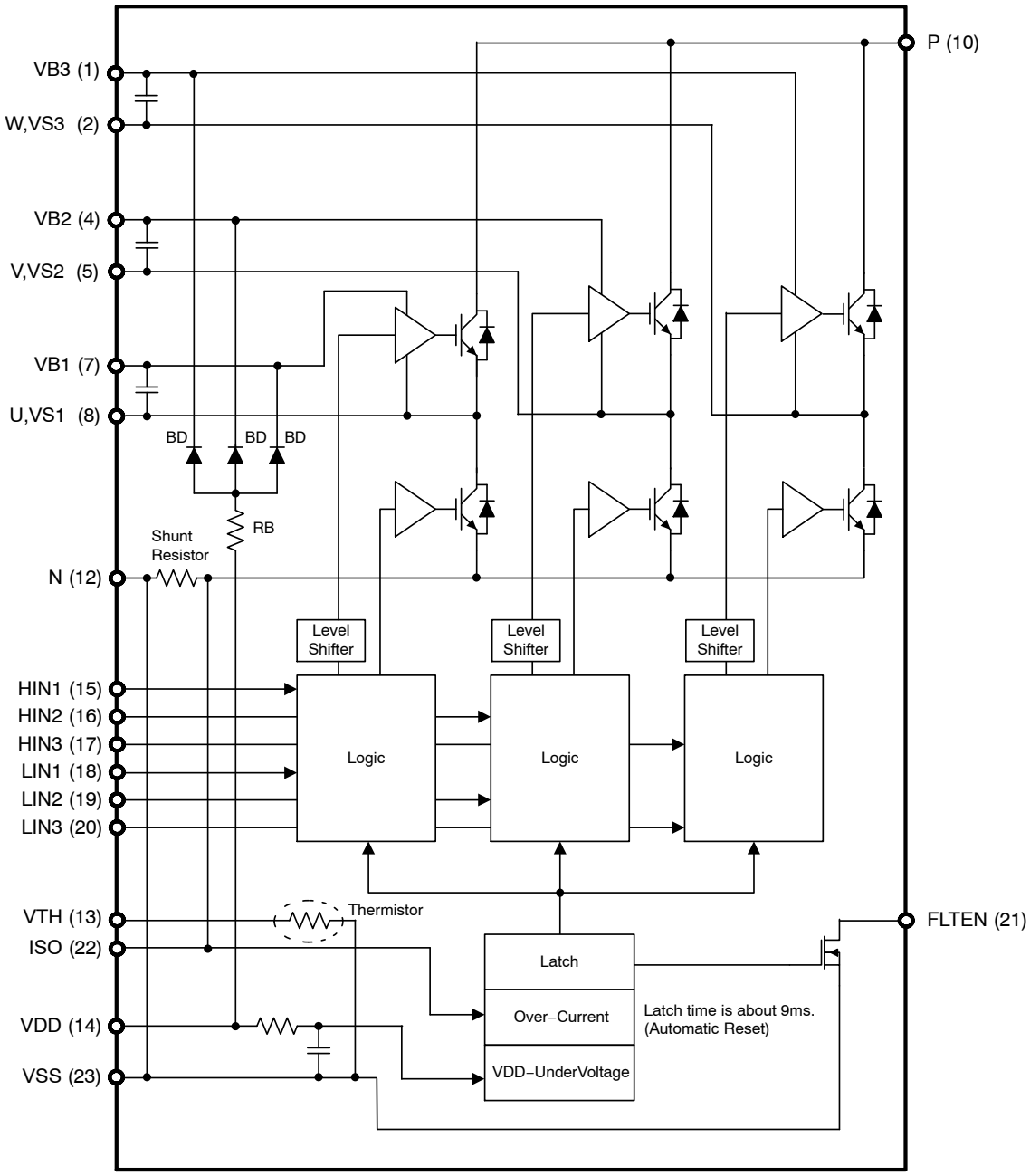


Figure 3. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Label	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 − High Side Floating Supply Offset Voltage
4	VB2	High Side Floating Supply Voltage 2
5	V, VS2	Output 2 − High Side Floating Supply Offset Voltage
7	VB1	High Side Floating Supply Voltage 1
8	U, VS1	Output 1 − High Side Floating Supply Offset Voltage
10	P	Positive Bus Input Voltage
12	N	Negative Bus Input Voltage
13	VTH	Temperature Feedback
14	VDD	+15 V Main Supply
15	HIN1	Logic Input High Side Gate Driver − Phase U
16	HIN2	Logic Input High Side Gate Driver − Phase V
17	HIN3	Logic Input High Side Gate Driver − Phase W
18	LIN1	Logic Input Low Side Gate Driver − Phase U
19	LIN2	Logic Input Low Side Gate Driver − Phase V
20	LIN3	Logic Input Low Side Gate Driver − Phase W
21	FLTEN	Fault output and Enable
22	ISO	Current monitor output
23	VSS	Negative Main Supply

1. Pins 3, 6, 9, 11 are not present.

Table 2. ABSOLUTE MAXIMUM RATINGS at T_C = 25°C, (Note 2)

Symbol	Parameter	Min	Max	Unit
Supply voltage	VCC	P to N, surge < 500 V (Notes 3)	450	V
Collector−emitter voltage	VCE	P to U, V, W or U, V, W, to N	600	V
Output current	Io	P,N,U,V,W terminal current	±10	A
		P,N,U,V,W terminal current, Tc = 100°C	±5	A
Output peak current	Iop	P,N,U,V,W terminal current, P.W. = 1ms	±20	A
Pre−driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, VDD to VSS (Notes 4)	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3	−0.3 to 7	V
FLTEN terminal voltage	VFLTEN	FLTEN terminal	−0.3 to VDD	V
Maximum power dissipation	Pd	IGBT per 1 channel	22	W
Junction temperature	Tj	IGBT, FRD, Pre−Driver IC	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating case temperature	Tc	IPM case	−40 to +100	°C
Tightening torque		A screw part (Notes 5)	0.9	Nm
Withstand voltage	Vis	50 Hz sine wave AC 1 minute (Notes 6)	2000	VRMS

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. Surge voltage developed by the switching operation due to the wiring inductance between P and N terminal.
4. VD1=VB1 to U, VD2=VB2 to V, VD3=VB3 to W, VD4=VDD to VSS terminal voltage.
5. Flatness of the heat−sink should be less than −50 μm to +100 μm.
6. Test conditions : AC2500V, 1 second
7. Reference voltage is “VSS” terminal voltage unless otherwise specified.

Table 3. RECOMMENDED OPERATING RANGES (at T_C = 25°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	P to N	0	280	450	V
Pre−driver supply voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} (Note 8)	13.5	15	16.5	V
ON−state input voltage	VIN(ON)	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3	0	–	0.3	V
OFF−state input voltage	VIN(OFF)		3.0	–	5.0	
PWM frequency	fPWM		1.0		20	kHz
Dead time	DT	Turn−off to turn−on (external)	2.0	–	–	μs
Allowable input pulse width	PWIN	ON and OFF	1.0	–	–	μs
Package mounting torque		‘M3’ type screw	0.6		0.9	Nm

8. Pre−drive power supply (VD4 = 15±1.5 V) must have the capacity of Io = 20 mA (DC), 0.5 A (Peak).

Table 4. ELECTRICAL CHARACTERISTICS T_C = 25°C, VD1, VD2, VD3, VD4 = 15 V (Note 9)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Power output section							
Collector−emitter leakage current	V_{CE} = 600 V		I_{CE}	–	–	100	μA
Bootstrap diode reverse current	VR(BD) = 600 V		IR(BD)	–	–	100	μA
Collector to emitter saturation voltage	Ic = 10 A, Tj = 25°C	Upper side	V_{CE}(sat)	–	1.4	2.3	V
		Lower side (Note 9)		–	1.7	2.6	V
	Ic = 5A, Tj = 100°C	Upper side		–	1.3	–	V
		Lower side (Note 9)		–	1.6	–	V
Diode forward voltage	IF = 10 A, Tj = 25°C	Upper side	VF	–	1.3	2.2	V
		Lower side (Note 9)		–	1.6	2.5	V
	IF = 5 A, Tj = 100°C	Upper side		–	1.2	–	V
		Lower side (Note 9)		–	1.5	–	V
Junction to case thermal resistance	IGBT		θj−c(T)	–	–	5.5	°C/W
	FRD		θj−c(D)	–	–	6.5	
Switching Character							
Switching time	Io = 10 A Inductive load		t ON	0.2	0.4	1.1	μs
			t OFF	–	0.5	1.2	μs
Turn−on switching loss	Ic=5 A, P = 300 V, V_{DD} = 15 V, L = 3.9 mH Tc = 25°C		Eon	–	200	–	μJ
Turn−off switching loss			Eoff	–	130	–	μJ
Total switching loss			Etot	–	330	–	μJ
Turn−on switching loss	Ic = 5 A, P = 300 V, V_{DD} = 15 V, L = 3.9 mH Tc = 100°C		Eon	–	240	–	μJ
Turn−off switching loss			Eoff	–	160	–	μJ
Total switching loss			Etot	–	400	–	μJ
Diode reverse recovery energy	I_F = 5 A, P = 400 V, V_{DD} = 15 V, L = 0.5 mH, Tc = 100°C		Erec	–	17	–	μJ
Diode reverse recovery time			Trr	–	62	–	ns
Reverse bias safe operating area	Io = 20°, VCE = 450 V		RBSOA	Full Square			
Short circuit safe operating area	VCE = 400 V, Tc=100°C		SCSOA	4.0	–	–	μs
Control (Pre−driver) section							
Pre−driver power dissipation	VD1,2,3 = 15 V		ID	–	0.08	0.4	mA
	VD4 = 15 V			–	1.6	4.0	

Table 4. ELECTRICAL CHARACTERISTICS T_C = 25°C, VD1, VD2, VD3, VD4 = 15 V (Note 9)

High level Input voltage	HIN1,HIN2,HIN3, LIN1,LIN2,LIN3 to VSS	Vin H	2.5	–		V
Low level Input voltage		Vin L	–	–	0.8	V
Input threshold voltage hysteresis		Vinth(hys)	0.5	0.8	–	V
Logic 1 input leakage current	VIN = +3.3V	I_{IN+}	76	118	160	μA
Logic 0 input leakage current	VIN = 0 V	I_{IN-}	97	150	203	μA
FLTEN terminal sink current	FAULT:ON / VFLTEN = 0.1 V	IoSD	–	2.0	–	mA
FLTEN clearance delay time	From time fault condition clear	FLTCLR	6.0	9.0	12.0	ms
FLTEN Threshold	VEN rising	VEN+	2.5		–	V
	VEN falling	VEN−	–	–	0.8	V
V_{CC} and V_{BS} supply undervoltage protection reset		V_{CCUV+} V_{BSUV+}	10.5	11.1	11.7	V
V_{CC} and V_{BS} supply undervoltage protection set		V_{CCUV-} V_{BSUV-}	10.3	10.9	11.5	V
V_{CC} and V_{BS} supply undervoltage hysteresis		V_{CCUVH} V_{BSUVH}	0.14	0.2		V
Output level for current monitor	Io = 10 A	ISO	0.30	0.33	0.36	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Reference voltage is “VSS” terminal voltage unless otherwise specified.

APPLICATIONS INFORMATION

Input / Output Timing Chart

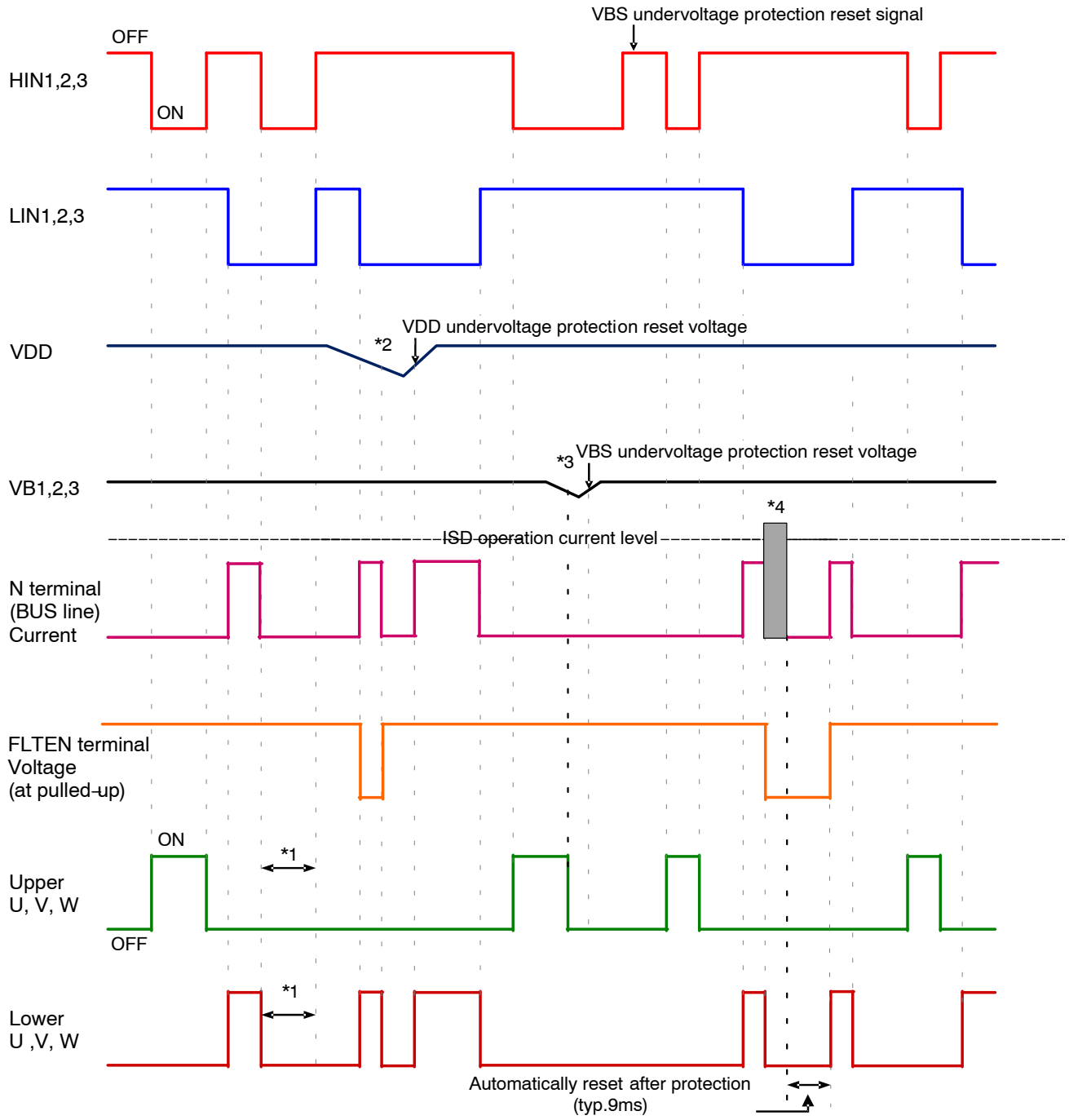


Figure 4. Input/Output Timing Chart

NOTES:

1. Shows the prevention of shoot−thru via control logic, however, more dead time must be added to account for switching delay externally.
2. When VDD decreases all gate output signals will go low and cut off all 6 IGBT outputs. When VDD rises the operation will resume immediately.
3. When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
4. In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in typ. 9ms after the over current condition is removed.

Table 5. LOGIC LEVEL TABLE

INPUT			OUTPUT			
HIN	LIN	OCP	High side IGBT	Low side IGBT	U,V,W	FLTEN
H	L	OFF	OFF	ON	P	OFF
L	H	OFF	ON	OFF	N	OFF
L	L	OFF	OFF	OFF	High Impedance	OFF
H	H	OFF	OFF	OFF	High Impedance	OFF
X	X	ON	OFF	OFF	High Impedance	ON

Table 6. THERMISTOR CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
	R_{100}	Tc = 100°C	5.12	5.38	5.66	kΩ
B−Constant (25 to 50°C)	B		4160	4250	4335	K
Temperature Range			−40	−	+125	°C

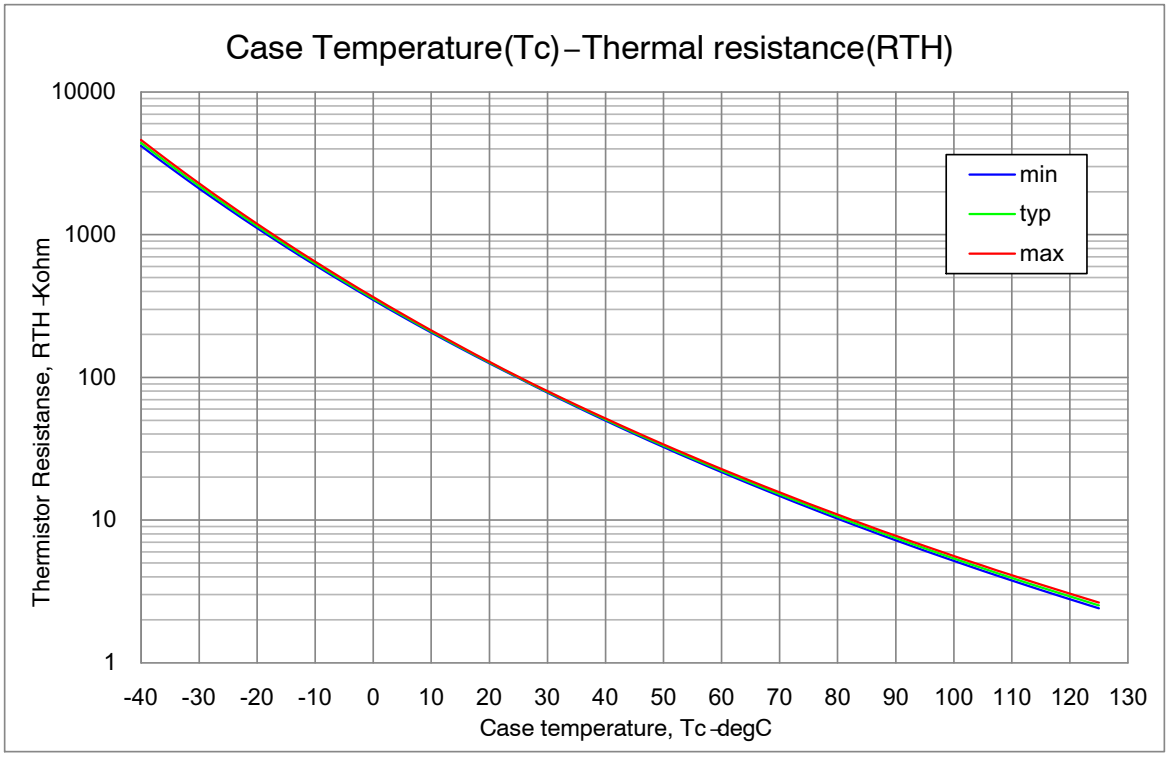


Figure 5. Thermistor Resistance versus Case Temperature

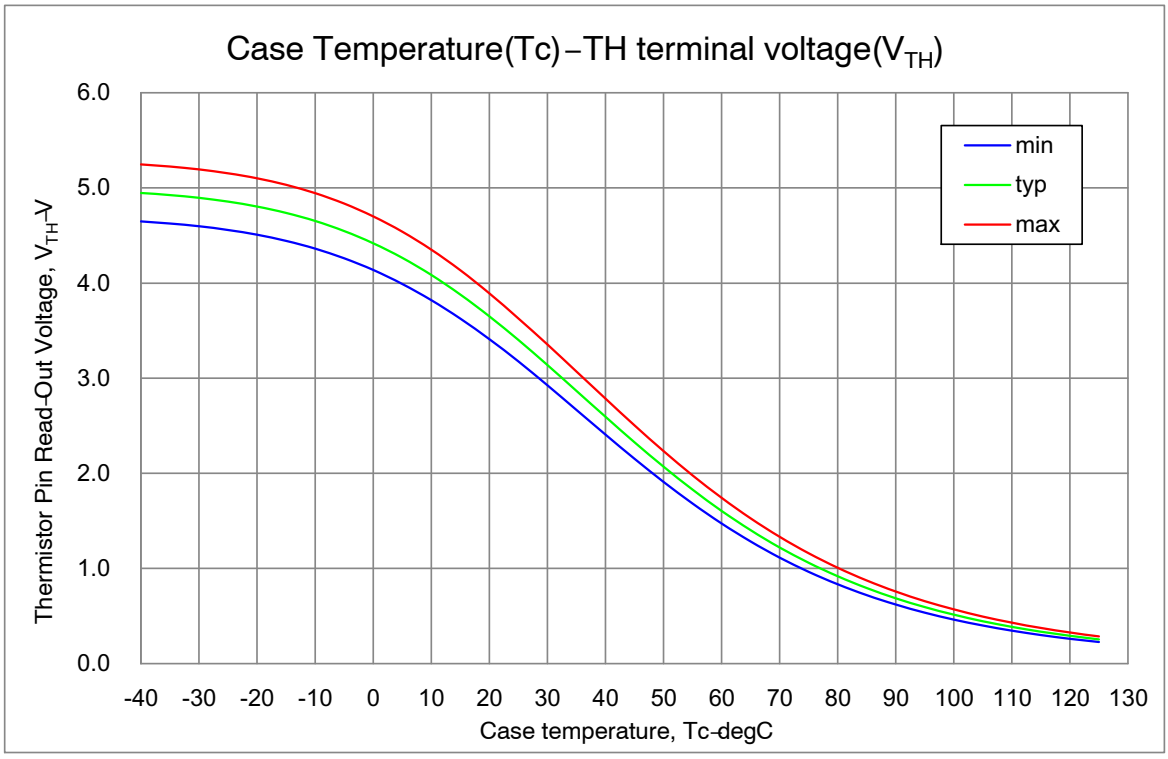


Figure 6. Thermistor Voltage versus Case Temperature Condition: Pull−up resistor = 4.7 kphm, Pull−up voltage of TH = 5 V

Fault Output

The FLTEN terminal is an open drain output requiring a pull−up resistor. If the pull−up voltage is 5 V, use a pull−up resistor with a value of 6.8 kΩ or higher. If the pull−up voltage is 15 V, use a pull−up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a VDD under voltage or an overcurrent condition.

The terminal has a function of enable output, this pin is used to enable or shut down the built−in driver. If the voltage on the FLTEN pin rises above the ENABLE ON−state voltage, the output drivers are enabled. If the voltage on the FLTEN pin falls below the ENABLE OFF−state voltage, the drivers are disabled.

Under Voltage Lockout Protection.

If VDD goes below the VDD supply under voltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply under voltage lockout rising threshold. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent Protection

Over current protection is implemented by measuring the voltage across a shunt resistor to negative supply terminal. In case of an OCP fault the gate drivers are shut down internally and the external Fault signal becomes active (low).

Once activated by a fault condition the FAULT signal output returns to inactive (and is pulled high by the external resistor) when the fault condition is over and the fault clear time (FLTCLR) has passed. This implies that the system microcontroller needs to disable all input signals to the module by driving them low upon detection of a fault condition. An additional fuse is recommended to protect against system level or abnormal over−current fault conditions.

Capacitors on High Voltage and V_{DD} supplies

Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor.

Minimum input pulse width

When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS : Bootstrap power supply.
  15 V is recommended.
- QG : Total gate charge of IGBT at VBS = 15 V.
  89nC

- UVLO : Falling threshold for UVLO. Specified as 12 V.
- ID_{MAX} : High side drive consumption current. Specified as 400 μA
- t_{ONMAX} : Maximum ON pulse width of high side IGBT.

Capacitance calculation formula

CB = (QG + IDMAX * tONMAX) / (VBS − UVLO)

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

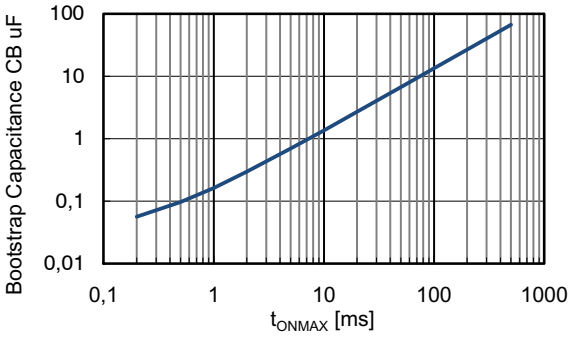


Figure 7. Bootstrap capacitance versus tONMAX

Table 7. MOUNTING INSTRUCTIONS

Item	Recommended Condition
Pitch	56.0 ± 0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D : 7 mm, d : 3.2 mm and t : 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to +100 μm Screw holes must be countersunk No contamination on the heat sink surface that contacts IPM
Torque	Final tightening : 0.6 to 0.9 Nm Temporary tightening : 20 to 30 % of final tightening
Grease	Silicone grease Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back

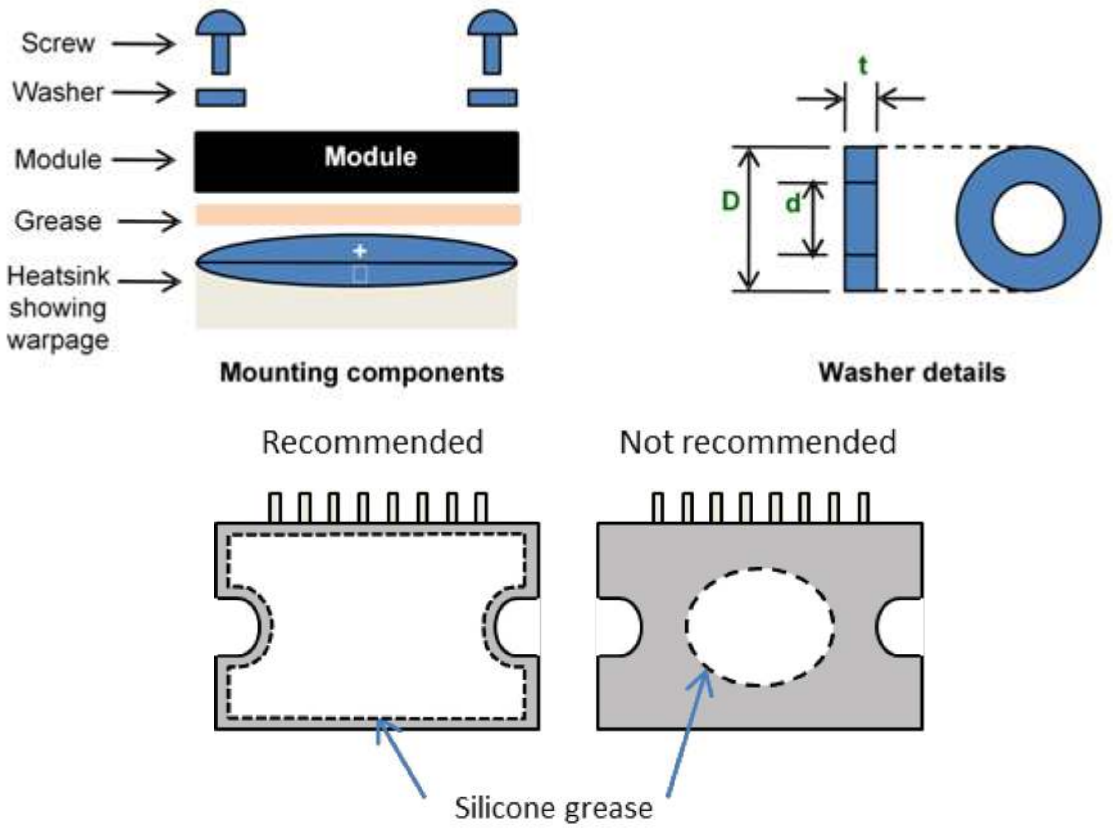


Figure 8. Module Mounting Details: Components; Washer Drawing; Need for Even Spreading of Thermal Grease

- V_{CE}(sat) (Test by pulse)

- I_{CE}

	U+	V+	W+	U−	V−	W−
M	10	10	10	8	5	2
N	8	5	2	12	12	12

	U(DB)	V(DB)	W(DB)
M	7	4	1
N	23	23	23

U+, V+, W+ : High side phase
U−, V−, W− : Low side phase

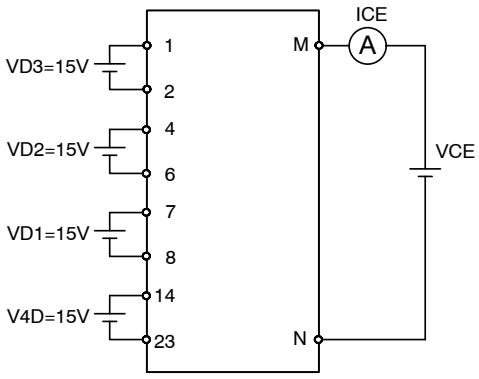


Figure 9. Test Circuit for ICE

- V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	10	10	10	8	5	2
N	8	5	2	12	12	12
m	15	16	17	18	19	

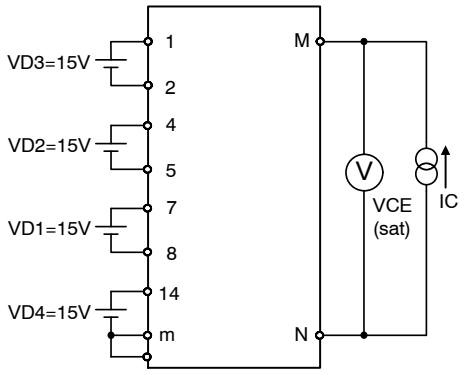


Figure 10. Test Circuit for V_{CE} (sat)

- V_F (Test by pulse)

	U+	V+	W+	U−	V−	W−
M	10	10	10	8	5	2
N	8	5	2	12	12	12

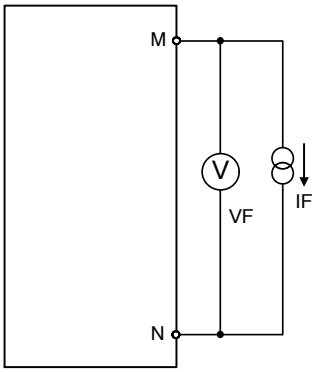


Figure 11. Test Circuit for V_{CE} (sat)

- ID

	VD1	VD2	VD3	VD4
M	7	4	1	14
N	8	5	2	23

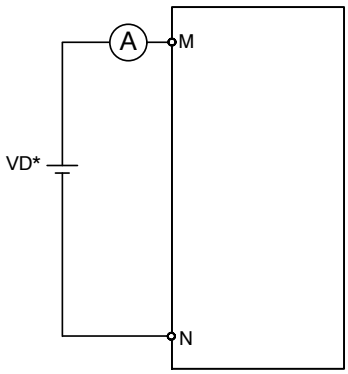
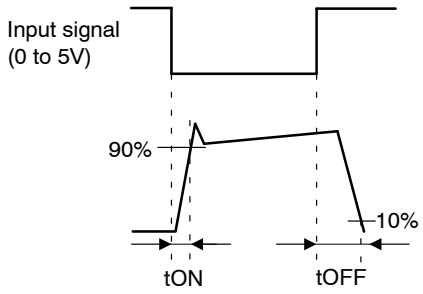


Figure 12. Test Circuit for ID

- Switching time (The circuit is a representative example of the low side U phase)



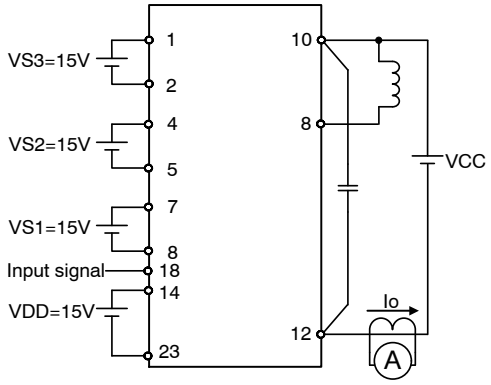


Figure 13. Switching Time Test Circuit

Table 8. ORDERING INFORMATION

Device	Marking	Package	Shipping
STK541UC62A−E	STK541UC62A	SIP23 62x21.8 (Pb−Free)	8 Unit / Tube

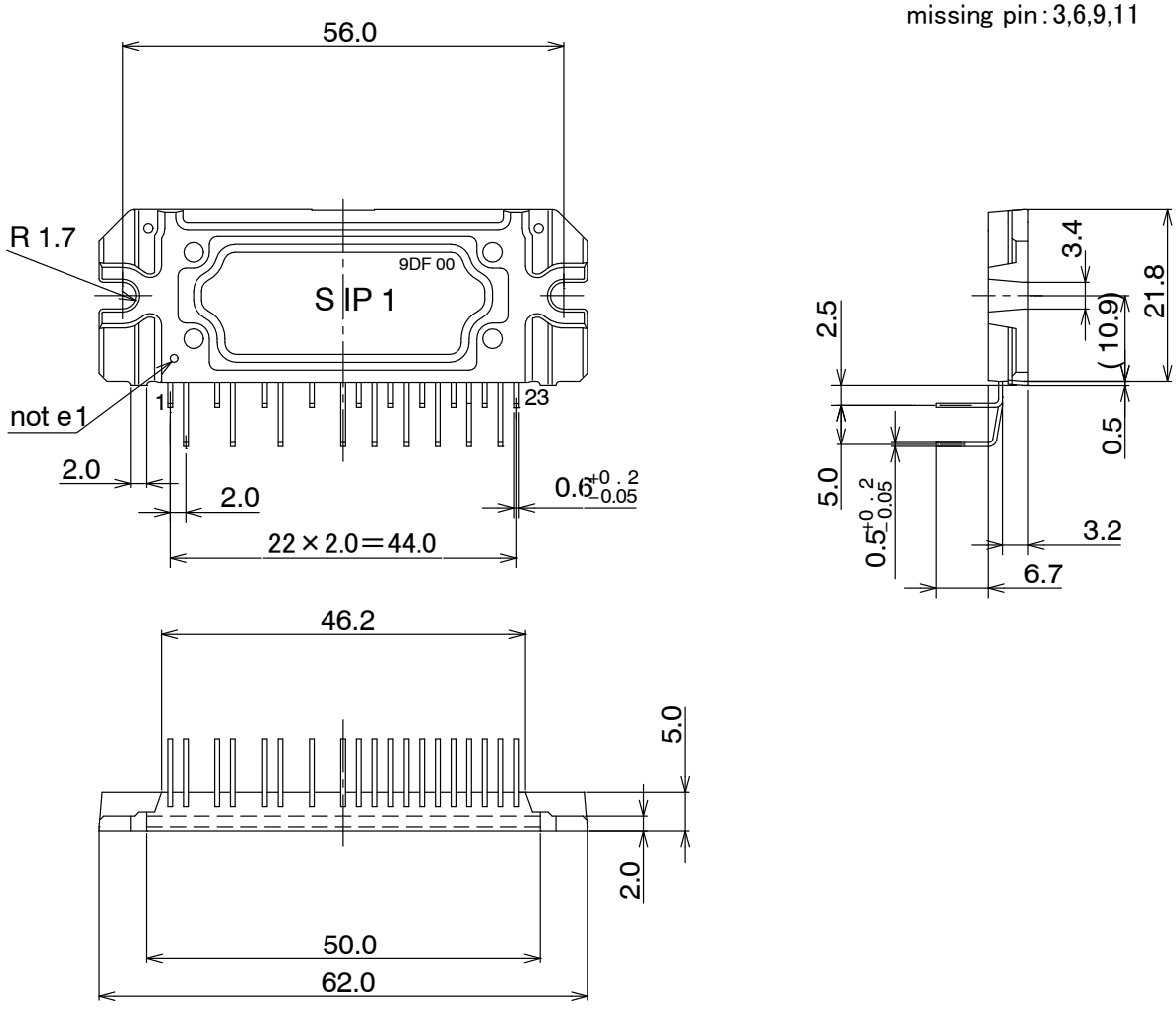
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP23 56x21.8
CASE 127BV
ISSUE O

DATE 30 APR 2012

missing pin : 3,6,9,11



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