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Evaluating the ADRF6780 5.9 GHz to 23.6 GHz, Wideband Upconverter

FEATURES

Full feature evaluation board for the ADRF6780
On-board USB for serial port interface (SPI) control
5 V operation
ACE software interface for SPI control

EVALUATION KIT CONTENTS

ADRF6780-EVALZ evaluation board

EQUIPMENT NEEDED

5 V dc power supply
RF signal generator
Spectrum analyzer

DOCUMENTS NEEDED

ADRF6780 data sheet
ADRF6780-EVALZ evaluation board user guide

SOFTWARE NEEDED

Analysis|Control|Evaluation (ACE) software
USB drivers for the ADRF6780-042654, Rev. A (ADRF6780-EVALZ) evaluation board

ADRF6780-042654, REV. A (ADRF6780-EVALZ)
EVALUATION BOARD

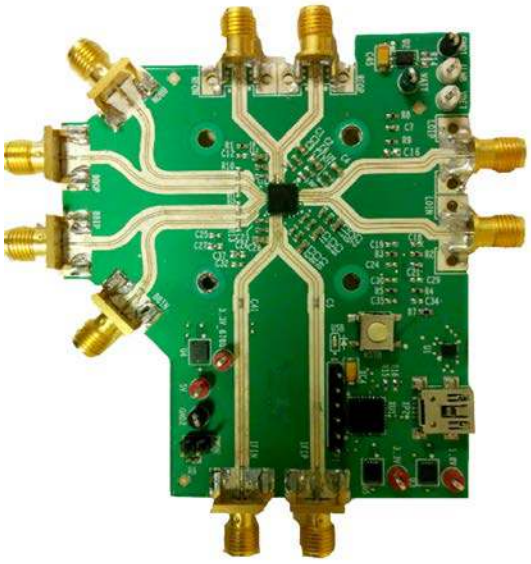

Figure 1.

GENERAL DESCRIPTION

The ADRF6780 is a silicon germanium (SiGe) design, wideband, microwave upconverter optimized for point to point microwave radio designs operating in the 5.9 GHz to 23.6 GHz frequency range.

The upconverter offers two modes of frequency translation. The device is capable of direct conversion to radio frequency (RF) from baseband IQ input signals, as well as single sideband (SSB) upconversion from a real intermediate frequency (IF) input carrier frequency. The baseband inputs are high impedance and are generally terminated off chip with 100 Ω differential back terminations. The baseband IQ input path can be disabled and a modulated real IF signal anywhere from 800 MHz to 3500 MHz can fed into the IF input path and upconverted to 5.9 GHz to 23.6 GHz while suppressing the unwanted sideband by typically better than 25 dBc. The serial port interface (SPI) allows for tweaking of the quadrature phase adjustment to allow for optimum sideband suppression. In addition, the SPI interface allows for powering down the output power detector to reduce power consumption when power monitoring is not necessary.

The ADRF6780 upconverter comes in a compact, thermally enhanced, 5 mm × 5 mm LFCSP package. The ADRF6780 operates over the −40°C to +85°C temperature range.

For full details on the ADRF6780, see the ADRF6780 data sheet, which should be consulted in conjunction with this ADRF6780-EVALZ evaluation board user guide when using this evaluation board.

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REVISION HISTORY

1/2019—Rev. 0 to Rev. A

Change to Evaluation Board Hardware Section 3
Change to Figure 3 3
Replaced Figure 30 16
Changes to Table 2 19

4/2016—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADRF6780-042654, Rev. A (ADRF6780-EVALZ) comes with a ADRF6780 chip, and Figure 2 shows the location of this chip on the evaluation board and the block diagram of the ADRF6780.

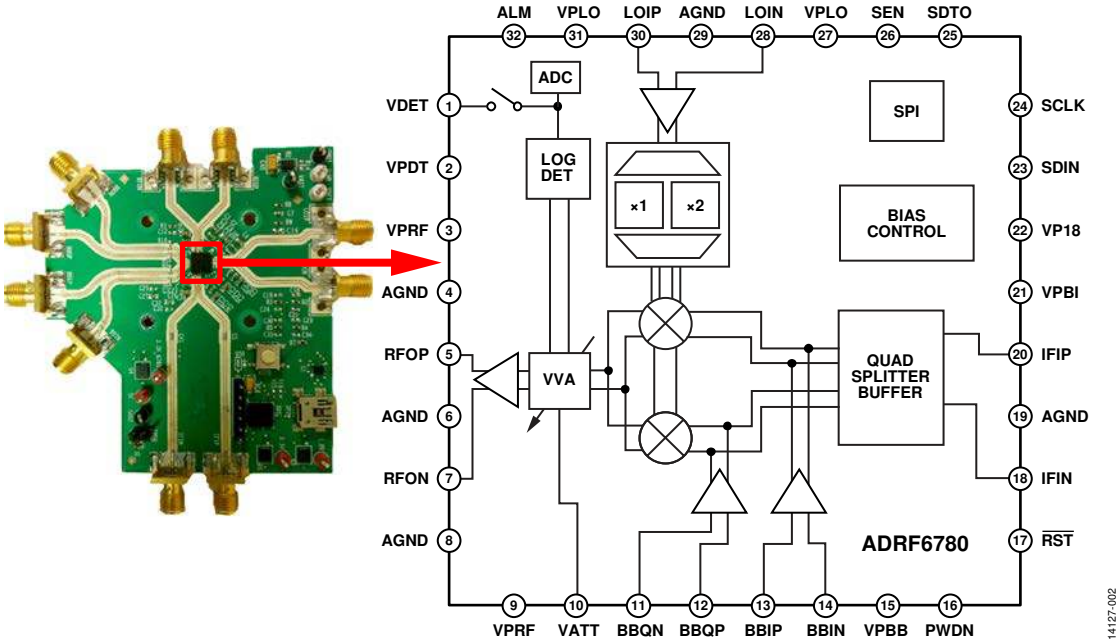


Figure 2. Evaluation Board Configuration

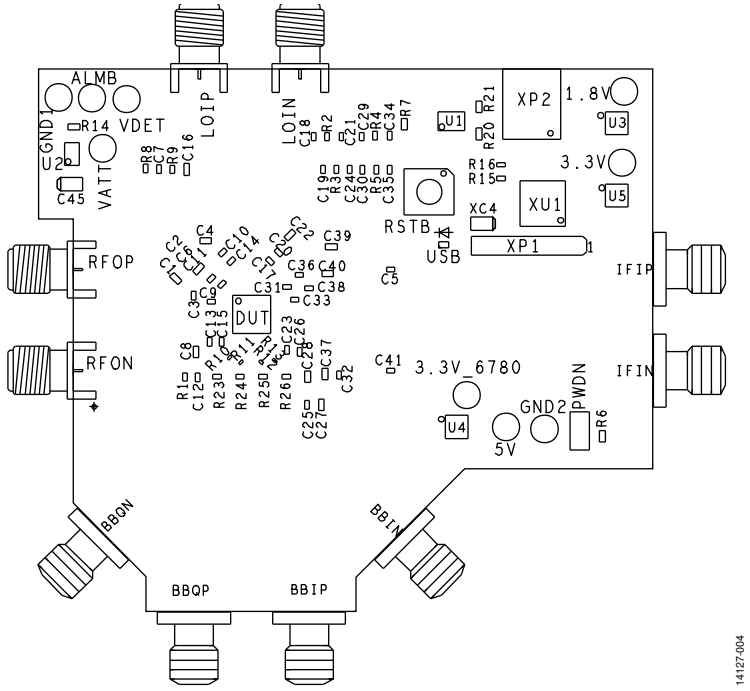


Figure 3. Top View of the ADRF6780-EVALZ

The ADRF6780-EVALZ evaluation board has IF/IQ inputs for the two LO modes (×1/×2) that the device supports. When evaluating the device in IF mode, connect the IF inputs, IFIN and IFIP, to a signal generator. Note that, when using the IF mode, the IQ inputs must be kept floating without termination resistors (R10 to R13). When evaluating the devices in IQ mode, connect the IQ inputs, BBIN, BBIP, BBQN, and BBQP, to an IQ baseband generator. Use 0 Ω series resistors (R10, R11, R12, and R13) with the IQ inputs. The ADRF6780-EVALZ runs on 5 V dc supplies. Figure 3 shows the top side of the ADRF6780-EVALZ evaluation board and is intended for evaluation purposes only with no implied guarantee of performance or reliability.

Connect the 5 V dc to the 5V test point, and ground to the GND1 test point. The 3.3V and 1.8V test points are for evaluation purposes only. Connect the spectrum analyzer differentially to the Southwest/SRI 2.92 mm connectors, RFON and RFOP. It is recommended to use a 180° hybrid from 5.9 GHz to 23.6 GHz to view the single-ended RF output. Connect LOIN and LOIP the Southwest/SRI 2.92 mm connectors, differentially to the low phase signal generator. Use a 180° hybrid from 5.9 GHz to 14 GHz for the differential inputs. In IF mode, connect IFIP and IFIN differentially to the signal generator (use a 180° hybrid from 500 MHz to 4 GHz for the differential inputs), keep the IQ inputs floating, and remove any termination from the ADRF6780-EVALZ. In IQ mode, connect BBIN, BBIP, BBQN, and BBQP to the I/Q baseband generator. In addition, connect the PC to the ADRF6780-EVALZ by using the mini-USB connector (J2). See Figure 5 and Figure 6 for the ADRF6780-EVALZ lab connections. When using the AD5601 nanoDAC® to generate the VATT voltage, note that the 2600 mV dc power supply is not needed (see the Setting VATT Voltage for the ADRF6780 section for additional details). Figure 4 shows the block diagram of the ADRF6780 lab bench setup, and Figure 3 shows the top view of the ADRF6780-EVALZ. The ADRF6780-EVALZ also features a PWDN jumper to power down the device and a reset button to hard reset the ADRF6780-EVALZ.

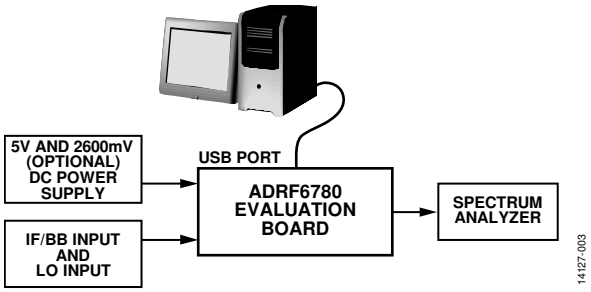


Figure 4. Block Diagram of the ADRF6780

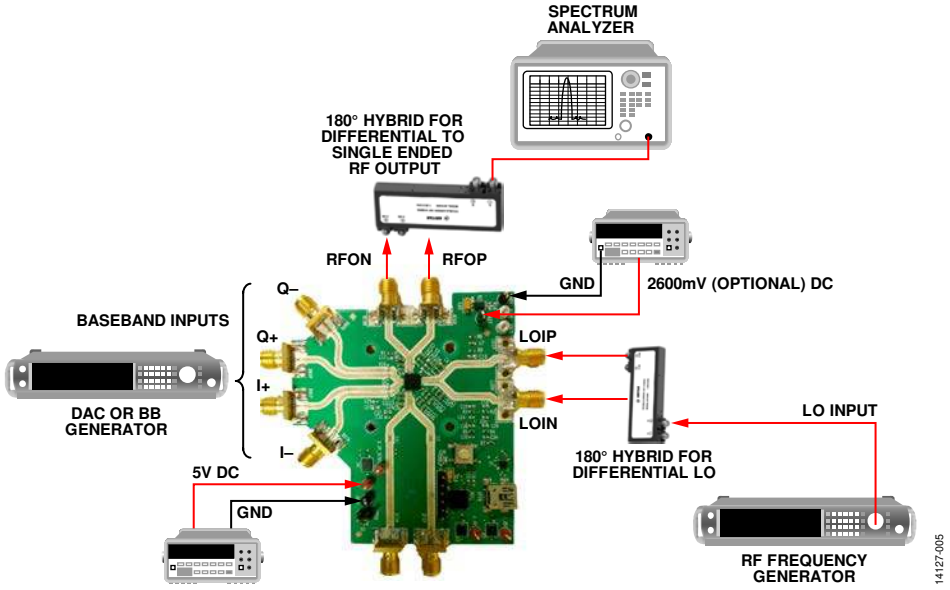


Figure 5. ADRF6780 Lab Bench Setup for the IQ Inputs

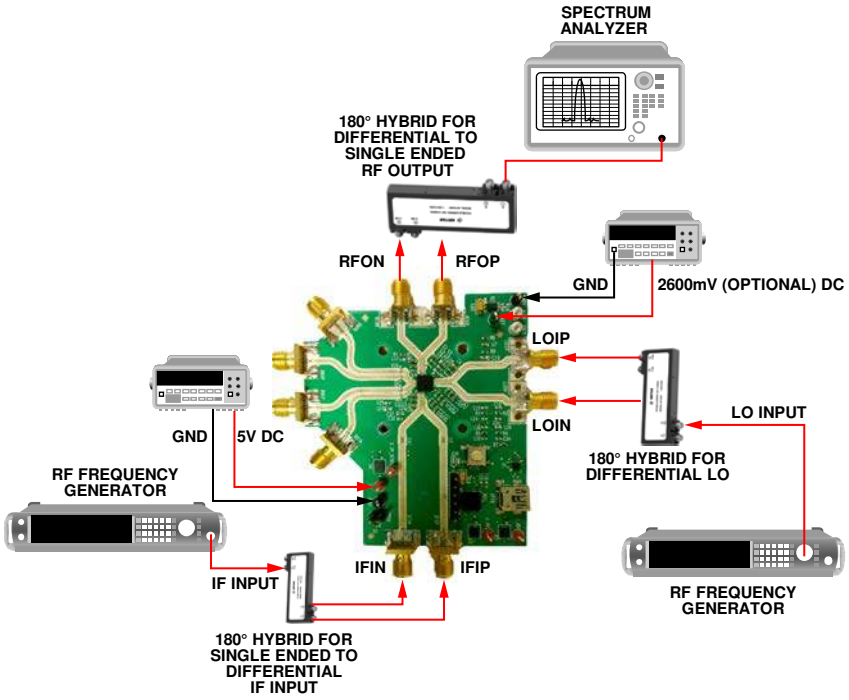


Figure 6. ADRF6780 Lab Bench Setup for the IF Inputs

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND ADRF6780 PLUGINS AND DRIVERS

The ADRF6780-EVALZ software uses the Analog Devices, Inc., Analysis|Control|Evaluation (ACE) software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

After the ACE software is installed, USB drivers must also be installed to use the ADRF6780-EVALZ. To install these drivers, go to the Evaluation Kits section of the ADRF6780 product page.

Once the installations are finished, the ADRF6780-EVALZ evaluation board plugin will appear when you open the ACE software (see Figure 7).

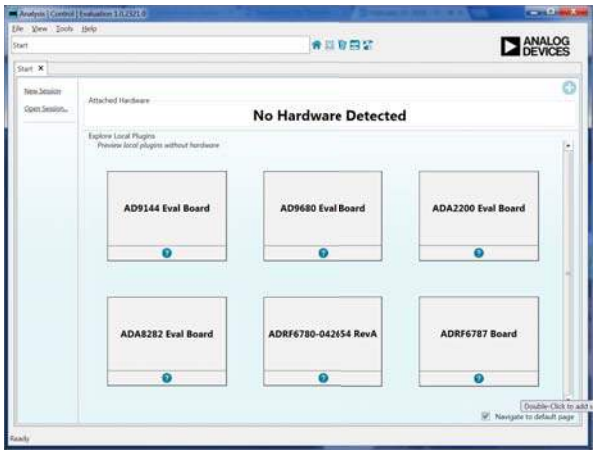


Figure 7. ADRF6780-EVALZ Evaluation Board Plugin Window after Opening the ACE Software

INITIAL SETUP

To set up the ADRF6780-EVALZ, take the following steps:

1. Connect a USB cable to the PC and then to the ADRF6780-EVALZ.
2. Power up the ADRF6780-EVALZ with a 5 V dc supply. When the USB cable is connected to the PC, the blue LED lights up. The PC should recognize the ADRF6780-EVALZ as the ADRF6780-042654, Rev. A.
3. Open the ACE software. The ADRF6780-042654, Rev. A (ADRF6780-EVALZ) appears in the **Attached Hardware** section (see Figure 8). Double-click on the evaluation board plugin. If the device is turned off and on, or if the USB cable is unplugged and plugged in, while the ACE software is open, you may lose contact with the ADRF6780-EVALZ. If this happens, click the **System** tab, then click the **USB** symbol on the ADRF6780-042654, Rev. A subsystem, and then click **Acquire** to talk to the ADRF6780-EVALZ again.

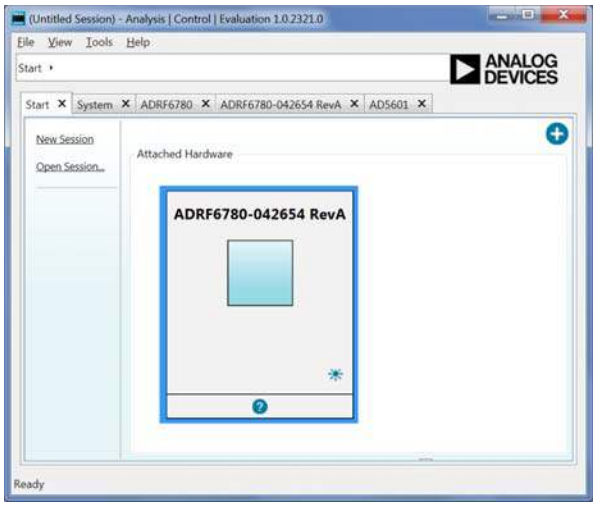


Figure 8. Attached Hardware Section when the ADRF6780-042654, Rev. A (ADRF6780-EVALZ) Is Connected

4. The **ADRF6780-042654, Rev. A** tab then opens. On the left-side of the screen, click **Initial Configuration** to open this menu. Go to **Gain Setup** to enter the VATT voltage Note that 2600 mV is the highest gain for the device (see Figure 9). Click **Appl**y and then double-click the **ADRF6780** button (see the middle of the screen shown in Figure 9).

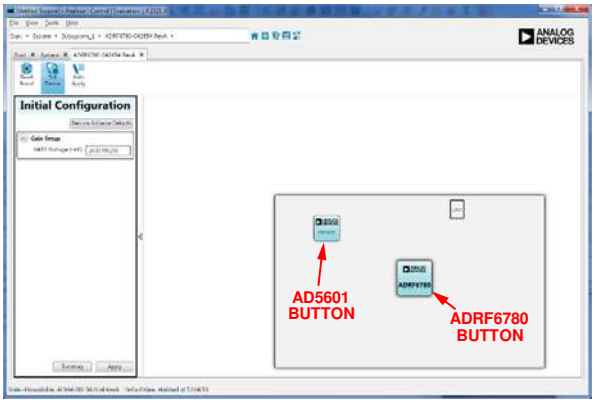


Figure 9. Initial Configuration for the Gain Setup and Board Plugin View

5. The ADRF6780 block diagram now appears (see Figure 10).

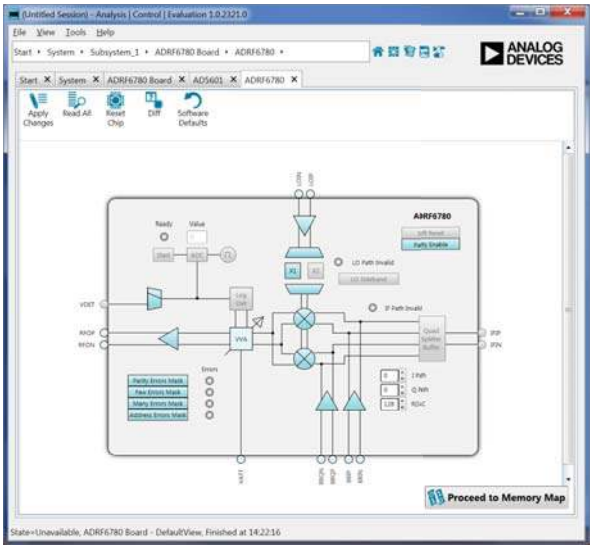


Figure 10. ADRF6780 Block Diagram in the ACE Software

ADRF6780 BLOCK DIAGRAM AND ITS FUNCTIONS

The ADRF6780 ACE plugin is conveniently organized so that it appears similar to the block diagram shown in the ADRF6780 data sheet. In this way, it is easy to correlate the functions on the ADRF6780-EVALZ with the descriptions in the ADRF6780-EVALZ data sheet. A full description of each block and register and its settings is given in the ADRF6780 data sheet. Some of the blocks and their functions are described as they pertain to the ADRF6780-EVALZ. The full screen ADRF6780 block diagram with labels is shown in Figure 11, and Table 1 describes the functionality of each block.

Due to ongoing improvements and enhancements to the software, note that some of the screen images in this user guide may not be the latest versions found in the software.

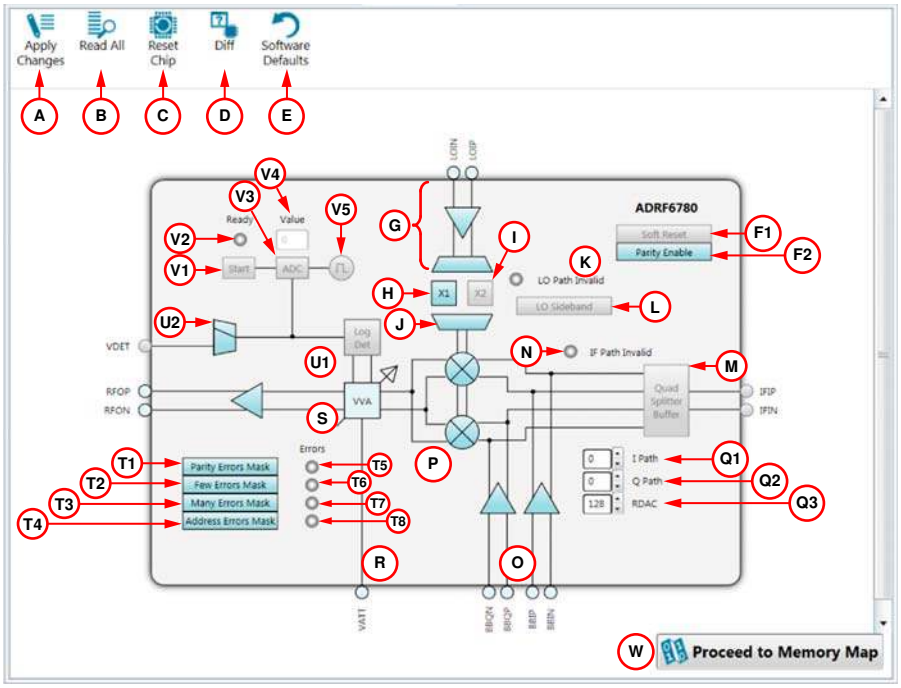


Figure 11. ADRF6780 Block Diagram with Labels

Table 1. ADRF6780 Block Diagram Label Functions (See Figure 11)

Label	Function
A	To apply all of the register values to the device, click **Apply Changes** (Label A). If **Auto Apply** is highlighted in the **ADRF6780-042654, Rev. A** tab, then the **Apply Changes** feature (Label A) and the **Read All** feature (Label B) continuously run every few seconds, and the **Apply Changes** (Label A) and **Read All** (Label B) buttons do not need to be clicked to apply or read back the block diagram settings.
B	To read back all of the SPI registers of the device, click **Read All** (Label B). If **Auto Apply** is highlighted in the **ADRF6780-042654, Rev. A** tab, then the **Apply Changes** feature (Label A) and the **Read All** feature (Label B) continuously run every few seconds, and the **Apply Changes** (Label A) and **Read All** (Label B) buttons do not need to be clicked to apply or read back the block diagram settings.
C	Click **Reset Chip** (Label C) to reset the 1.8 V SPI. Note that it has similar functionality as the **Soft Reset** button (Label F1).
D	Click **Diff** (Label D) to shows registers that are different on the device.
E	Click **Software Defaults** (Label E) to load the software defaults on to the device, and then click **Apply Changes** (Label A).
F1	Click **Soft Reset** (Label F1) and then **Apply Changes** (Label A) to set the SOFT_RESET bit (Bit 14, Register 0x00). When **Soft Reset** is highlighted, the soft reset feature is enabled. When **Soft Reset** is not highlighted, the soft reset feature is disabled. After resetting the device, disable the SOFT_RESET bit and enable the PARITY_EN bit (Bit 15, Register 0x00).
F2	Click **Parity Enable** (Label F2) and then **Apply Changes** (Label A) to set the PARITY_EN bit (Bit 15, Register 0x00). When **Parity Enable** is highlighted, the PARITY_EN bit is enabled. When **Parity Enable** is not highlighted, the PARITY_EN bit is disabled.
G	Click **LO Buffer Enable** (Label G) and **Apply Changes** (Label A) to set the LO_BUFFER_ENABLE bit (Bit 6, Register 0x03). When **LO Buffer Enable** is highlighted, the LO buffer is enabled. When **LO Buffer Enable** is not highlighted, the LO buffer is disabled.
H	Click **LO PPF Enable** (Label H) and **Apply Changes** (Label A) to set the LO_PPF_ENABLE bit (Bit 2, Register 0x03). When **LO PPF Enable** is highlighted, the LO_PPF_ENABLE bit is enabled. When **LO PPF Enable** is not highlighted, the LO_X2_ENABLE bit is disabled.

Label	Function
I	Click **LO ×2 Enable** (Label I) and **Apply Changes** (Label A) to set the LO_×2_ENABLE bit (Bit 3, Register 0x03). When **LO ×2 Enable** is highlighted, the LO_×2_ENABLE bit is enabled. When **LO ×2 Enable** is not highlighted, the LO_×2_ENABLE bit is disabled.
J	Click **LO Enable** (Label J) and **Apply Changes** (Label A) to set the LO_ENABLE bit (Bit 1, Register 0x03). When **LO Enable** is highlighted, the LO_ENABLE bit is enabled. When **LO Enable** is not highlighted, the LO_ENABLE bit is disabled.
K	When the LO_PPF_ENABLE and LO_×2_ENABLE bits (Bits[3:2], Register 0x03) are enabled simultaneously, the **LO Path Invalid** light turns green.
L	Click **LO Sideband** (Label L) and **Apply Changes** (Label A) to set the LO_SIDEBAND bit (Bit 10, Register 0x05). When **LO Sideband** is highlighted, the LO_SIDEBAND bit is enabled. When **LO Sideband** is not highlighted, the LO_SIDEBAND bit is disabled.
M	Click **Quad Splitter Buffer** (Label M) and **Apply Changes** (Label A) to set the IF_MODE_ENABLE bit (Bit 5, Register 0x03). When **Quad Splitter Buffer** is highlighted, the IF_MODE_ENABLE bit is enabled. When **Quad Splitter Buffer** is not highlighted, the IF_MODE_ENABLE bit is disabled.
O	Click **IQ Mode Enable** (Label O) and **Apply Changes** (Label A) to set the IQ_MODE_ENABLE bit (Bit 4, Register 0x03). When **IQ Mode Enable** is highlighted, the IQ_MODE_ENABLE bit is enabled. When **IQ Mode Enable** is not highlighted, the IQ_MODE_ENABLE bit is disabled.
P	Click **Upconverter Bias Enable** (Label P) and **Apply Changes** (Label A) to set the UC_BIAS_ENABLE bit (Bit 0, Register 0x03). When **Upconverter Bias Enable** is highlighted, the UC_BIAS_ENABLE bit is enabled. When **Upconverter Bias Enable** is not highlighted, the UC_BIAS_ENABLE bit is disabled.
Q1 to Q3	Linearity blocks (**I Path**, **Q Path**, and **RDAC**). Use the scroll or enter a value between 0 and 15 in the **I Path** box (Label Q1) and click **Apply Changes** (Label A) to set the I_PATH_PHASE_ACCURACY bits (Bits[3:0], Register 0x05). Use the scroll or enter a value between 0 and 15 in the **Q Path** box (Label Q2) and click **Apply Changes** (Label A) to set the Q_PATH_PHASE_ACCURACY bits (Bits[7:4], Register 0x05). The **I Path** and **Q Path** are each 4-bit controllers that allow users to change the quadrature phase accuracy tuning to lower the RF output image. Use the scroll or enter a value between 0 and 255 in the **RDAC** box (Label Q3) and click **Apply Changes** (Label A) to set the RDAC_LINERIZE bits (Bits[7:0], Register 0x04). The default value is 128. RDAC is an 8-bit controller that can improve the RF harmonic performance.
R	See the Setting VATT Voltage for the ADRF6780 section for additional details.
S	Click **VGA Buffer Enable** (Label S) and **Apply Changes** (Label A) to set the VGA_BUFFER_ENABLE bit (Bit 8, Register 0x03). When **VGA Buffer Enable** is highlighted, the VGA_BUFFER_ENABLE bit is enabled. When **VGA Buffer Enable** is not highlighted, the VGA_BUFFER_ENABLE bit is disabled.
T1 to T8	Error Mask and ReadBack follow: Click **Parity Errors Mask** (Label T1) and **Apply Changes** (Label A) to set the PARITY_ERROR_MASK bit (Bit 15, Register 0x02). When **Parity Errors Mask** is highlighted, the PARITY_ERRORS_MASK bit is enabled. When **Parity Errors Mask** is not highlighted, the PARITY_ERROR_MASK bit is disabled. Click **Few Errors Mask** (Label T2) and **Apply Changes** (Label A) to set the TOO_FEW_ERRORS_MASK bit (Bit 14, Register 0x02). When the **Few Errors Mask** is highlighted, the TOO_FEW_ERRORS_MASK bit is enabled. When the **Few Errors Mask** is not highlighted, the TOO_FEW_ERRORS_MASK bit is disabled. Click **Many Errors Mask** (Label T3) and **Apply Changes** (Label A) to set the TOO_MANY_ERRORS_MASK bit (Bit 13, Register 0x02). When **Many Errors Mask** is highlighted, the TOO_MANY_ERRORS_MASK bit is enabled. When **Many Errors Mask** is not highlighted, the TOO_MANY_ERRORS_MASK bit is disabled. Click **Address Errors Mask** (Label T4) and **Apply Changes** (Label A) to set the ADDRESS_RANGE_ERROR_MASK bit (Bit 12, Register 0x02). When **Address Errors Mask** is highlighted, the ADDRESS_RANGE_ERROR_MASK bit is enabled. When **Address Errors Mask** is not highlighted, the ADDRESS_RANGE_ERROR_MASK bit is disabled. When the PARITY_ERROR_MASK bit (Bit 15, Register 0x02) is set, **Parity Error** will light up green (Label T5) when then the PARITY_ERROR bit (Bit 15, Register 0x01) gets toggled. When the TOO_FEW_ERRORS_MASK bit (Bit 14, Register 0x02) is set, **Too Few Errors** will light up green (Label T6) when the TOO_FEW_ERRORS bit (Bit 14, Register 0x01) gets toggled. When the TOO_MANY_ERRORS_MASK bit (Bit 13, Register 0x02) is set, **Too Many Errors** will light up green (Label T7) when the TOO_MANY_ERRORS bit (Bit 13, Register 0x01) gets toggled. When the ADDRESS_RANGE_ERROR_MASK bit (Bit 12, Register 0x02) is set, **Address Range Error** will light up green (Label T8) when the ADDRESS_RANGE_ERROR bit (Bit 12, Register 0x01) gets toggled.

Label	Function
U1 to U2	Detectors follow. Click **Detector Enable** (Label U1) and **Apply Changes** (Label A) to set the DETECTOR_ENABLE bit (Bit 7, Register 0x03). Note that this turns on the detector. When **Detector Enable** is highlighted, the DETECTOR_ENABLE bit is enabled. When **Detector Enable** is highlighted, the DETECTOR_ENABLE bit is disabled. Click **VDET Output Select** (Label U2) and **Apply Changes** (Label A) to set the VDET_OUTPUT_SELECT bit (Bit 3, Register 0x06). When the switch is set toward the VDET pin (Bit 3 = 1), the detector output can be read from the VDET test point on the board. When the switch is not set toward the VDET test point (Bit 3 = 0), the VDET output does not appear on the test point.
V1 to V5	ADCs follow. Click **ADC Start** (Label V1) and then **Apply Changes** (Label A) to set the ADC_START bit (Bit 2, Register 0x06). When **ADC Start Enable** is highlighted, the ADC_START bit is enabled. When **ADC Start Enable** is not highlighted, the ADC_START bit is disabled. **Ready** light (Label V2) displays the ADC status. Click **Read All** (Label B). If **Ready** LED is green, the ADC is ready. If **Ready** LED is not green then the ADC is busy. This bit reads the ADC_STATUS bit in (Bit 8, Register 0x0C). Click **ADC Enable** (Label V3) and **Apply Changes** (Label A) to set the ADC_ENABLE bit (Bit 1, Register 0x06). When **ADC Enable** is highlighted, the ADC_ENABLE bit is enabled. When **ADC Enable** is not highlighted, the ADC_ENABLE bit is disabled. The ADC **Value** field (Label V4) reads back the decimal ADC value for the detector. It reads back from the ADC_VALUE bits, 8 bits (Bits[7:0], Register 0x0C). Click **ADC Clock** (Label V5) and **Apply Changes** (Label A) to set the ADC_CLOCK_ENABLE bit (Bit 0, Register 0x06). When **ADC Clock** is highlighted, the ADC_CLOCK_ENABLE is enabled. When **ADC Clock** is not highlighted, the ADC_CLOCK_ENABLE is disabled. To read the ADC value, the ADC_CLOCK_ENABLE, ADC_ENABLE, and ADC_START bits (Bits[3:0}, Register 0x06) must be highlighted (press **Apply Changes**, Label A). Next, press **Read All** (Label B). If **Ready** LED (Label V2) is not green, keep pressing **Read All** (Label B) until it is green. When the **Ready** LED is green, click **ADC Start** (Label V1) to disable it (**ADC Start** button unhighlightes), and then press **Apply Changes** (Label A). Lastly, click **Read All** (Label A) again to get the ADC value.
W	Click **Proceed to Memory Map** (Label W) to open the ADRF6780 memory map (see Figure 12).

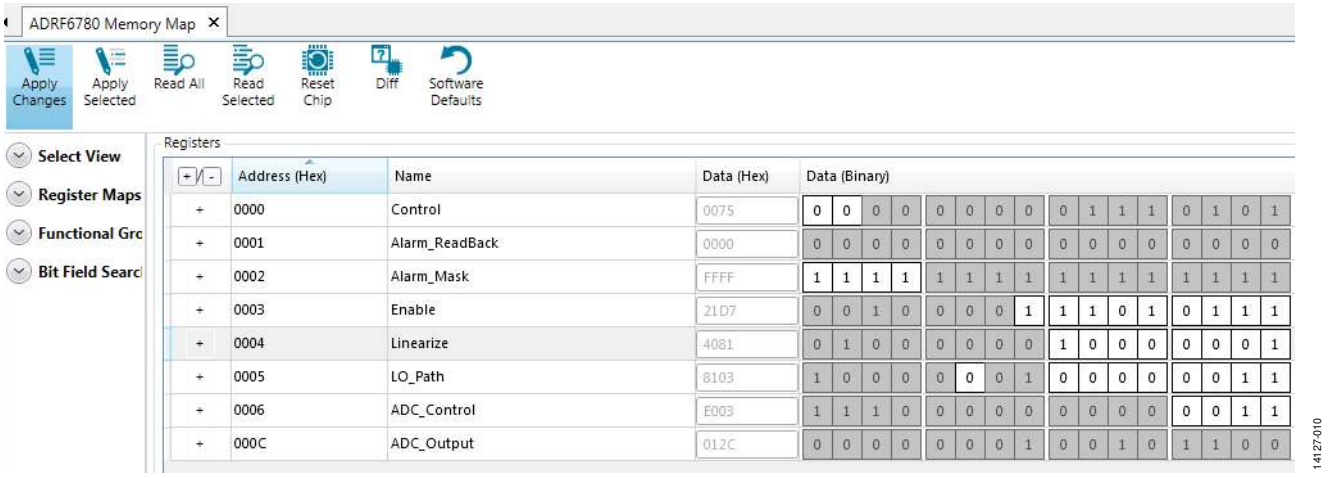


Figure 12. ADRF6780 Memory Map in the ACE Software

SETTING VATT VOLTAGE FOR THE ADRF6780

The ADRF6780-EVALZ comes with the AD5601 nanoDAC. The AD5601 nanoDAC sets the VATT voltage for the VATT pin of the ADRF6780. When the ADRF6780 evaluation board plugin is opened, the voltage can be set in the **Initial Configuration** menu. Note that 2600 mV is the highest gain setting for the devices.

When using an external power supply for the VATT voltage, use the AD5601 nanoDAC plugin to change the voltage or power down the nanoDAC. To open the nanoDAC plugin, select the **AD5601** tab at the top of the ACE software window or double click the **AD5601** button within the **ADRF6780-042654, Rev. A** tab (see Figure 9). Figure 13 shows the AD5601 nanoDAC user interface. The user interface contains two section: the **Power Down Modes** section and the VATT voltage section.

To power up or power down the AD5601 nanoDAC, go to the **Power-Down Modes** section. To use the AD5601 nanoDAC, set the **Power-Down Modes** box to 0. When the VATT voltage is being applied externally, through the test loop, set the **Power-Down Modes** box to 1, 2, or 3. For more information on the different power-down modes of the AD5601 nanoDAC, see the power-down modes section of the AD5601 data sheet.

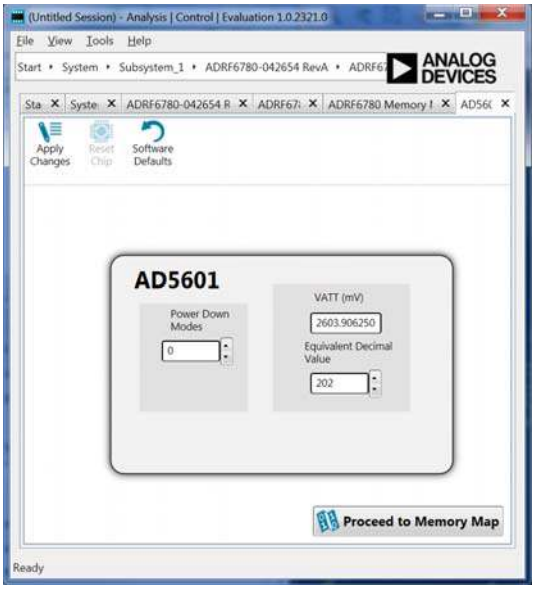


Figure 13. AD5601 nanoDAC User Interface

To set the VATT voltage, type a number in the **VATT (mV)** box or type the corresponding decimal number for an 8-bit register in the **Equivalent Decimal Value** box. The VATT (mV) range available is from 0 mV to 3300 mV. To set the lowest gain for the ADRF6780, set **VATT (mV)** to 0, and to set the highest gain for the ADRF6780, set **VATT (mV)** to 2600. Note that, there is no change in the gain of the ADRF6780 above 2600 mV.

After making any changes to the voltage or the power-down mode, click **Apply Changes** shown in the top left of the ACE software window (see Figure 13). When the **Auto Apply** button is selected in the **ADRF6780-042654, Rev. A** tab, these changes take place automatically; therefore, there is no need to click **Apply Changes**.

TEST RESULTS

When testing the ADRF6780-EVALZ board, the following are the expected results. VATT = 2600 mV was used for both the IF results and the IQ results.

IF RESULTS

Resistors R10 to R13 were taken out for the IF measurements that follow. The hybrids and evaluation board have not been deembedded.

Figure 14 shows the results of an IF input of 2000 MHz at −10 dBm, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 10 GHz for a LO ×1 mode and upper sideband settings.

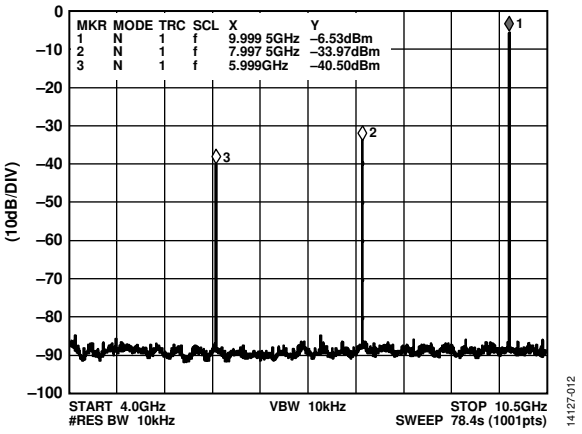


Figure 14. ADRF6780 Results for a LO ×1 Mode with Upper Sideband Settings and Set to IF Mode

Figure 15 shows the graphical user interface (GUI) settings for the results shown in Figure 14.

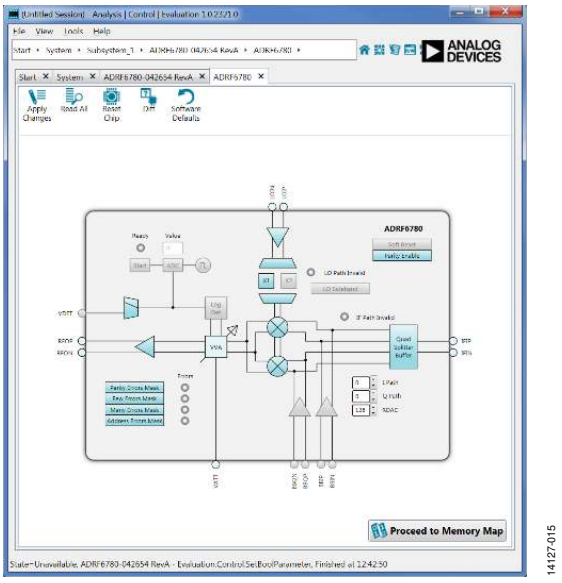


Figure 15. ADRF6780 GUI Settings for a LO in ×1 Mode with Upper Sideband Settings and Set to IF Mode

Figure 16 shows the results of an IF input of 2000 MHz at −10 dBm, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 6 GHz for a LO ×1 mode and lower sideband settings.

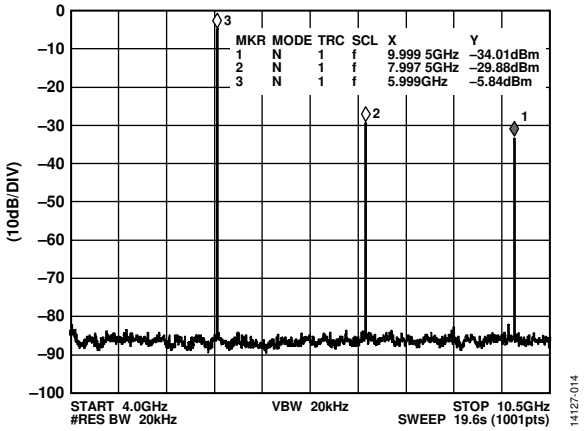


Figure 16. ADRF6780 Results for a LO ×1 Mode with Lower Sideband Settings and Set to IF Mode

Figure 17 shows the GUI settings for the results shown in Figure 16.

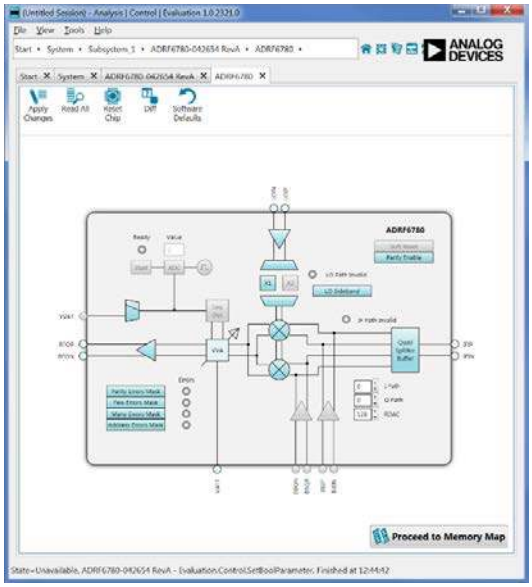


Figure 17. ADRF6780 GUI Settings for a LO in ×1 Mode with Lower Sideband Settings and Set to IF Mode

Figure 18 shows the results of an IF input of 2000 MHz at −10 dBm, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 18 GHz for a LO ×2 mode and lower sideband settings.

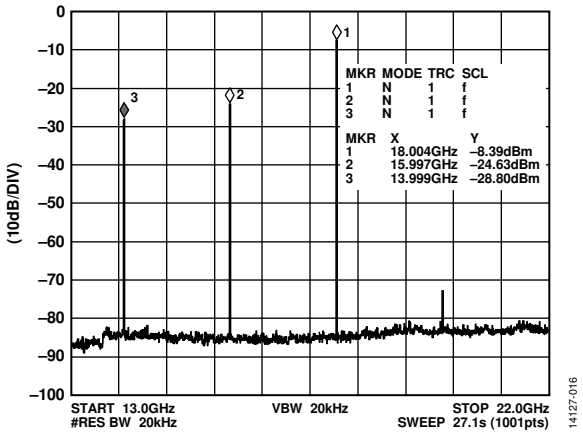


Figure 18. ADRF6780 Results for a LO ×2 Mode with Upper Sideband Settings and Set to IF Mode

Figure 19 shows the GUI settings for the results shown in Figure 18.

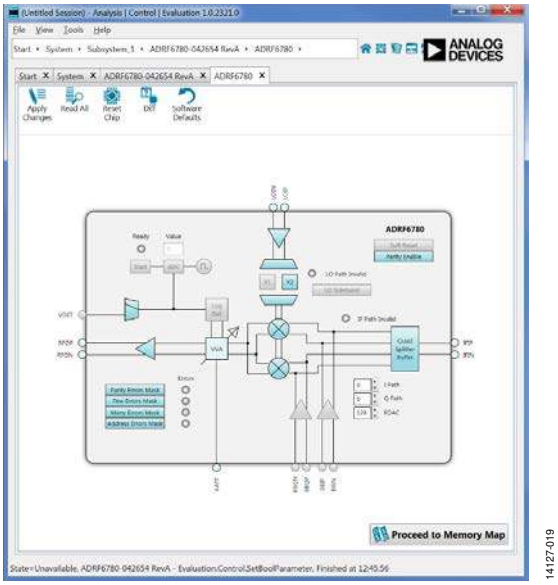


Figure 19. ADRF6780 GUI Settings for a LO ×2 Mode with Upper Sideband Settings and Set to IF Mode

Figure 20 shows the results of an IF input of 2000 MHz at −10 dBm, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 14 GHz for a LO ×2 mode and lower sideband settings.

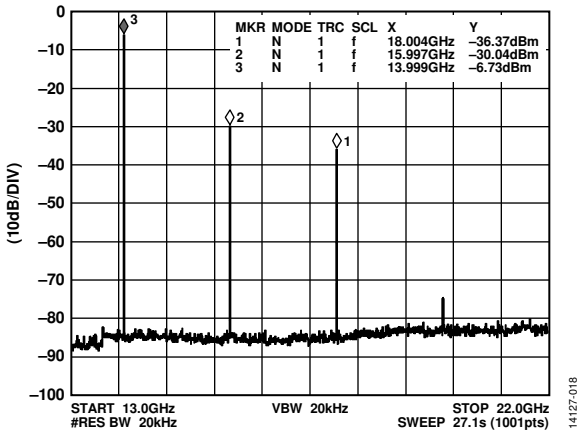


Figure 20. ADRF6780 Results for a LO ×2 Mode with Lower Sideband Settings and Set to IF Mode

Figure 21 shows the GUI settings for the results shown in Figure 20.

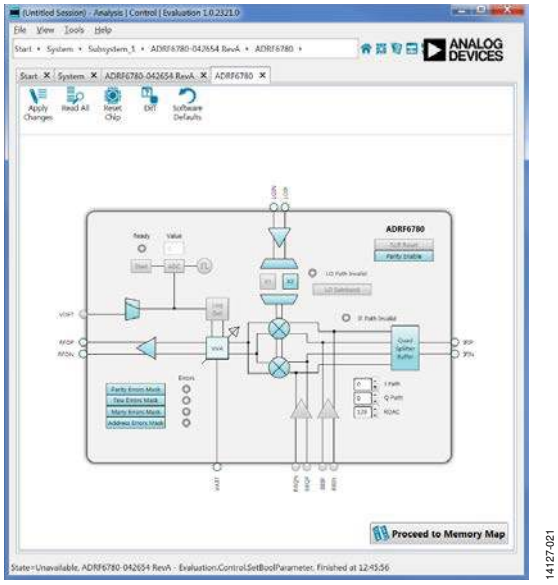


Figure 21. ADRF6780 GUI Settings for a LO ×2 Mode with Lower Sideband Settings and Set to IF Mode

IQ RESULTS

Resistors R10 to R13 were added for the IQ measurements that follow. The hybrids and evaluation board have not been deembedded.

Figure 22 shows the IQ output, lower sideband for a signal of 10 MHz, 160 mV p-p, and 0.5 V common-mode, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 7.99 GHz for a LO ×1 mode and lower sideband settings.

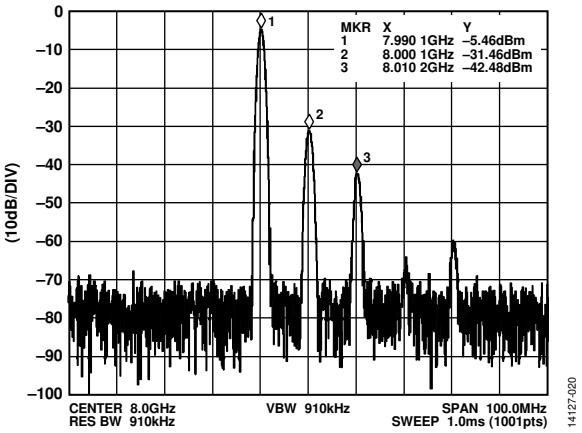


Figure 22. ADRF6780 Results for a LO in ×1 Mode with Lower Sideband Settings and Set to IQ Mode

Figure 23 shows the GUI settings for the results shown in Figure 22.

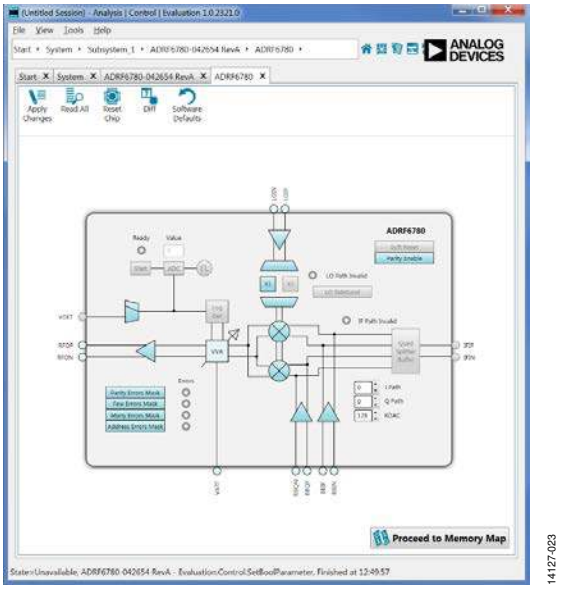


Figure 23. ADRF6780 GUI Settings for a LO in ×1 Mode with Lower Sideband Settings and Set to IQ Mode

Figure 24 shows the IQ output, lower sideband for a signal of 10 MHz, 160 mV p-p, and 0.5 V common-mode, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 8.01 GHz for a LO ×1 mode and upper sideband settings.

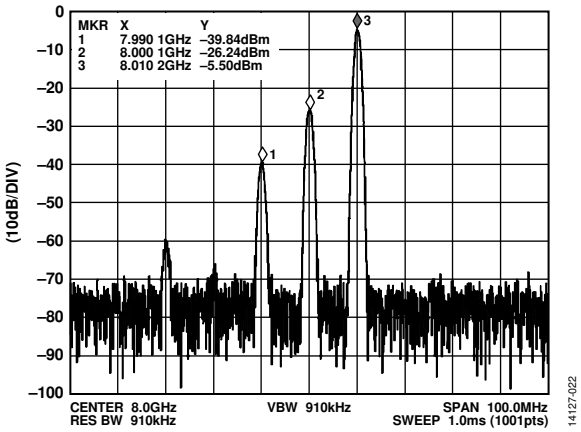


Figure 24. ADRF6780 Results for a LO in ×1 Mode with Upper Sideband Settings and Set to IQ Mode

Figure 25 shows the GUI settings for the results shown in Figure 24.

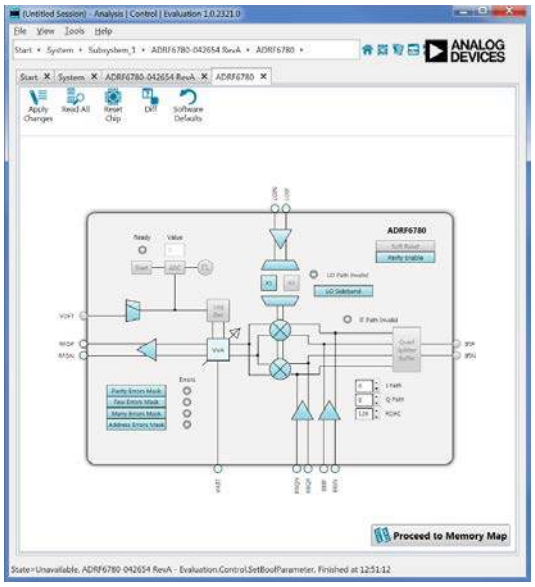


Figure 25. ADRF6780 GUI Settings for a LO in ×1 Mode with Upper Sideband Settings and Set to IQ Mode

Figure 26 shows the IQ output, lower sideband for a signal of 10 MHz, 160 mV p-p, and 0.5 V common-mode, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 15.99 GHz for LO ×2 mode and lower sideband settings.

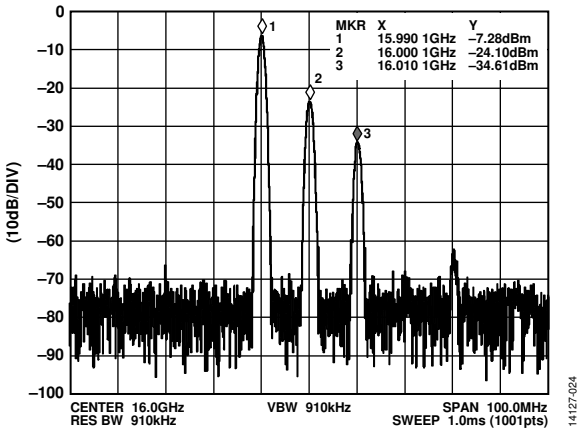


Figure 26. ADRF6780 Results for a LO in ×2 Mode with Lower Sideband Settings and Set to IQ Mode

Figure 27 shows the GUI settings for the results shown in Figure 26.

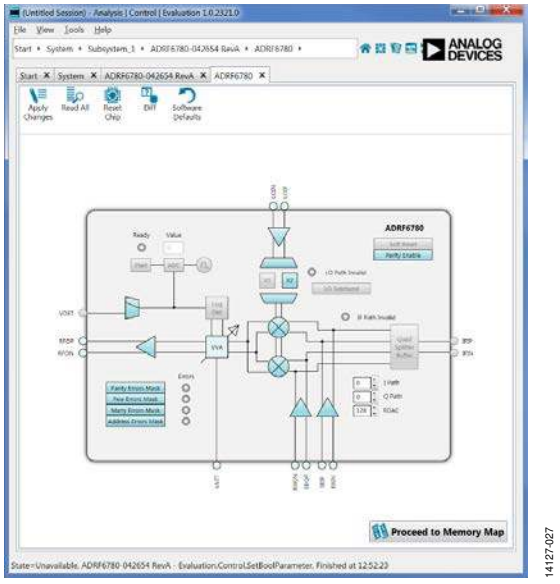


Figure 27. ADRF6780 GUI Settings for a LO in ×2 Mode with Lower Sideband Settings and Set to IQ Mode

Figure 28 shows the IQ output, lower sideband for a signal of 10 MHz, 160 mV p-p, and 0.5 V common-mode, single tone mixed, with an 8 GHz LO at 0 dBm to an RF output of 16.01 GHz for LO ×2 mode and upper sideband settings.

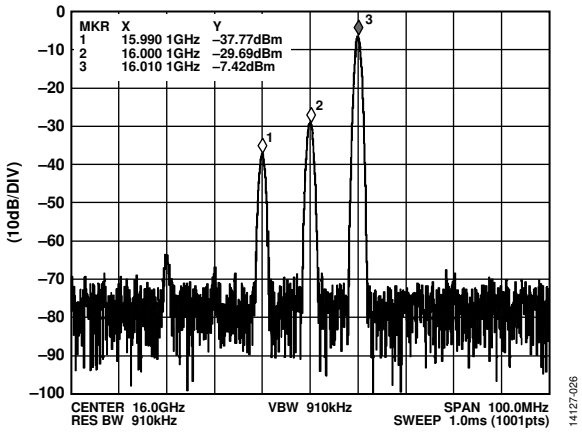


Figure 28. ADRF6780 Results for a LO in ×2 Mode with Upper Sideband Settings and Set to IQ Mode

Figure 29 shows the GUI settings for the results shown in Figure 28.

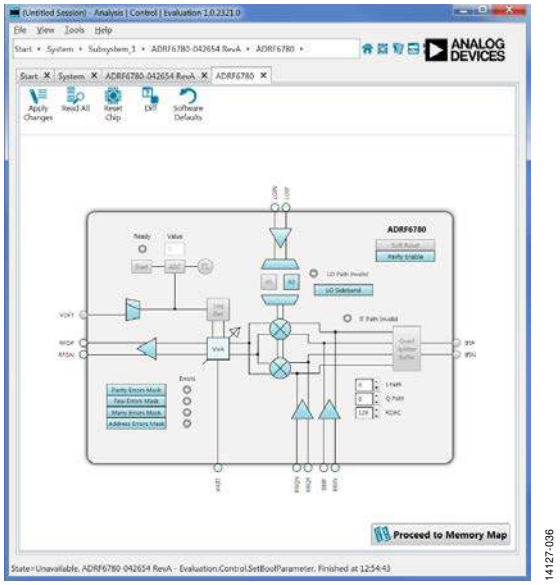


Figure 29. ADRF6780 GUI Settings for a LO in ×2 Mode with Upper Sideband Settings and Set to IQ Mode

EVALUATION BOARD SCHEMATICS AND ARTWORK

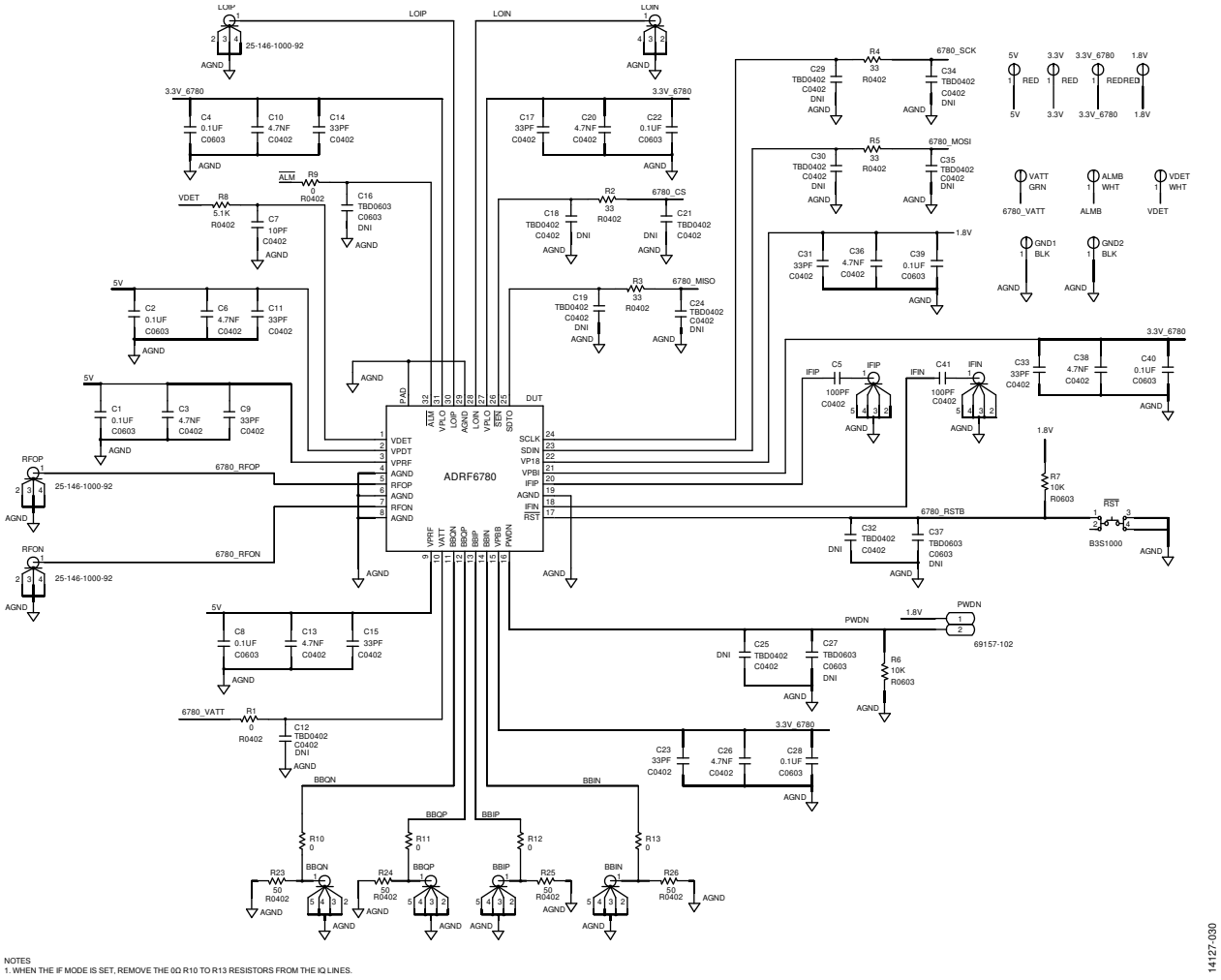


Figure 30. ADRF6780-EVALZ Evaluation Board Schematic, Page 1

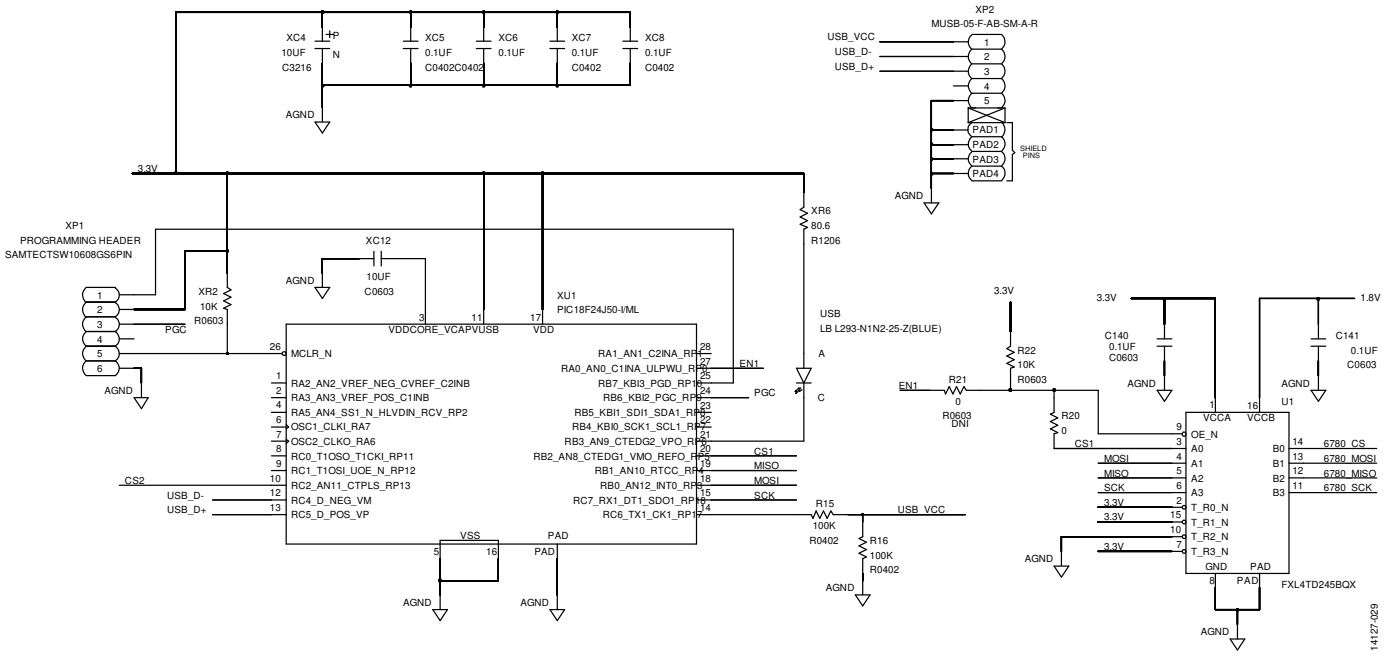
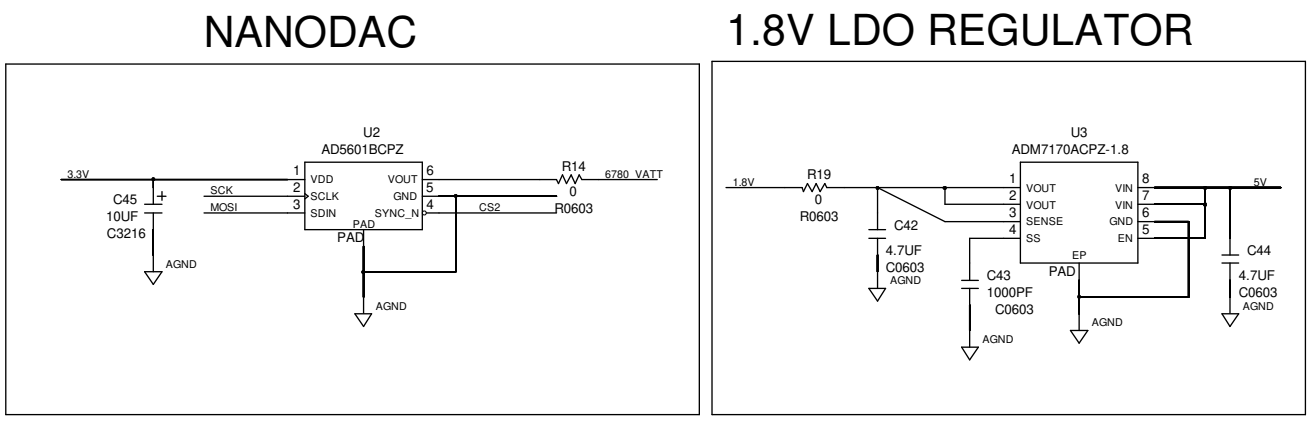


Figure 31. ADRF6780-EVALZ Evaluation Board Schematic, Page 2



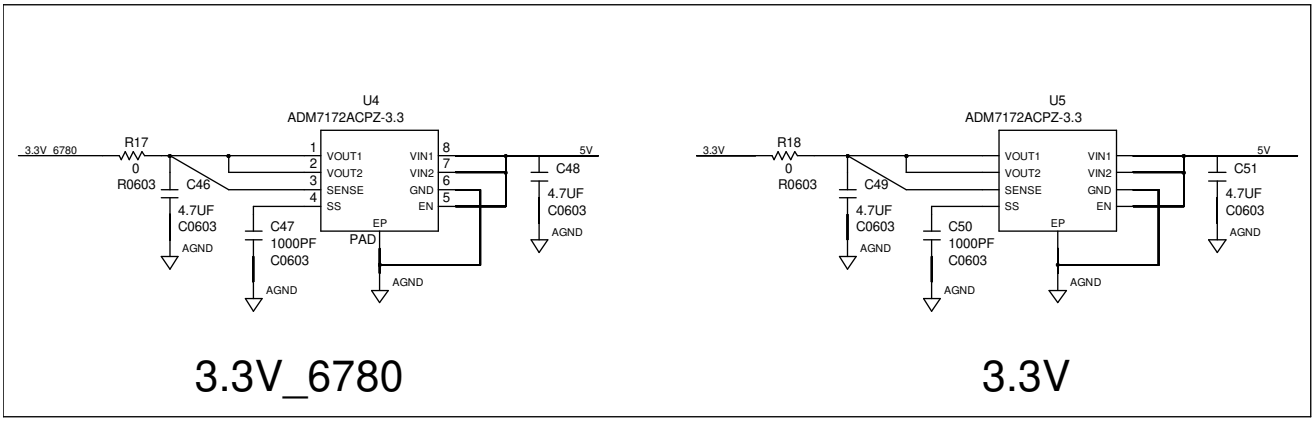


Figure 32. ADRF6780-EVALZ Evaluation Board Schematic, Page 3

ADRF6780-EVALZ EVALUATION BOARD ARTWORK

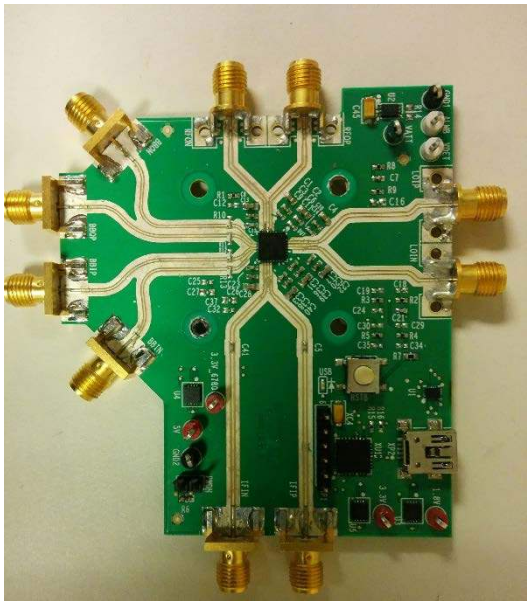


Figure 33. ADRF6780-EVALZ Evaluation Board Top

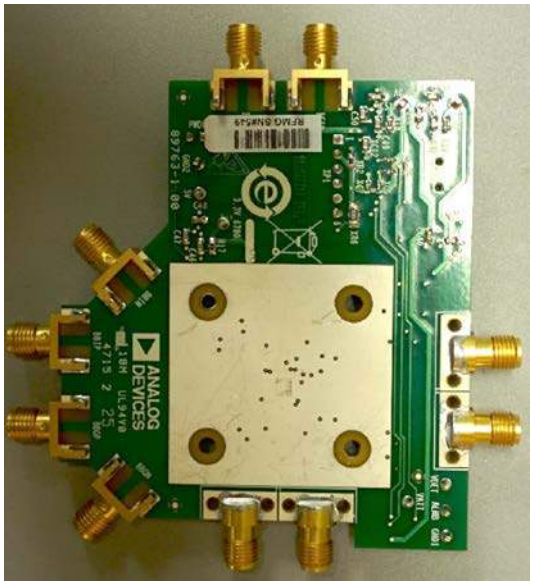


Figure 34. ADRF6780-EVALZ Evaluation Board Bottom

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. ADRF6780-EVALZ Configuration Options

Component	Function	Default Condition
VPLO3.3V, VPDT5V, VPRF5V, VPBB3.3V, VPBI3.3V,1P8V, AGND	Power supplies and ground.	Not applicable
LOIN, LOIP, VDET, RFON, RFOP, BBIN, BBIP, BBQN, BBQN, IFIN, IFIP, VATT	Data and clock.	Not applicable
SCLK, SDIN, SENB, SDTO	SPI.	Not applicable
R2 to R5	33 Ω series resistors for SPI pins.	R2, R3, R4, R5 = 33 Ω (0402)
5V, 3.3V, 3.3V_6780, 1.8V, VDET, ALMB, VATT, GND1 to GND2	Test points.	Not applicable
PWDN	Power-down function.	Apply 1.8 V on PWDN (Pin2) jumper to power down the device
R1, R9, R14, R15, R17 to R20, XR2, XR6	Shorts or power supply decoupling resistors.	R1, R9, R17, R18, R19 = 0 Ω (0402), R8 = 5.1 kΩ (0402), R15 = 100 kΩ (0402), R14, R20 = 0 Ω (0402), XR2 = 10 kΩ (0603), XR6 = 80.6 Ω (1206)
R6, R7, R16, R22	Pull-up or pull-down resistors.	R6, R7, R22 = 10 kΩ (0603), R16 = 100 kΩ (0402)
C1 to C4, C6, C7, C8 to C11, C13 to C15, C17, C20, C22, C23, C26, C28, C31, C33, C36, C38 to C40, C42 to C51, XC12, XC4 to XC8, C140, C141	These capacitors provide the required decoupling of the supply related pins.	XC4, C45 = 10 µF (3216), XC12 = 10 µF (0603), C42, C44, C46, C48, C49, C51 = 4.7 µF (0603), C1, C2, C4, C8, C22, C28, C39, C40 = 0.1 µF (0603), XC5, XC6, XC7, XC8 = 0.1 µF (0402), C3, C6, C10, C13, C20, C26, C36, C38 = 4.7 nF (0402), C43, C47, C50 = 1000 pF (0603), C9, C11, C14, C15, C17, C23, C31, C33 = 33 pF (0402), C7 = 10 pF (0402), C140, C141 = 0.1 µF (0603)
R10 to R13	Remove when using IF inputs (IF mode).	R10, R11, R12, R13 = 0 Ω (0402)
R23 to R26	These resistors provide a 50 Ω termination for a baseband input data.	R23, R24, R25, R26 = 50 Ω (0402)
C5, C41	AC coupling capacitors.	C5, C41 = 100 pF (0402)
C21	CS decoupling resistor.	C21 = 100 pF (0402)
C12, C16, C18, C19, C24, C25, C27, C29, C30, C32, C34, C35, C37, R21	Do not install (DNI).	C16, C24, C34, C35 = (0402), C27, C37, R21 = (0603), C12, C18, C19, C25 = (0402), C29, C30, C32 = (0402)
XP1	Programming header.	Not applicable
XP2	Mini USB connector.	Connect the mini USB cable to XP2 to interface with the SPI
RSTB	Reset button.	Click RSTB to reset the device
USB	Blue LED.	Is blue when the USB is connected to XP2, and the PC and the ADRF6780 evaluation board is powered on with a 5 V supply
XU1	Microcontroller.	PIC18F24J50
U1	Level shifter.	FXL4TD245BQX

Component	Function	Default Condition
U3 to U5	3.3 V and 1.8 V regulators.	ADM7170 (U3) = 1.8 V regulator, ADM7172 (U4) = 3.3 V regulator, ADM7172 (U5) = 3.3 V regulator for ADRF6780
U2	AD5601 nanoDAC.	Not applicable
DUT	ADRF6780, device under test.	Not applicable

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG14127-0-1/19(A)

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