

Description

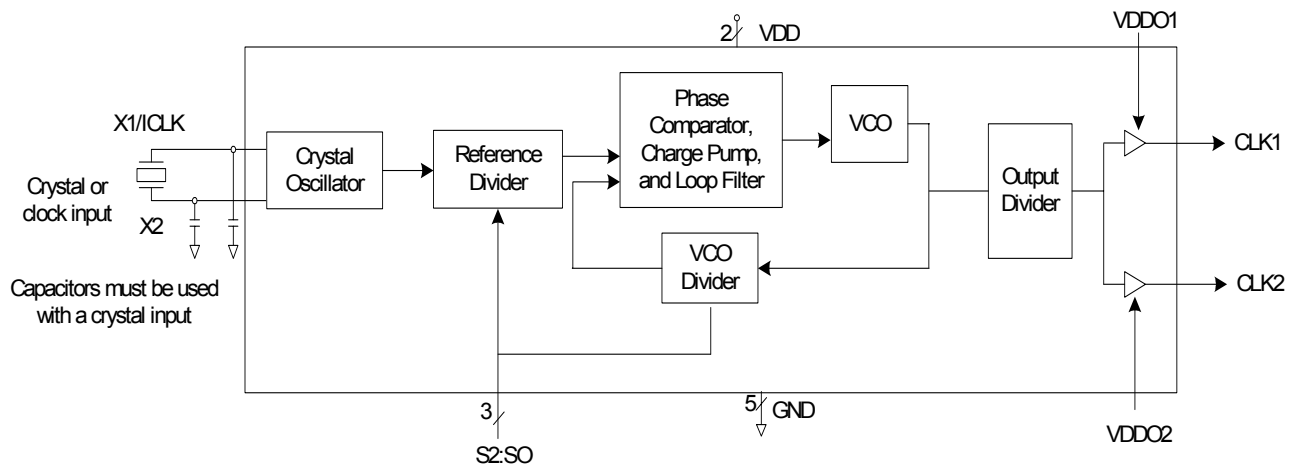
The ICS613 is a low cost, low phase noise, high performance clock synthesizer for any applications that require low phase noise and low jitter. It is IDT's lowest phase noise multiplier. Using IDT's patented analog and digital Phase Locked Loop (PLL) techniques, the chip can accept a 25 MHz crystal or clock input, and produces output clocks up to 157.5 MHz.

The chip has separate power supplies for the clock outputs, allowing each output to be run at different voltages. It also allows the core of the chip to operate at 3.3 V, while the output clocks run at either 2.5 V or 3.3 V.

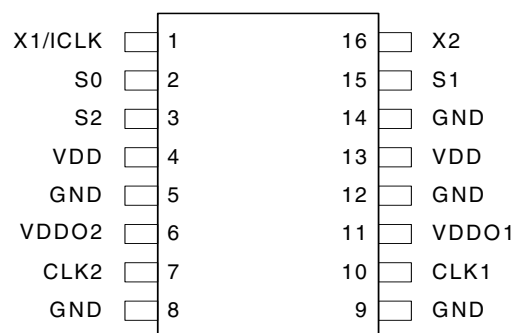
Features

- Packaged in 16 pin SOIC
- Pb (lead) free package
- Uses a fundamental 25 MHz crystal or clock
- Operating voltage of 3.3 V
- Separate output voltage supplies which can run at 2.5 V or 3.3 V
- Output clocks up to 157.5 MHz
- Low phase noise: -110 dBc/Hz at 10 kHz
- Low jitter of 36 ps (one sigma)
- Advanced, low power, sub-micron CMOS process

Block Diagram



Pin Assignment



16 Pin (150 mil) SOIC

Clock Select Table

| S2 | S1 | S0 | Input | Output (CLK1 and CLK2) |
|----|----|----|-------|------------------------|
| 0 | 0 | 0 | 25 | 125 |
| 0 | 0 | 1 | 25 | 156.25 |
| 0 | 1 | 0 | 25 | 143.75 |
| 0 | 1 | 1 | 25 | 150 |
| 1 | 0 | 0 | 25 | 146.875 |
| 1 | 0 | 1 | 25 | 157.5 |
| 1 | 1 | 0 | 25 | 140 |
| 1 | 1 | 1 | 25 | 156.25 |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|---|
| 1 | XI/ICLK | Input | Crystal Connection. Connect to a 25 MHz crystal or clock. |
| 2 | S0 | Input | Select pin 0. Internal pull-down. |
| 3 | S2 | Input | Select pin 2. Internal pull-down. |
| 4 | VDD | Power | Connect to +3.3V. Must be the same as pin 13. |
| 5 | GND | Power | Connect to ground. |
| 6 | VDDO2 | Power | Output VDD for CLK2. Connect to either +2.5V or +3.3V. |
| 7 | CLK2 | Output | CLK2 output. Frequency based on table above. |
| 8 | GND | Power | Connect to ground. |
| 9 | GND | Power | Connect to ground. |
| 10 | CLK1 | Output | CLK1 output. Frequency based on table above. |
| 11 | VDDO1 | Power | Output VDD for CLK1. Connect to either +2.5V or +3.3V. |
| 12 | GND | Power | Connect to ground. |
| 13 | VDD | Power | Connect to +3.3V. Must be the same as pin 4. |
| 14 | GND | Power | Connect to ground. |
| 15 | S1 | Input | Select pin 1. Internal pull-up. |
| 16 | X2 | Input | Crystal Connection. Connect to a 25 MHz crystal. Leave unconnected for clock input. |

External Component Selection

The ICS613 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μ F should be connected between VDD and GND pairs on pins 4 and 5, pins 6 and 8, pins 11 and 9, and pins 13 and 14 as close to the ICS613 as possible. For optimum device performance, the decoupling capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance) place a 33 Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω .

Crystal Tuning Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground.

These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal $(C_L - 6\text{pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF.

Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF $[(16-6) \times 2 = 20]$.

Reducing Jitter and Phase Noise

For applications that only require one output, jitter and phase noise can be reduced by tying the unused VDDO to ground. This will stop the output clock low which will result in less switching noise on the active output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS613. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|-------------------------------|-------------------|
| Supply Voltage, VDD | 7V |
| All Inputs and Outputs | -0.5V to VDD+0.5V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature | 0 | – | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | | +3.45 | V |

DC Electrical Characteristics

VDD=3.3V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|-----------------|--------------------------|---------|------|------|-------|
| Operating Voltage | VDD | | 3.15 | | 3.45 | V |
| Output Voltage | VDDO | | 2.375 | | VDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |
| Output High Voltage (CMOS Level) | V _{OH} | I _{OH} = -4 mA | VDD-0.4 | | | V |
| Input High Voltage (S2:S0) | V _{IH} | | 2.5 | | | V |
| Input Low Voltage (S2:S0) | V _{IL} | | | | 0.5 | V |
| Input High Voltage (ICLK) | V _{IH} | | 1.7 | | | V |
| Input Low Voltage (ICLK) | V _{IL} | | | | 0.7 | V |
| Operating Supply Current | I _{DD} | No load | | 27 | | mA |
| Short Circuit Current | I _{OS} | | | ±50 | | mA |

AC Electrical Characteristics

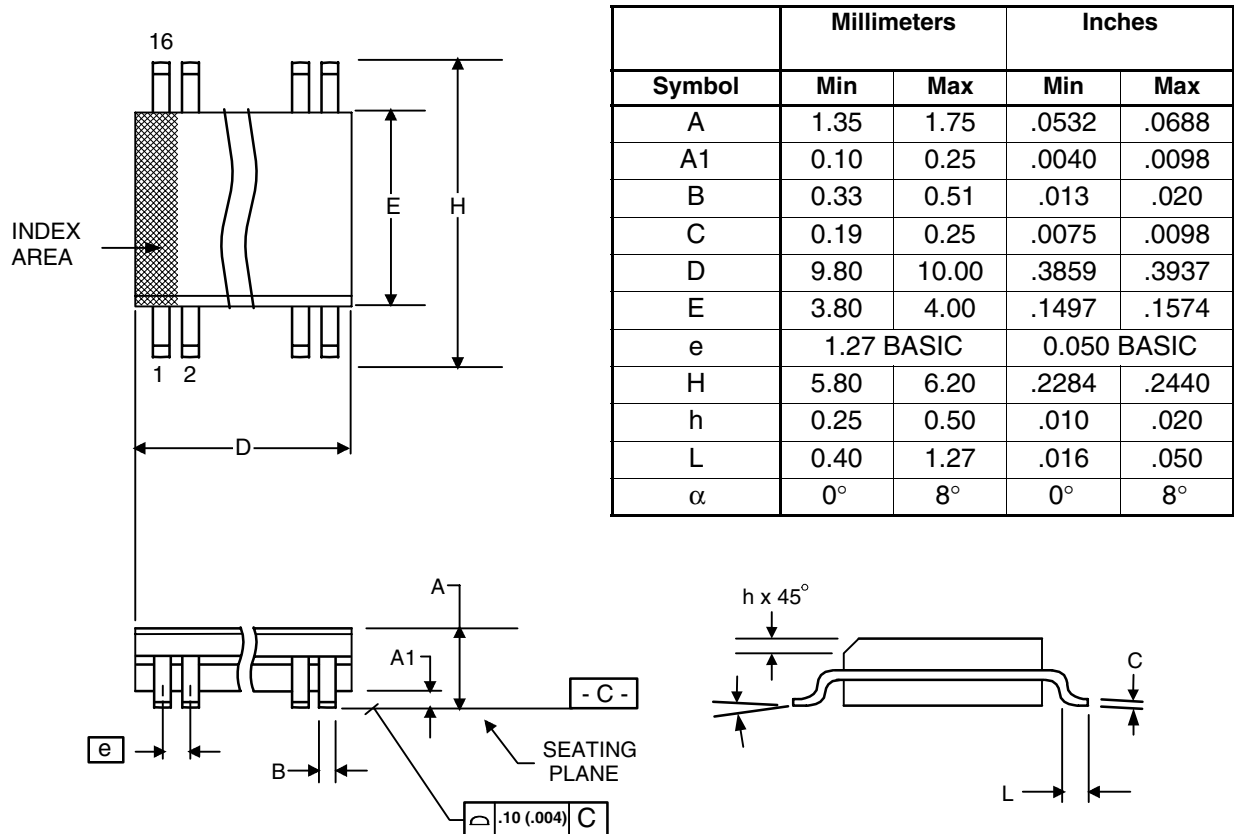
VDD = 3.3V ±5%, Ambient Temperature 0 to +70° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------|------------------|---|------|------|-------|-------|
| Input Frequency | f _{in} | | | 25 | | MHz |
| Output Frequency | f _{out} | | 125 | | 157.5 | MHz |
| Output Rise Time | t _{OR} | 20% to 80%, C _L =15 pF, VDD=3.3 V | | 700 | | ps |
| Output Fall Time | t _{OF} | 80% to 20%, C _L =15 pF, VDD=3.3 V | | 700 | | ps |
| Output Rise Time | t _{OR} | 20% to 80%, C _L =15 pF, VDDO's=2.5 V | | | 1.0 | ns |
| Output Fall Time | t _{OF} | 80% to 20%, C _L =15 pF, VDDO's=2.5 V | | | 1.0 | ns |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|----------|-----------------------------|------|----------|----------|--------|
| Output Clock Duty Cycle | t_D | At VDDO's/2, $C_L=15$ pF | 45 | 50 | 55 | % |
| Maximum Output Jitter, short term | t_J | $C_L=15$ pF, 125 MHz output | | ± 30 | ± 60 | ps |
| Maximum one sigma jitter | t_{SJ} | $C_L=15$ pF, 125 MHz output | | 8 | 20 | ps |
| Phase Noise, relative to carrier, 125 MHz | | 100 Hz offset | | -90 | | dBc/Hz |
| Phase Noise, relative to carrier, 125 MHz | | 1 kHz offset | | -115 | | dBc/Hz |
| Phase Noise, relative to carrier, 125 MHz | | 10 kHz offset | | -120 | | dBc/Hz |
| Phase Noise, relative to carrier, 125 MHz | | 100 kHz offset | | -115 | | dBc/Hz |
| Skew | | VDDO1=VDDO2 | | 0 | 250 | ps |

Package Outline and Package Dimensions (16 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-----------|--------------------|-------------|-------------|
| 613MLF | ICS613MLF | Tubes | 16 pin SOIC | 0 to +70° C |
| 613MLFT | ICS613MLF | Tape and Reel | 16 pin SOIC | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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