HARRIS HM-6561

256 x 4 CMOS RAM

Features

- HM-6100 Compatible
- Low Standby Power ..... 50µW Max.
- Low Operating Power ..... 20mW/MHz Max.
- Fast Access Time ..... 220ns Max.
- Data Retention Voltage ..... 2.0V Min.
- TTL Compatible In/Out
- High Output Drive - 1 TTL Loads
- On Chip Address Registers
- Common Data In/Out
- Three-State Outputs
- Easy Microprocessor Interfacing
- Wide Operating Temperature Ranges:
  - ▸ HM-6561-5 ..... 0°C to +70°C
  - ▸ HM-6561-9 ..... -40°C to +85°C
  - ▸ HM-6561-8 ..... -55°C to +125°C

Description

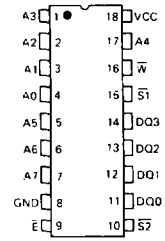
The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

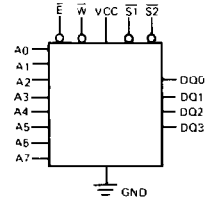
Pinout

TOP VIEW

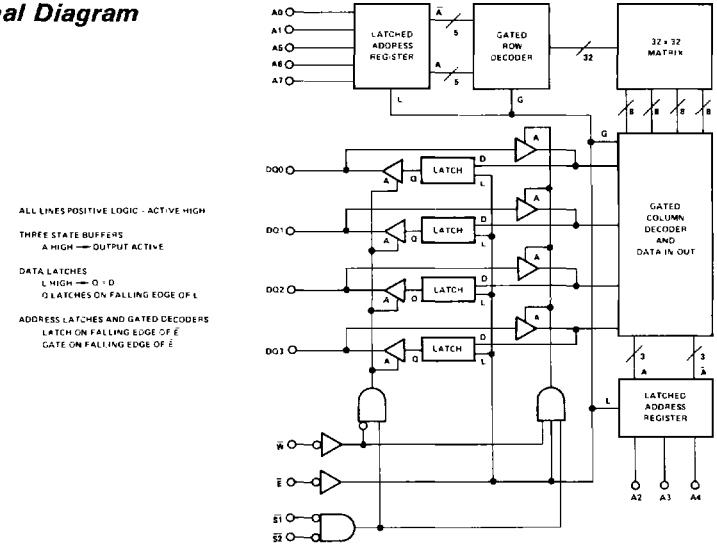


A-Address Input
E-Chip Enable
S-Chip Select
W-Write Enable
DQ-Data In/Out

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 74°C/W (CERDIP Package)
Gate Count ..... 1944 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6561B-9 ..... -40°C to +85°C
HM-6561B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6561B-9 -40°C to +85°C
T_A = HM-6561B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6561B-9 -40°C to +85°C
T_A = HM-6561B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	220	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	220	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	120	ns	(Notes 2, 4)
(4) TSHQZ	Chip Select Output Disable Time	-	120	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	220	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(9) TDVWH	Data Setup Time	100	-	ns	(Notes 1, 4)
(10) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(11) TWLDV	Write Data Delay Time	20	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	120	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	120	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	120	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	120	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	120	-	ns	(Notes 1, 4)
(17) TWLSL	Early Output High Z Time	0	-	ns	(Notes 1, 4)
(18) TSHWH	Late Output High Z Time	0	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	320	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 74°C/W (CERDIP Package)
Gate Count ..... 1944 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6561-9 ..... -40°C to +85°C
HM-6561-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6561-9 -40°C to +85°C
T_A = HM-6561-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	10	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6561-9 -40°C to +85°C
T_A = HM-6561-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	300	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	150	ns	(Notes 2, 4)
(4) TSHQZ	Chip Select Output Disable Time	-	150	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(9) TDVWH	Data Setup Time	150	-	ns	(Notes 1, 4)
(10) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(11) TWLDV	Write Data Delay Time	30	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	180	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	180	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	180	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	180	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	180	-	ns	(Notes 1, 4)
(17) TWLSL	Early Output High Z Time	0	-	ns	(Notes 1, 4)
(18) TSHWH	Late Output High Z Time	0	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	400	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 74°C/W (CERDIP Package)
Gate Count ..... 1944 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6561-5 ..... 0°C to +70°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6561-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
ICCDR	Data Retention Supply Current	-	100	µA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.2mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CIO	Input/Output Capacitance (Note 2)	10	pF	VIO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

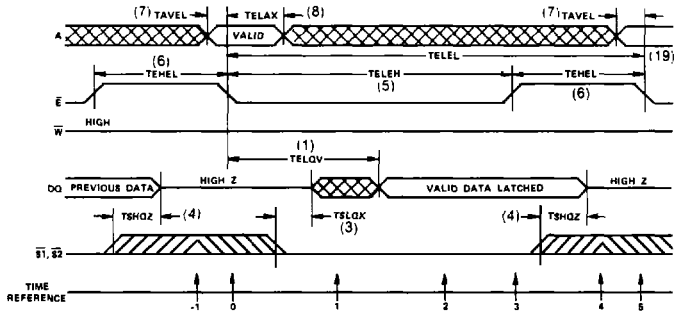
A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6561-5 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	350	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	360	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	180	ns	(Notes 2, 4)
(4) TSHQZ	Chip Select Output Disable Time	-	180	ns	(Notes 2, 4)
(5) TELEH	Chip Enable Pulse Negative Width	350	-	ns	(Notes 1, 4)
(6) TEHEL	Chip Enable Pulse Positive Width	150	-	ns	(Notes 1, 4)
(7) TAVEL	Address Setup Time	10	-	ns	(Notes 1, 4)
(8) TELAX	Address Hold Time	70	-	ns	(Notes 1, 4)
(9) TDVWH	Data Setup Time	170	-	ns	(Notes 1, 4)
(10) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(11) TWLDV	Write Data Delay Time	40	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	210	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	210	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	210	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	210	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	210	-	ns	(Notes 1, 4)
(17) TWLSL	Early Output High Z Time	0	-	ns	(Notes 1, 4)
(18) TSHWH	Late Output High Z Time	0	-	ns	(Notes 1, 4)
(19) TELEL	Read or Write Cycle Time	500	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V, Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle



TRUTH TABLE

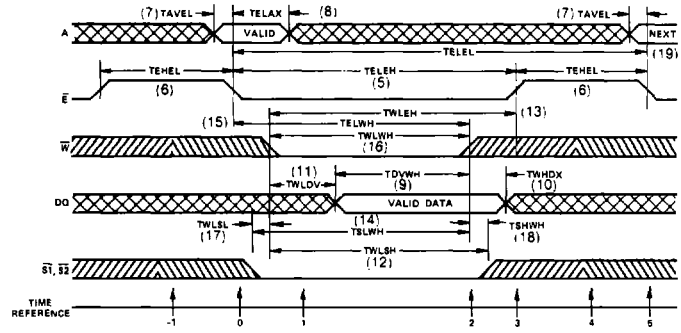
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	Memory Disabled
0	↘	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↗	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTES: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	Memory Disabled
0	↘	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↗	X	V	Data In is Written
3	↗	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↘	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTES: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

If one or both selects are high until $\overline{W}$ falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in Case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH TWLSL TSHWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH TWLSL TSHWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.