# SPECTRALINEAR

# CY28419

# Clock Synthesizer with Differential SRC and CPU Outputs

## Features

- **CK409B-compliant**
- **Supports Intel Pentium® 4-type CPUs**
- **Selectable CPU frequencies**
- **3.3V power supply**
- **Ten copies of PCI clocks**
- **Two copies 48 MHz clock**
- **Five copies of 3V66 with one optional VCH**

- **Four differential CPU clock pairs**
- **One differential SRC clock**
- **I²C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **56-pin SSOP package**

| CPU | SRC | 3V66 | PCI | REF | 48M |
|-----|-----|------|-----|-----|-----|
| x 4 | x 1 | x 5 | x 10 | x 2 | x 2 |

## Block Diagram



## Pin Configuration [1]



SSOP-56
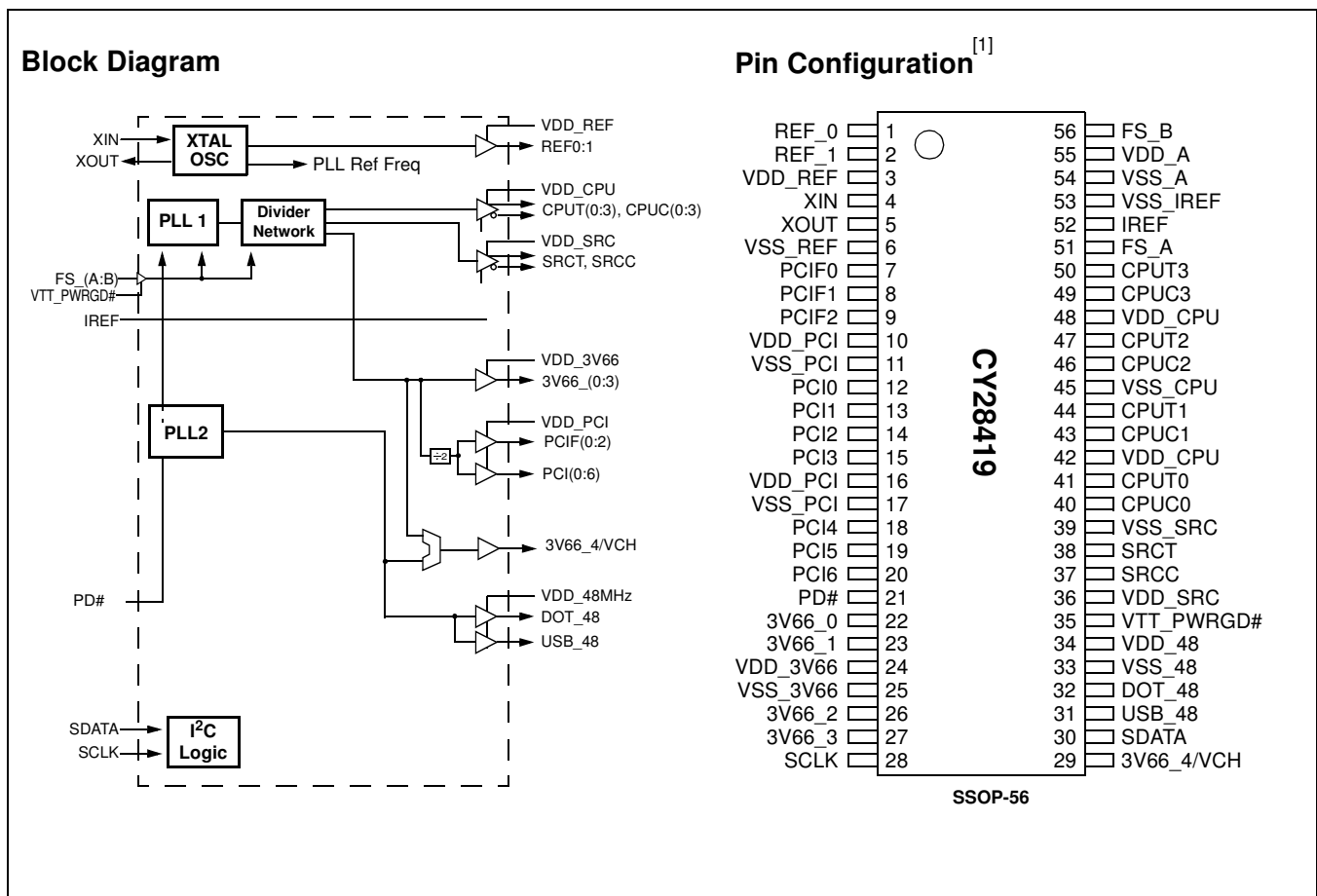
**Note:**
1. Signals marked with [*] and [**] have internal pull-up and pull-down resistors, respectively.

# CY28419

## Pin Description

| Pin No. | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1,2 | REF(0:1) | O, SE | **Reference Clock**. 3.3V 14.318-Mz clock output. |
| 4 | XIN | I | **Crystal Connection or External Reference Frequency Input**. This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| 5 | XOUT | O, SE | **Crystal Connection**. Connection for an external 14.318-MHz crystal output. |
| 41,44,47,50 | CPUT(0:3) | O, DIF | **CPU Clock Output**. Differential CPU clock outputs. See *Table 1* for frequency configuration. |
| 40,43,46,49 | CPUC(0:3) | O, DIF | **CPU Clock Output**. Differential CPU clock outputs. See *Table 1* for frequency configuration. |
| 38, 37 | SRCT, SRCC | O, DIF | **Differential serial reference clock**. |
| 22,23,26,27 | 3V66(3:0) | O, SE | **66 MHz Clock Output**. 3.3V 66-MHz clock from internal VCO. |
| 29 | 3V66_4VCH | O, SE | **48/66 MHz Clock Output**. 3.3V selectable through SMBus to be 66 or 48 MHz. |
| 7,8,9 | PCIF(0:2) | O, SE | **Free Running PCI Output**. 33-MHz clocks divided down from 3V66. |
| 12,13,14,15, 18,19,20 | PCI(0:6) | O, SE | *PCI Clock Output*. 33-MHz clocks divided down from 3V66. |
| 31, | USB_48 | O, SE | **Fixed 48 MHz clock output**. |
| 32 | DOT_48 | O, SE | **Fixed 48 MHz clock output**. |
| 51,56 | FS_A, FS_B | I | **3.3V LVTTL input for CPU frequency selection**. |
| 52 | IREF | I | **Current Reference**. A precision resistor is attached to this pin which is connected to the internal current reference. |
| 21 | PD# | I, PU | **3.3V LVTTL input for power-down# active LOW**. |
| 35 | VTT_PWRGD# | I | **3.3V LVTTL input is a level-sensitive strobe used to latch the FS0 input** (active LOW). |
| 30 | SDATA | I/O | **SMBus-compatible SDATA**. |
| 28 | SCLK | I | **SMBus-compatible SCLOCK**. |
| 53 | VSS_IREF | GND | **Ground for current reference**. |
| 55 | VDD_A | PWR | **3.3V power supply for PLL**. |
| 54 | VSS_A | GND | **Ground for PLL**. |
| 42,48 | VDD_CPU | PWR | **3.3V power supply for outputs**. |
| 45 | VSS_CPU | GND | **Ground for outputs**. |
| 36 | VDD_SRC | PWR | **3.3V power supply for outputs**. |
| 39 | VSS_SRC | GND | **Ground for outputs**. |
| 34 | VDD_48 | PWR | **3.3V power supply for outputs**. |
| 33 | VSS_48 | GND | **Ground for outputs**. |
| 10,16 | VDD_PCI | PWR | **3.3V power supply for outputs**. |
| 11,17 | VSS_PCI | GND | **Ground for outputs**. |
| 24 | VDD_3V66 | PWR | **3.3V power supply for outputs**. |
| 25 | VSS_3V66 | GND | **Ground for outputs**. |
| 3 | VDD_REF | PWR | **3.3V power supply for outputs**. |
| 6 | VSS_REF | GND | **Ground for outputs**. |

## Frequency Select Pins (FS_A, FS_B)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A and FS_B inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A and FS_B input values. For all logic levels of FS_A and FS_B except MID, VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled low, all further VTT_PWRGD#, FS_A and FS_B transitions will be ignored. In the case where FS_B is at mid level when VTT_PWRGD# is sampled low, the clock chip will assume "Test Clock Mode". Once "Test Clock Mode" has been invoked, all further FS_B transitions will be ignored and FS_A will asynchronously select between the Hi-Z and REF/N mode. Exiting test mode is accomplished by cycling power with FS_B in a high or low state.

**Table 1. Frequency Select Table (FS_A FS_B)**

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|-----|-----|------|----------|------|------|---------|
| 0 | 0 | 100 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | MID | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N | REF/N |
| 0 | 1 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 133 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 1 | 166 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | MID | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

**Table 2. Frequency Select Table (FS_A FS_B) SMBus Bit 5 of Byte 6 = 1**

| FS_A | FS_B | CPU | SRC | 3V66 | PCIF/PCI | REF0 | REF1 | USB/DOT |
|------|------|-----|-----|------|----------|------|------|---------|
| 0 | 0 | 200 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 0 | 1 | 400 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 0 | 266 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |
| 1 | 1 | 333 MHz | 100/200 MHz | 66 MHz | 33 MHz | 14.3 MHz | 14.31 MHz | 48 MHz |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3. Command Code Definition**

| Bit | Description |
|-----|-------------|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000' |

**Table 4. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|------|-------------|------|-------------|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '00000000' stands for block operation | 11:18 | Command Code – 8 bits '00000000' stands for block operation |

**Table 4.  Block Read and Block Write Protocol** (continued)

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 1 – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge from master |
| .... | ...................... | 39:46 | Data byte from slave – 8 bits |
| .... | Data Byte (N–1) –8 bits | 47 | Acknowledge from master |
| .... | Acknowledge from slave | 48:55 | Data byte from slave – 8 bits |
| .... | Data Byte N –8 bits | 56 | Acknowledge from master |
| .... | Acknowledge from slave | .... | Data byte N from slave – 8 bits |
| .... | Stop | .... | Acknowledge from master |
| | | .... | Stop |

**Table 5.  Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | 11:18 | Command Code – 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave – 8 bits |
| | | 38 | Acknowledge from master |
| | | 39 | Stop |

**Byte 0: Control Register 0**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 1 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 1 | Reserved | Reserved |
| 1 | Externally Selected | FS_B | FS_B reflects the value of the FS_B pin sampled on power-up. 0 = FS_B low at power-up |
| 0 | Externally Selected | FS_A | FS_A reflects the value of the FS_A pin sampled on power-up. 0 = FS_A low at power-up |

**Byte 1: Control Register 1**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | SRCT, SRCC | Allow control of SRCT/C with assertion of PCI_STP# 0 = Free Running, 1 = Stopped with PCI_STP# |
| 6 | 1 | SRCT, SRCC | SRCT/C Output Enable 0 = Disabled (three-state), 1 = Enabled |
| 5 | 1 | Reserved | Reserved |
| 4 | 1 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 1 | CPUT2, CPUC2 | CPUT/C2 Output Enable 0 = Disabled (three-state), 1 = Enabled |
| 1 | 1 | CPUT1, CPUC1 | CPUT/C1 Output Enable, 0 = Disabled (three-state), 1 = Enabled |
| 0 | 1 | CPUT0, CPUC0 | CPUT/C0 Output Enable 0 = Disabled (three-state), 1 = Enabled |

**Byte 2: Control Register 2**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | SRCT, SRCC | SRCT/C Pwrdwn drive mode 0 = Driven in power-down, 1 = Three-state in power-down |
| 6 | 0 | SRCT, SRCC | SRCT/C Stop drive mode 0 = Driven in PCI_STP, 1 = Three-state in power-down |
| 5 | 0 | CPUT2, CPUC2 | CPUT/C2 Pwrdwn drive mode 0 = Driven in power-down, 1 = Three-state in power-down |
| 4 | 0 | CPUT1, CPUC1 | CPUT/C1 Pwrdwn drive mode 0 = Driven in power-down, 1 = Three-state in power-down |
| 3 | 0 | CPUT0, CPUC0 | CPUT/C0 Pwrdwn drive mode 0 = Driven in power-down, 1 = Three-state in power-down |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Byte 3: Control Register 3**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | All PCI and SRC Clock outputs except PCIF and SRC clocks set to free-running | PCI_STP Control. 0 = SW PCI_STP not enabled and only the PCI_STP# pin will stop the PCI stop enabled outputs, 1 = the PCI_STP function is enabled and the stop enabled outputs will be stopped in a synchronous manner with no short pulses. |
| 6 | 1 | PCI6 | PCI6 Output Enable 0 = Disabled, 1 = Enabled |
| 5 | 1 | PCI5 | PCI5 Output Enable 0 = Disabled, 1 = Enabled |
| 4 | 1 | PCI4 | PCI4 Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 1 | PCI3 | PCI3 Output Enable 0 = Disabled, 1 = Enabled |
| 2 | 1 | PCI2 | PCI2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | PCI1 | PCI1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | PCI0 | PCI0 Output Enable 0 = Disabled, 1 = Enabled |

**Byte 4: Control Register 4**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | USB_ 48MHz | USB_48 Drive Strength 0 = High drive strength, 1 = Normal drive strength |
| 6 | 1 | USB_ 48MHz | USB_48 Output Enable 0 = Disabled, 1 = Enabled |
| 5 | 0 | PCIF2 | Allow control of PCIF2 with assertion of PCI_STP# 0 = Free Running, 1 = Stopped with PCI_STP# |
| 4 | 0 | PCIF1 | Allow control of PCIF1 with assertion of PCI_STP# 0 = Free Running, 1 = Stopped with PCI_STP# |
| 3 | 0 | PCIF0 | Allow control of PCIF0 with assertion of PCI_STP# 0 = Free Running, 1 = Stopped with PCI_STP# |
| 2 | 1 | PCIF2 | PCIF2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | PCIF1 | PCIF1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | PCIF0 | PCIF0 Output Enable 0 = Disabled, 1 = Enabled |

**Byte 5: Control Register 5**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | DOT_48 | DOT_48 Output Enable 0 = Disabled, 1 = Enabled |
| 6 | 1 | CPUT3, CPUC3 | 0 = three-state, 1 = Enabled |
| 5 | 0 | 3V66_4/VCH | VCH Select 66 MHz/48 MHz 0 = 3V66 mode, 1 = VCH (48MHz) mode |
| 4 | 1 | 3V66_4/VCH | 3V66_4/VCH Output Enable 0 = Disabled, 1 = Enabled |
| 3 | 1 | 3V66_3 | 3V66_3 Output Enable 0 = Disabled, 1 = Enabled |
| 2 | 1 | 3V66_2 | 3V66_2 Output Enable 0 = Disabled, 1 = Enabled |
| 1 | 1 | 3V66_1 | 3V66_1 Output Enable 0 = Disabled, 1 = Enabled |
| 0 | 1 | 3V66_0 | 3V66_0 Output Enable 0 = Disabled, 1 = Enabled |

**Byte 6: Control Register 6**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | REF<br>PCIF<br>PCI<br>3V66<br>USB_48<br>DOT_48<br>CPUT/C<br>SRCT/C | Test Clock Mode<br>0= Disabled, 1 = Enabled |
| 6 | 0 | | Reserved, Set = 0 |
| 5 | 0 | CPUC0, CPUT0<br>CPUC1, CPUT1<br>CPUC2, CPUT2<br>CPUC3, CPUT3 | FS_A & FS_B Operation<br>0 = Normal, 1 = Test mode |
| 4 | 0 | SRCT, SRCC | SRC Frequency Select<br>0 = 100 MHz, 1 = 200 MHz |
| 3 | 0 | | Reserved, Set = 0 |
| 2 | 0 | PCIF<br>PCI<br>3V66<br>SRC(T/C)<br>CPUT/ C | Spread Spectrum Mode<br>0 = Spread Off, 1 = Spread On |
| 1 | 1 | REF_1 | REF_1 Output Enable<br>0 = Disabled, 1 = Enabled |
| 0 | 1 | REF_0 | REF_0 Output Enable<br>0 = Disabled, 1 = Enabled |

**Byte 7: Vendor ID**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Revision Code Bit 3 | Revision Code Bit 3 |
| 6 | 0 | Revision Code Bit 2 | Revision Code Bit 2 |
| 5 | 0 | Revision Code Bit 1 | Revision Code Bit 1 |
| 4 | 0 | Revision Code Bit 0 | Revision Code Bit 0 |
| 3 | 1 | Vendor ID Bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID Bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID Bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID Bit 0 | Vendor ID Bit 0 |

## Crystal Recommendations

The CY28419 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28419 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 6. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|---|---|---|---|---|---|---|---|---|---|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 50 ppm | 50 ppm | 5 ppm |

## Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low-ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is **not true**.
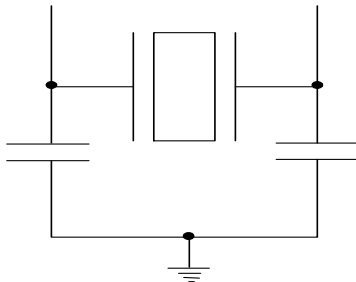


**Figure 1. Crystal Capacitive Clarification**

## Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.
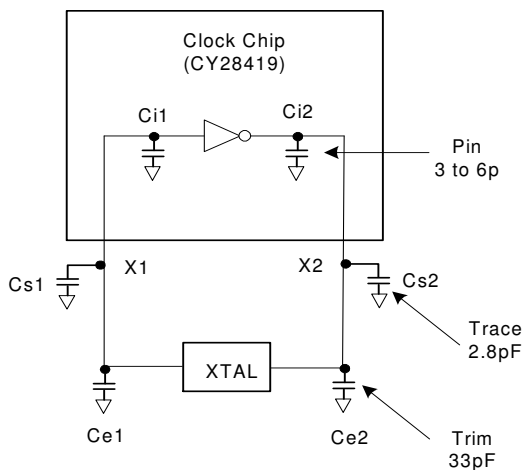


**Figure 2. Crystal Loading Example**

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance(CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors(Ce1,Ce2) should be calculated to provide equal capacitative loading on both sides.

Use the following formulas to calculate the trim capacitor values fro Ce1 and Ce2.

**Load Capacitance (each side)**

$$Ce = 2 * CL - (Cs + Ci)$$

**Total Capacitance (as seen by the crystal)**

$$CLe = \frac{1}{\left(\dfrac{1}{Ce1 + Cs1 + Ci1} + \dfrac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL....................................................Crystal load capacitance

CLe........................................ Actual loading seen by crystal
.................................... using standard value trim capacitors

Ce...................................................... External trim capacitors

Cs........................................... Stray capacitance (trace, etc.)

Ci ........................................................Internal capacitance
.............................................. (lead frame, bond wires, etc.)

### PD# (Power-down) Clarification

The PD# pin is used to shut off all clocks and PLLs without having to remove power from the device. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the power-down state.

### PD#–Assertion

When PD# is sampled low by two consecutive rising edges of the CPUC clock then all clock outputs (except CPU) clocks must be held low on their next high to low transition. CPU clocks must be held with CPUT clock pin driven high with a value of 2x Iref and CPUC undriven as the default condition. There exists an I2C bit that allows for the CPUT/C outputs to be three-stated during power-down. Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.
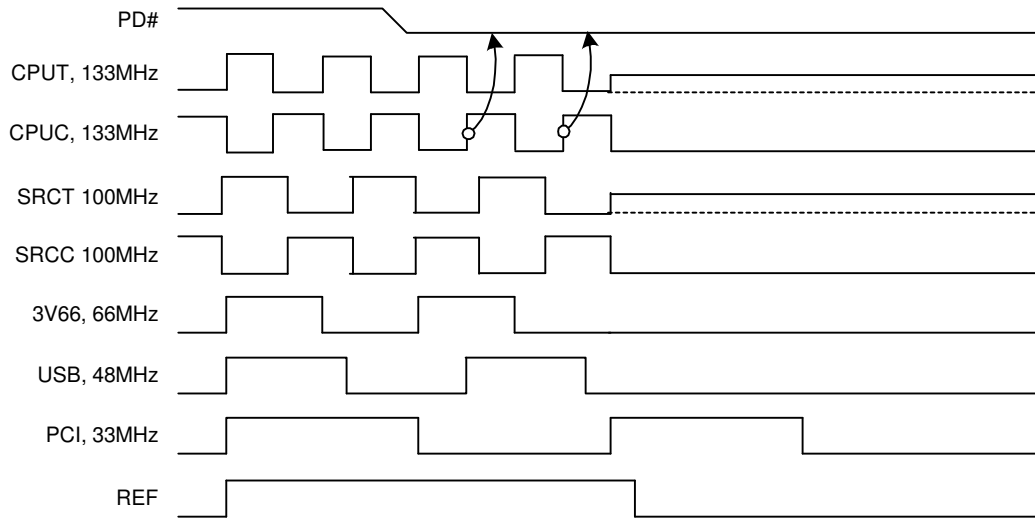
**Figure 3. Power-down Assertion Timing Waveforms**

**PD# Deassertion**

The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 1.8 ms. The CPUT/C outputs must be driven to greater than 200 mV is less than 300 us.
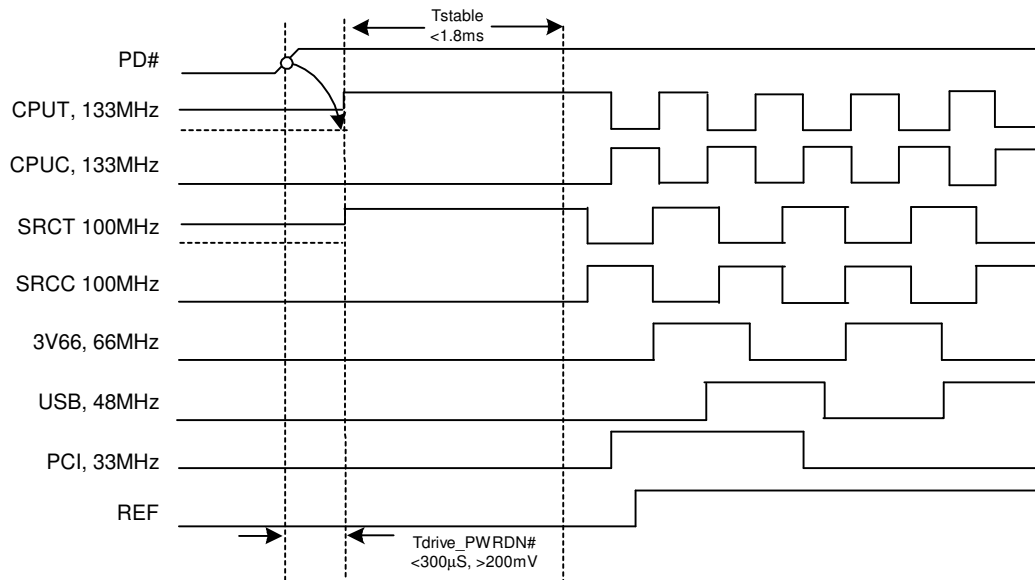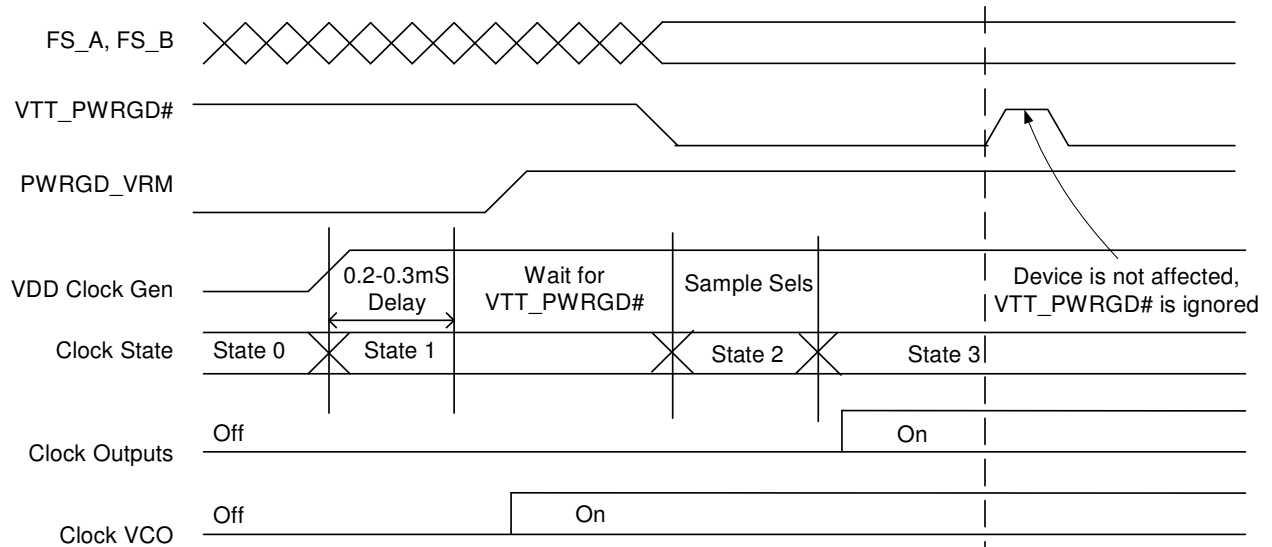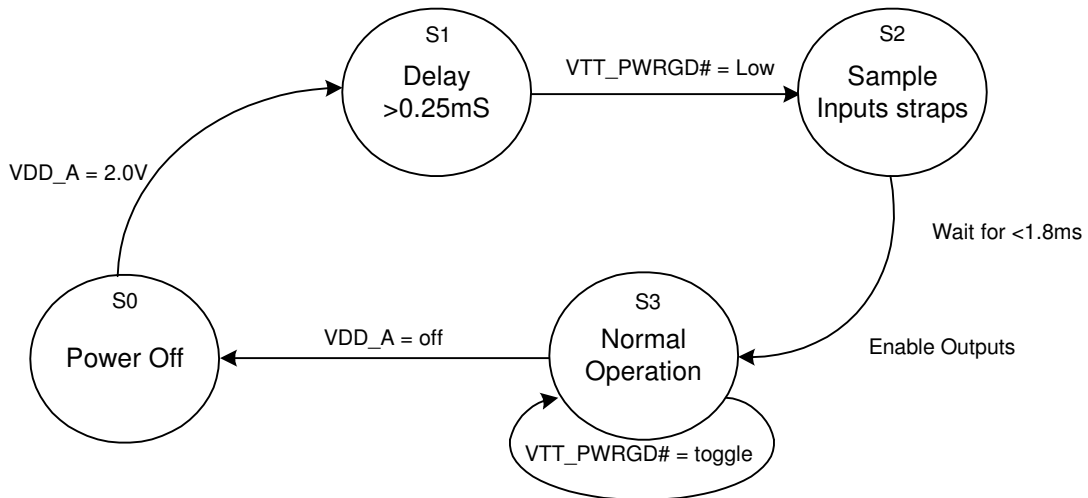


**Figure 4. Power-down Deassertion Timing Waveforms**

**Figure 5. VTTPWRGD Timing Diagram**



**Figure 6. Clock Generator Power-up/Run State Diagram**

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | −0.5 | 4.6 | V |
| $V_{DD\_A}$ | Analog Supply Voltage | | −0.5 | 4.6 | V |
| $V_{IN}$ | Input Voltage | Relative to $V_{SS}$ | −0.5 | $V_{DD}$ + 0.5 | VDC |
| $T_S$ | Temperature, Storage | Non-functional | −65 | +150 | ℃ |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | 70 | ℃ |
| $T_J$ | Temperature, Junction | Functional | – | 150 | ℃ |
| $\varnothing_{JC}$ | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | – | 15 | ℃/W |
| $\varnothing_{JA}$ | Dissipation, Junction to Ambient | JEDEC (JESD 51) | – | 45 | ℃/W |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| UL-94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

**Multiple Supplies**: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications

| Parameter | Description | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $V_{DD\_A}$ | 3.3 Operating Voltage | 3.3V ± 5% | 3.135 | 3.465 | V |
| $V_{ILI2C}$ | Input Low Voltage | SDATA, SCLK | – | 1.0 | V |
| $V_{IHI2C}$ | Input High Voltage | SDATA, SCLK | 2.2 | – | V |
| $V_{IL}$ | Input Low Voltage | | $V_{SS}$ – 0.5 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{DD}$ + 0.5 | V |
| $I_{IL}$ | Input Leakage Current | except Pull-ups or Pull-downs 0 < $V_{IN}$ < $V_{DD}$ | −5 | 5 | μA |
| $I_{ILI2C}$ | Input High Voltage | SDATA, SCLK | 2.2 | – | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1 mA | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −1 mA | 2.4 | – | V |
| $I_{OZ}$ | High-impedance Output Current | | −10 | 10 | μA |
| $C_{IN}$ | Input Pin Capacitance | | 2 | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | 3 | 6 | pF |
| $L_{IN}$ | Pin Inductance | | – | 7 | nH |
| $V_{XIH}$ | Xin High Voltage | | $0.7V_{DD}$ | $V_{DD}$ | V |
| $V_{XIL}$ | Xin Low Voltage | | 0 | $0.3V_{DD}$ | V |
| $I_{DD}$ | Dynamic Supply Current | At 200 MHz and all outputs loaded per *Table 9* and *Figure 7* | – | 280 | mA |
| $I_{PD}$ | Power-down Supply Current | PD# asserted, Outputs Three-stated | – | 1 | mA |

## AC Electrical Specifications

| Parameter | Description | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **Crystal** | | | | | |
| $T_{DC}$ | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| $T_{PERIOD}$ | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |
| $T_R / T_F$ | XIN Rise and Fall Times | Measured between $0.3V_{DD}$ and $0.7V_{DD}$ | – | 10.0 | ns |
| $T_{CCJ}$ | XIN Cycle-to-Cycle Jitter | As an average over 1-μs duration | – | 500 | ps |
| $L_{ACC}$ | Long-term Accuracy | Over 150 ms | – | 300 | ppm |

## AC Electrical Specifications (continued)

| Parameter | Description | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **CPU at 0.7V** | | | | | |
| $T_{DC}$ | CPUT and CPUC Duty Cycle | Measured at crossing point $V_{OX}$ | 45 | 55 | % |
| $T_{PERIOD}$ | 100-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 9.9970 | 10.003 | ns |
| $T_{PERIOD}$ | 133-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 7.4978 | 7.5023 | ns |
| $T_{PERIOD}$ | 166-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 5.9982 | 6.0018 | ns |
| $T_{PERIOD}$ | 200-MHz CPUT and CPUC Period | Measured at crossing point $V_{OX}$ | 4.9985 | 5.0015 | ns |
| $T_{SKEW}$ | Any CPU to CPU Clock Skew | Measured at crossing point $V_{OX}$ | – | 100 | ps |
| $T_{CCJ}$ | CPU Cycle-to-Cycle Jitter | Measured at crossing point $V_{OX}$ | – | 125 | ps |
| $T_R/T_F$ | CPUT/CPUC Rise and Fall Times | Measured from $V_{OL} = 0.175$ to $V_{OH} = 0.525V$ | 175 | 700 | ps |
| $T_{RFM}$ | Rise/Fall Matching | Determined as a fraction of $2*(T_R–T_F)/ (T_R+T_F)$ | – | 20 | % |
| $\Delta T_R$ | Rise Time Variation | | – | 125 | ps |
| $\Delta T_F$ | Fall Time Variation | | – | 125 | ps |
| $V_{HIGH}$ | Voltage High | Math average, see *Figure 7* | 660 | 850 | mv |
| $V_{LOW}$ | Voltage Low | Math average, see *Figure 7* | −150 | – | mv |
| $V_{OX}$ | Crossing Point voltage at 0.7V Swing | | 250 | 550 | mv |
| $V_{OVS}$ | Maximum Overshoot Voltage | | – | $V_{HIGH} + 0.3$ | V |
| $V_{UDS}$ | Minimum Undershoot Voltage | | −0.3 | – | V |
| $V_{RB}$ | Ring Back Voltage | See *Figure 7*. Measure SE | – | 0.2 | V |
| **SRC** | | | | | |
| $T_{DC}$ | SRCT and SRCC Duty Cycle | Measured at crossing point $V_{OX}$ | 45 | 55 | % |
| $T_{PERIOD}$ | 100-MHz SRCT and SRCC Period | Measured at crossing point $V_{OX}$ | 9.9970 | 10.003 | ns |
| $T_{PERIOD}$ | 200-MHz SRCT and SRCC Period | Measured at crossing point $V_{OX}$ | 4.9985 | 5.0015 | ns |
| $T_{CCJ}$ | SRC Cycle-to-Cycle Jitter | Measured at crossing point $V_{OX}$ | – | 125 | ps |
| $L_{ACC}$ | SRCT/C Long-term Accuracy | Measured at crossing point $V_{OX}$ | – | 300 | ppm |
| $T_R / T_F$ | SRCT/SRCT\C Rise and Fall Times | Measured from $V_{OL} = 0.175$ to $V_{OH} = 0.525V$ | 175 | 700 | ps |
| $T_{RFM}$ | Rise/Fall Matching | Determined as a fraction of $2*(T_R–T_F)/ (T_R+T_F)$ | – | 20 | % |
| $\Delta T_R$ | Rise Time Variation | | – | 125 | ps |
| $\Delta T_F$ | Fall Time Variation | | – | 125 | ps |
| $V_{HIGH}$ | Voltage High | Math average, see *Figure 7* | 660 | 850 | mv |
| $V_{LOW}$ | Voltage Low | Math average, see *Figure 7* | −150 | – | mv |
| $V_{OX}$ | Crossing Point Voltage at 0.7V Swing | | 250 | 550 | mV |
| $V_{OVS}$ | Maximum Overshoot Voltage | | – | $V_{HIGH}+0.3$ | V |
| $V_{UDS}$ | Minimum Undershoot Voltage | | −0.3 | – | V |
| $V_{RB}$ | Ring Back Voltage | See *Figure 7*. Measure SE | – | 0.2 | V |
| **3V66** | | | | | |
| $T_{DC}$ | 3V66 Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Spread Disabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0045 | ns |
| $T_{PERIOD}$ | Spread Enabled 3V66 Period | Measurement at 1.5V | 14.9955 | 15.0799 | ns |
| $T_{HIGH}$ | 3V66 High Time | Measurement at 2.0V | 4.9500 | – | ns |
| $T_{LOW}$ | 3V66 Low Time | Measurement at 0.8V | 4.5500 | – | ns |
| $T_R / T_F$ | 3V66 Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | ns |
| $T_{SKEW}$ | Any 3V66 to Any 3V66 Clock Skew | Measurement at 1.5V | – | 250 | ps |
| $T_{CCJ}$ | 3V66 Cycle-to-Cycle Jitter | Measurement at 1.5V | – | 250 | ps |

## AC Electrical Specifications (continued)

| Parameter | Description | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| **PCI / PCIF** | | | | | |
| $T_{DC}$ | PCIF and PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.0009 | ns |
| $T_{PERIOD}$ | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 29.9910 | 30.1598 | ns |
| $T_{HIGH}$ | PCIF and PCI High Time | Measurement at 2.0V | 12.0 | – | nS |
| $T_{LOW}$ | PCIF and PCI Low Time | Measurement at 0.8V | 12.0 | – | nS |
| $T_R / T_F$ | PCIF and PCI rise and fall times | Measured between 0.8V and 2.0V | 0.5 | 2.0 | nS |
| $T_{SKEW}$ | Any PCI Clock to Any PCI Clock Skew | Measurement at 1.5V | – | 500 | pS |
| $T_{CCJ}$ | PCIF and PCI Cycle-to-Cycle Jitter | Measurement at 1.5V | – | 250 | ps |
| **DOT** | | | | | |
| $T_{DC}$ | DOT Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | DOT Period | Measurement at 1.5V | 20.8257 | 20.8340 | ns |
| $T_{HIGH}$ | DOT High Time | Measurement at 2.0V | 8.994 | 10.486 | nS |
| $T_{LOW}$ | DOT Low Time | Measurement at 0.8V | 8.794 | 10.386 | nS |
| $T_R / T_F$ | Rise and Fall Times | Measured between 0.8V and 2.0V | 0.5 | 1.0 | ns |
| $T_{LTJ}$ | Long-term Jitter | 10-μs period | – | 2.0 | ns |
| **USB** | | | | | |
| $T_{DC}$ | USB Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | USB Period | Measurement at 1.5V | 20.8257 | 20.8340 | ns |
| $T_{HIGH}$ | USB High Time | Measurement at 2.0V | 8.094 | 10.036 | nS |
| $T_{LOW}$ | USB Low Time | Measurement at 0.8V | 7.694 | 9.836 | nS |
| $T_R / T_F$ | Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 2.0 | ns |
| $T_{LTJ}$ | Long-term Jitter | 125-μs period | – | 6.0 | ns |
| **REF** | | | | | |
| $T_{DC}$ | REF Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| $T_{PERIOD}$ | REF Period | Measurement at 1.5V | 69.827 | 69.855 | ns |
| $T_R / T_F$ | REF Rise and Fall Times | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| $T_{CCJ}$ | REF Cycle-to-Cycle Jitter | Measurement at 1.5V | – | 1000 | ps |
| **ENABLE/DISABLE and SET-UP** | | | | | |
| $T_{STABLE}$ | Clock Stabilization from Power-up | | – | 1.8 | ms |
| $T_{SS}$ | Stopclock Set-up Time | | 10.0 | – | ns |
| $T_{SH}$ | Stopclock Hold Time | | 0 | – | ns |

**Table 7. Group Timing Relationship and Tolerances**

| | | Offset | |
|---|---|---|---|
| **Group** | **Conditions** | **Min.** | **Max.** |
| 3V66 to PCI | 3V66 Leads PCI | 1.5 ns | 3.5 ns |

**Table 8. USB to DOT Phase Offset**

| Parameter | Typical | Value | Tolerance |
|---|---|---|---|
| DOT Skew | 0° | 0.0ns | 1000 ps |
| USB Skew | 180° | 0.0ns | 1000 ps |
| VCH SKew | 0° | 0.0ns | 1000 ps |

**Table 9. Maximum Lumped Capacitive Output Loads**

| Clock | Max Load | Unit |
|---|---|---|
| PCI Clocks | 30 | pF |
| 3V66 Clocks | 30 | pF |
| USB Clock | 20 | pF |
| DOT Clock | 10 | pF |
| REF Clock | 30 | pF |

## Test and Measurement Set-up

### For Differential CPU and SRC Output Signals

The following diagram shows lumped test load configurations
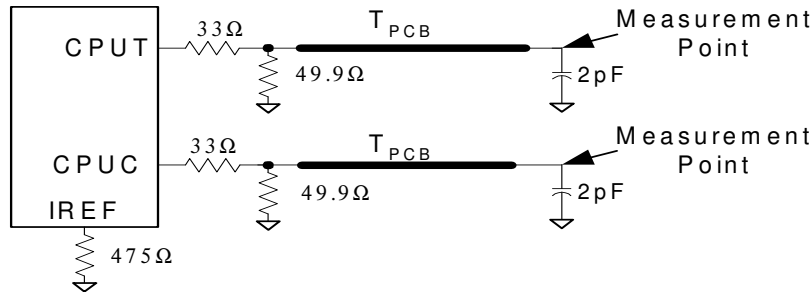for the differential Host Clock Outputs.
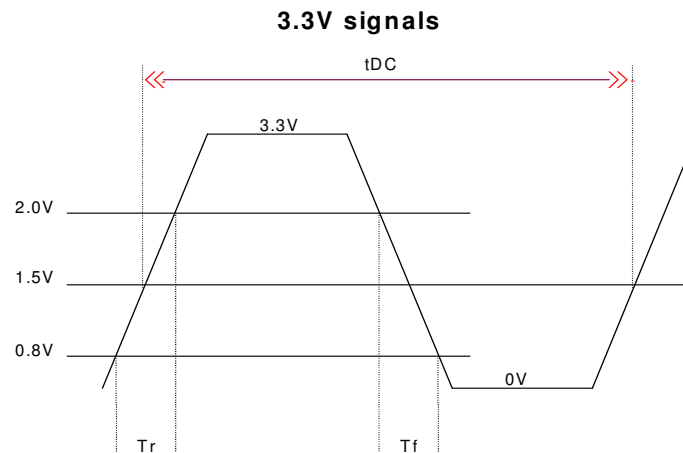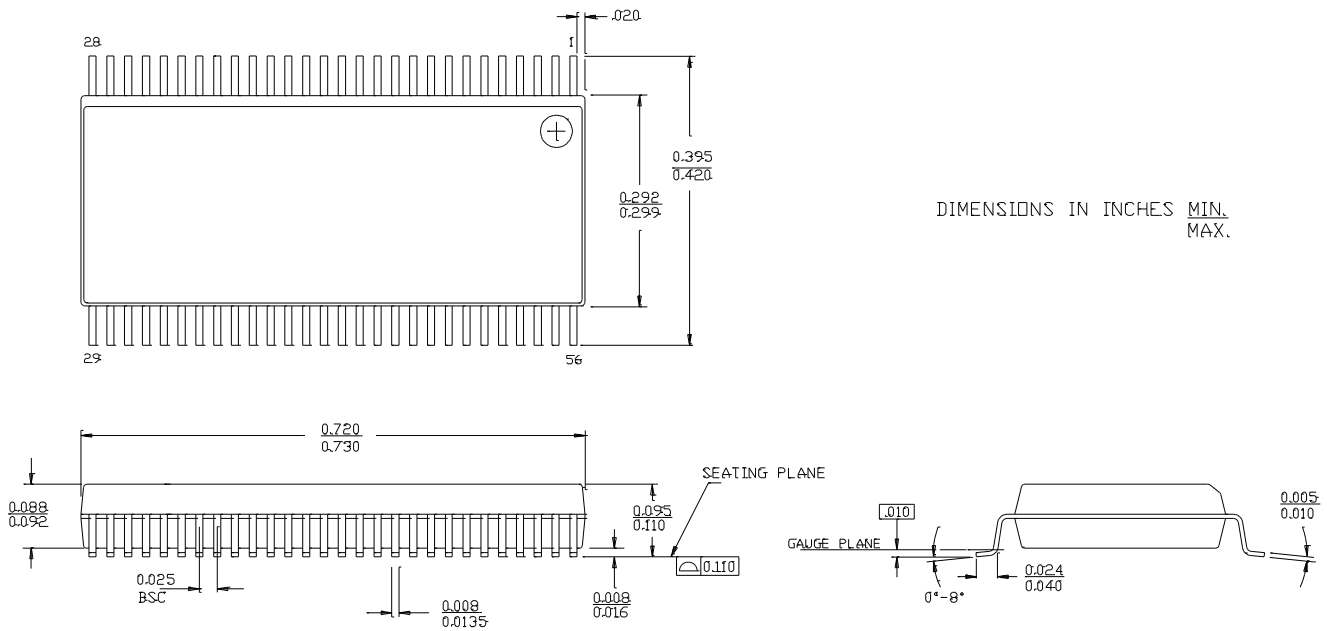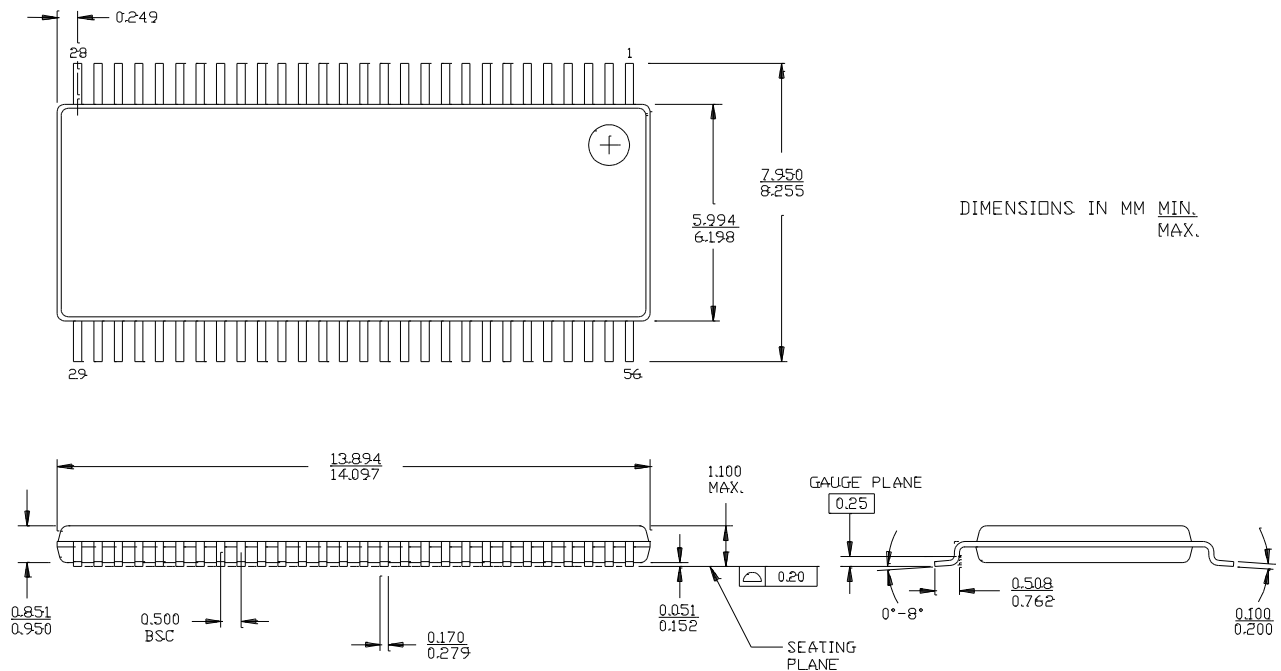


**Figure 7. 0.7V Load Configuration**

**3.3V signals**



**Figure 8. Lumped Load For Single-ended Output Signals (for AC Parameters Measurement)**

**Table 10.CPU Clock Current Select Function**

| Board Target Trace/Term Z | Reference R, Iref – V$_{DD}$ (3*Rr) | Output Current | Voh @ Z |
|---|---|---|---|
| 50 Ohms | R$_{REF}$ = 475 1%, I$_{REF}$ = 2.32 mA | Ioh = 6*Iref | 0.7V @ 50 |

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY28419OC | 56-pin Shrunk Small Outline package (SSOP) | Commercial, 0° to 70°C |
| CY28419OCT | 56-pin Shrunk Small Outline package (SSOP) – Tape and Reel | Commercial, 0° to 70°C |
| CY28419ZC | 56-pin Thin Shrunk Small Outline package (TSSOP) | Commercial, 0° to 70°C |
| CY28419ZCT | 56-pin Thin Shrunk Small Outline package (TSSOP) – Tape and Reel | Commercial, 0° to 70°C |
| **Part Number** | **Package Type - Lead Free** | **Product Flow** |
| CY28419OXC | 56-pin Shrunk Small Outline package (SSOP) | Commercial, 0° to 70°C |
| CY28419OXCT | 56-pin Shrunk Small Outline package (SSOP) – Tape and Reel | Commercial, 0° to 70°C |
| CY28419ZXC | 56-pin Thin Shrunk Small Outline package (TSSOP) | Commercial, 0° to 70°C |
| CY28419ZXCT | 56-pin Thin Shrunk Small Outline package (TSSOP) – Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

**56-Lead Shrunk Small Outline Package O56**

DIMENSIONS IN INCHES MIN.
MAX.

.020

28

0.395
0.420

0.292
0.299

29

56

0.720
0.730

SEATING PLANE

0.088
0.092

0.095
0.110

0.010

GAUGE PLANE

0.005
0.010

0.025
BSC

0.008
0.0135

0.008
0.016

0.110

0.024
0.040

0°–8°

**56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 14 mm) Z56**

0.249

28

1

7.950
8.255

5.994
6.198

DIMENSIONS IN MM MIN.
MAX.

29

56

13.894
14.097

1.100
MAX.

GAUGE PLANE

0.25

0.851
0.950

0.500
BSC

0.170
0.279

0.051
0.152

0.20

0.508
0.762

0°–8°

0.100
0.200

SEATING
PLANE