LM4925 Boomer™ Audio Power Amplifier Series 2 Cell, Single Ended Output, 40mW Stereo Headphone Audio Amplifier

Check for Samples: LM4925

FEATURES

- **BTL Mode for Mono Speaker**
- **2-Cell 1.5V to 3.6V Battery Operation**
- **Single Ended Headphone Operation with Output Coupling Capacitors**
- **Unity-Gain Stable**
- **“Click and Pop” Suppression Circuitry for Both Shutdown and Mute**
- **Active Low Micro-Power Shutdown**
- **Active-Low Mute Mode**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Portable Two-Cell Audio Products**
- **Portable Two-Cell Electronic Devices**

KEY SPECIFICATIONS

- **Mono-BTL Output Power**
  - **(R_L = 8Ω, V_{DD} = 3.0V, THD+N = 1%), 410mW (Typ)**
- **Single Ended Output Power Per Channel,**
  - **(R_L = 16Ω, V_{DD} = 3.0V, THD+N = 1%), 40mW (Typ)**
- **Micropower Shutdown Current, 0.1µA (Typ)**
- **Supply Voltage Operating Range, 1.5V < V_{DD} < 3.6V**
- **PSRR 100Hz, V_{DD} = 3V, BTL, 70dB (Typ)**

DESCRIPTION

The unity gain stable LM4925 is both a mono differential output (for BTL operation) audio amplifier and a Single Ended (SE) stereo headphone amplifier. Operating on a single 3V supply, the mono-BTL mode delivers 410mW into an 8Ω load at 1% THD+N. In Single Ended stereo headphone mode, the amplifier delivers 40mW per channel into a 16Ω load at 1% THD+N.

With the LM4925 packaged in the VSSOP and SON packages, the customer benefits include low profile and small size. This package minimizes PCB area and maximizes output power.

The LM4925 features circuitry that reduces output transients (“clicks” and “pops”) during device turn-on and turn-off, an externally controlled, low-power consumption, active-low shutdown mode, and thermal shutdown. Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

Typical Application

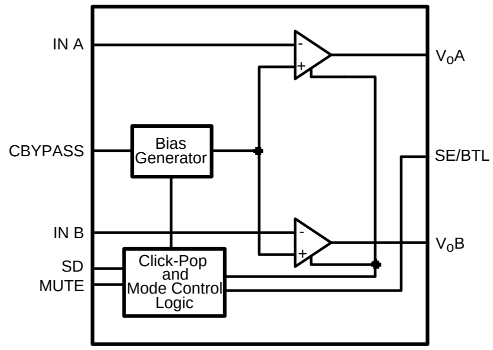


Figure 1. Block Diagram

Connection Diagrams

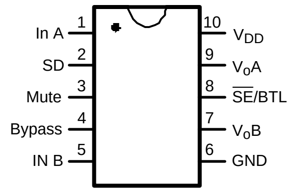


Figure 2. VSSOP Package
Top View
See Package Number DGS for VSSOP

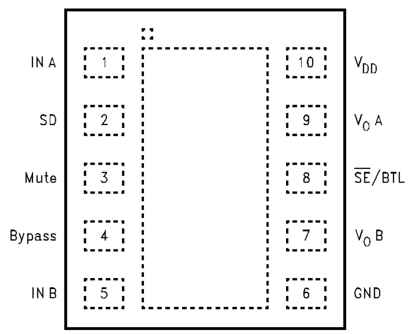


Figure 3. SON Package
Top View
See Package Number DSC0010A

Typical Connections

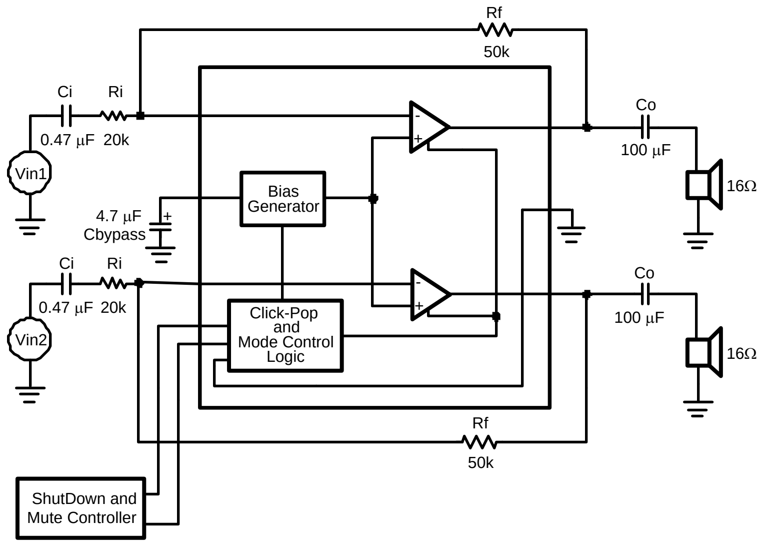


Figure 4. Typical Capacitive Couple (SE) Output Configuration Circuit

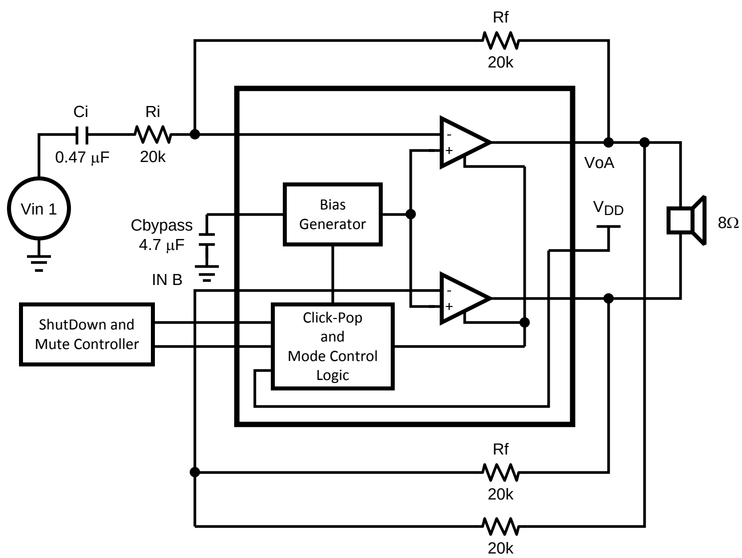


Figure 5. Typical BTL Speaker Configuration Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage			3.8V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation[3]			Internally limited
ESD Susceptibility[4]			2000V
ESD Susceptibility[5]			200V
Junction Temperature			150°C
Solder Information	Small Outline Package Vapor	Phase (60sec)	215°C
		Infrared (15 sec)	220°C
Thermal Resistance		θ_{JA} (typ) DGS	175°C/W
		θ_{JA} (typ) DSC0010A	73°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4925, T_{JMAX} = 150°C. For the θ_{JA}s, please see the Application Information section or the Absolute Maximum Ratings section.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine model, 220pF–240pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
	Supply Voltage	$1.5V \le V_{DD} \le 3.6V$

Electrical Characteristics V_{DD} = 3.0V[1][2]

The following specifications apply for the circuit shown in Figure 4 for Single Ended Outputs (A_V = 2.5V) and Figure 5 for BTL Outputs (A_{V-BTL} = 2), unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4925		Units (Limits)
			Typical[3]	Limit[4]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ [5]	1.0	1.6	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1	µA (max)
V_{OS}	Output Offset Voltage		2	10	mV (max)
P_O	Output Power[6]	R_L = 8Ω, BTL, Figure 5 THD+N = 1%, f = 1kHz	410	350	mW (min)
		R_L = 16Ω, Figure 4, SE per Channel, THD+N = 1%, f = 1kHz	40	30	mW (min)
THD+N	Total Harmonic Distortion + Noise	R_L = 8Ω, BTL, P_O = 300mW, Figure 5, f = 1kHz	0.1	0.5	% (max)
		R_L = 16Ω, SE, P_O = 20mW per channel, Figure 4, f = 1kHz	0.05		
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Input Referred, Single Ended Output, Figure 4	10		μV_{RMS}
Crosstalk		R_L = 16Ω, Figure 4	58		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave C_{BYPASS} = 4.7µF, R_L = 8Ω f = 100Hz, BTL, Figure 5	70		dB
		V_{RIPPLE} = 200mV_{P-P} sine wave C_{BYPASS} = 4.7µF, R_L = 16Ω f = 100Hz, SE, Figure 4	68		dB
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.6V		0.7V_{DD}	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.6V		0.3V_{DD}	V (max)
Mute Attenuation		1V_{PP} Reference, R_i = 20k, R_f = 50k		70	dB (min)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

Electrical Characteristics V_{DD} = 1.8V [(1)] [(2)]

The following specifications apply for the circuit shown in Figure 4 for Single Ended Outputs (A_V = 2.5V) and Figure 5 for BTL Outputs ($A_{V\text{-}BTL}$ = 2), unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4925		Units (Limits)
			Typical [(3)]	Limit [(4)]	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ [(5)]	0.9	1.6	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.05	1	μA (max)
V_{OS}	Output Offset Voltage		2	10	mV (max)
P_O	Output Power [(6)]	R_L = 8Ω, BTL, Figure 5, THD+N = 1%, f = 1kHz	120	90	mW (min)
		R_L = 16Ω, Figure 4, SE per Channel, THD+N = 1%, f = 1kHz	10	7	mW (min)
THD+N	Total Harmonic Distortion + Noise	R_L = 8Ω, BTL, P_O = 50mW, Figure 5, f = 1kHz	0.15	0.5	% (max)
		R_L = 16Ω, SE, P_O = 5mW per channel, Figure 4, f = 1kHz	0.1		
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Input Referred, Single Ended Output, Figure 4	10		μV_{RMS}
Crosstalk		R_L = 16Ω, Figure 4	58		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200m$V_{P\text{-}P}$ sine wave C_{BYPASS} = 4.7μF, R_L = 8Ω f = 100Hz, BTL, Figure 5	70		dB
		V_{RIPPLE} = 200m$V_{P\text{-}P}$ sine wave C_{BYPASS} = 4.7μF, R_L = 16Ω f = 100Hz, SE, Figure 4	68		dB
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.6V		0.7V_{DD}	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.6V		0.3V_{DD}	V (max)
Mute Attenuation		1V_{PP} Reference, R_i = 20k, R_f = 50k		70	dB (min)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 1.8V, SE, R_L = 16Ω
P_O = 5mW per channel

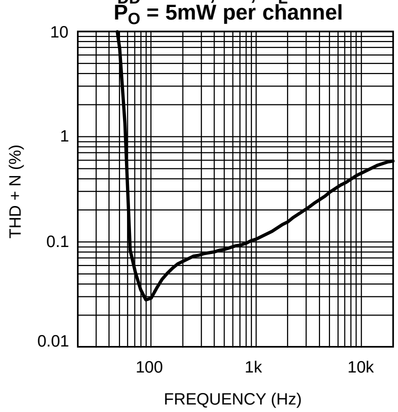


Figure 6.

THD+N vs Frequency
V_{DD} = 3V, SE, R_L = 16Ω
P_O = 20mW per channel

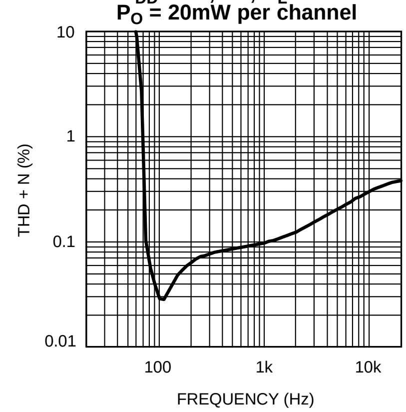


Figure 7.

THD+N vs Frequency
V_{DD} = 1.8V, BTL, R_L = 8Ω
P_O = 50mW

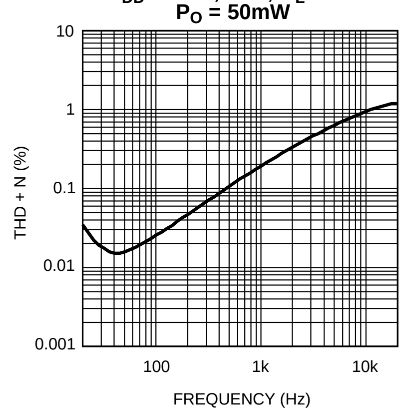


Figure 8.

THD+N vs Frequency
V_{DD} = 3V, BTL, R_L = 8Ω
P_O = 300mW

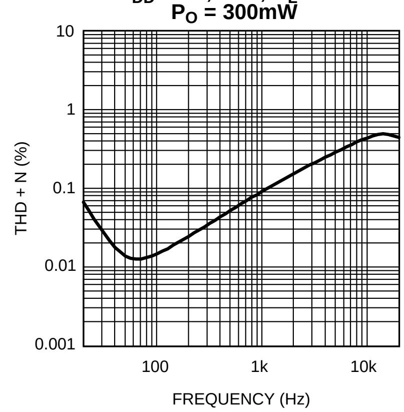


Figure 9.

THD+N vs Output Power
V_{DD} = 1.8V, SE, R_L = 16Ω
f = 1kHz, Both channels

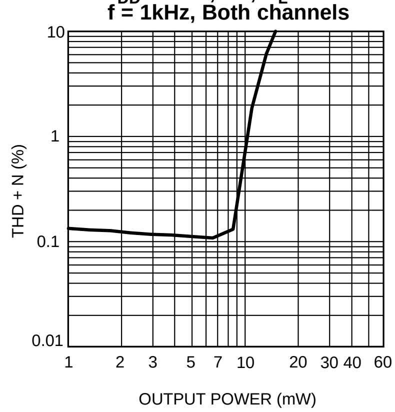


Figure 10.

THD+N vs Output Power
V_{DD} = 3V, SE, R_L = 16Ω
f = 1kHz, Both channels

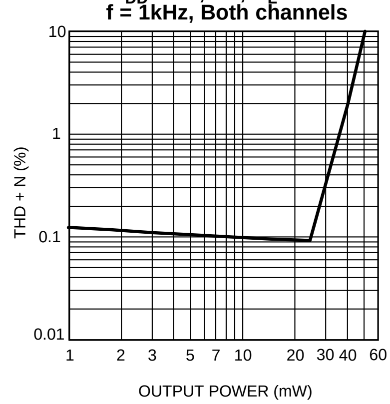


Figure 11.

Typical Performance Characteristics (continued)

THD+N vs Output Power
V_{DD} = 1.8V, BTL, R_L = 8Ω
f = 1kHz

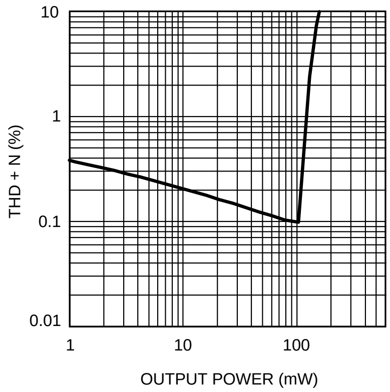


Figure 12.

THD+N vs Output Power
V_{DD} = 3V, BTL, R_L = 8Ω
f = 1kHz

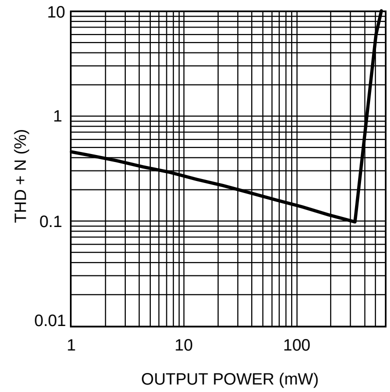


Figure 13.

Output Noise vs Frequency

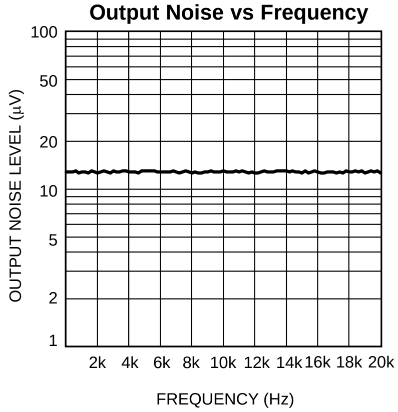


Figure 14.

Output Power vs Supply Voltage
R_L = 8Ω, BTL, f = 1kHz

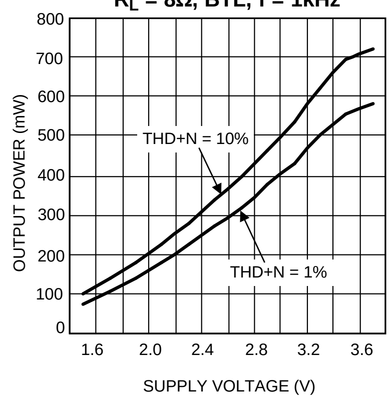


Figure 15.

Output Power vs Supply Voltage
R_L = 16Ω, SE, f = 1kHz

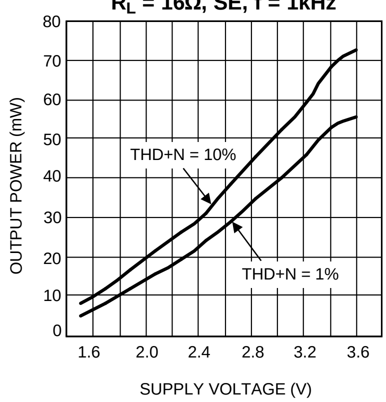


Figure 16.

Output Power vs Load Resistance
V_{DD} = 1.8V, BTL, f = 1kHz

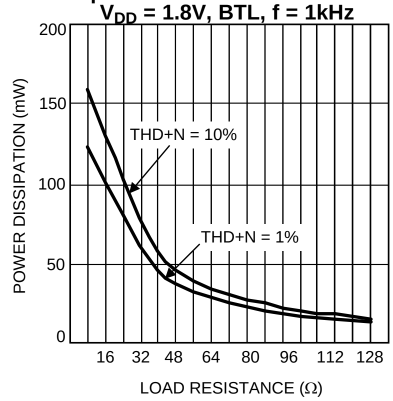


Figure 17.

Typical Performance Characteristics (continued)

Output Power vs Load Resistance
V_{DD} = 1.8V, SE, f = 1kHz

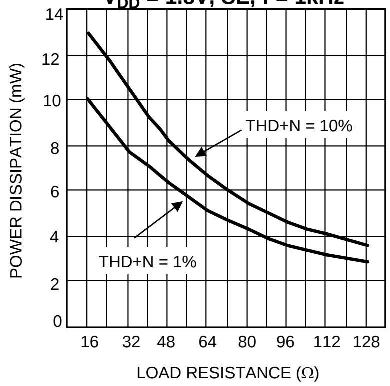


Figure 18.

Output Power vs Load Resistance
V_{DD} = 3V, BTL, f = 1kHz

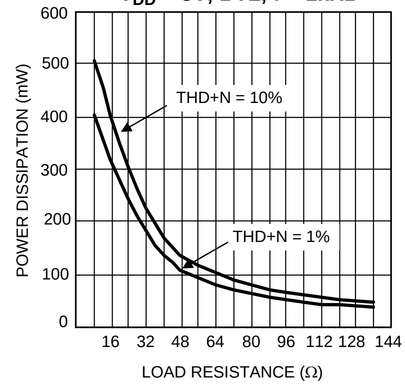


Figure 19.

Output Power vs Load Resistance
V_{DD} = 3V, SE, f = 1kHz

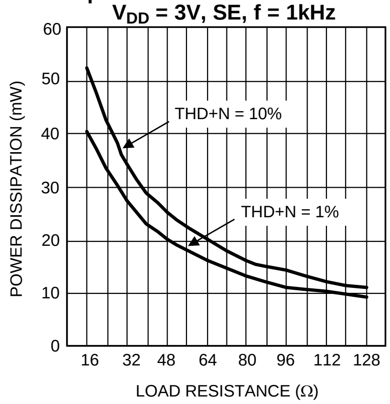


Figure 20.

Output Power vs Supply Voltage
R_L = 8Ω, BTL, f = 1kHz

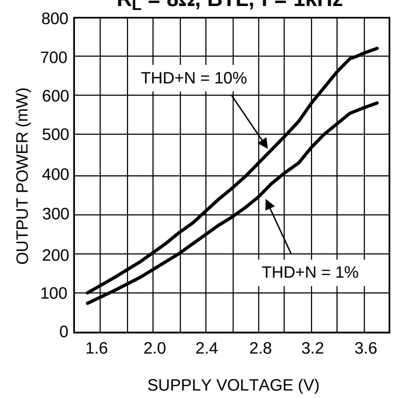


Figure 21.

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 8Ω, BTL, f = 1kHz

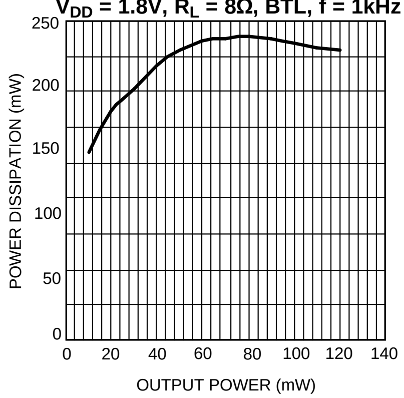


Figure 22.

Power Dissipation vs Output Power
V_{DD} = 1.8V, R_L = 16Ω, SE, f = 1kHz

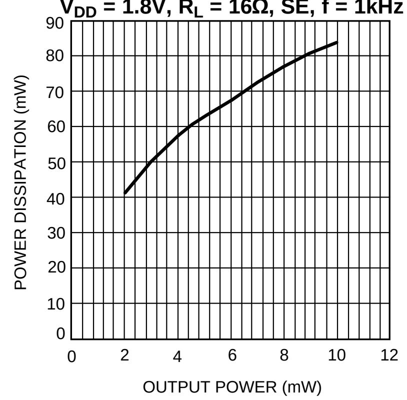


Figure 23.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 8Ω, BTL, f = 1kHz

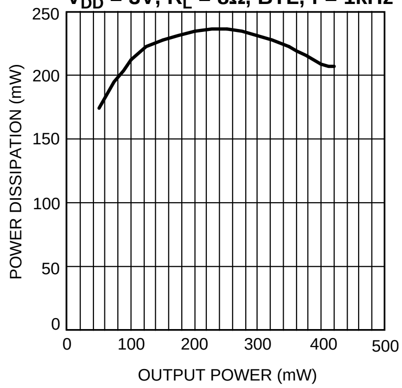


Figure 24.

Power Dissipation vs Output Power
V_{DD} = 3V, R_L = 16Ω, SE, f = 1kHz

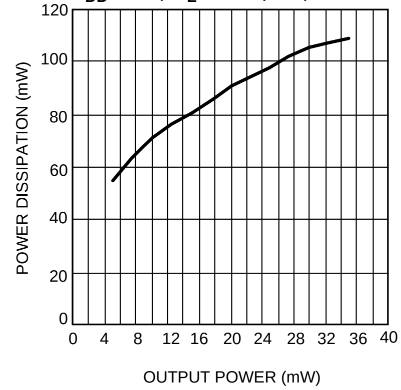


Figure 25.

Power Supply Rejection vs Frequency
V_{DD} = 1.8V, R_L = 8Ω, BTL
V_{RIPPLE} = 200mVp-p, A_{V-BTL} = 2V/V

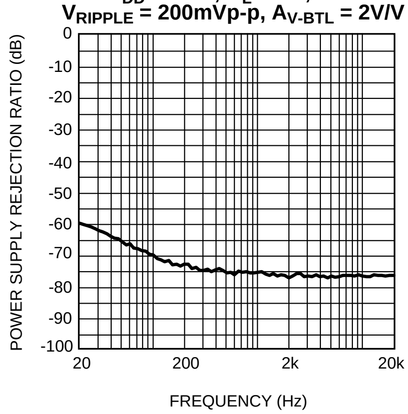


Figure 26.

Power Supply Rejection vs Frequency
V_{DD} = 1.8V, R_L = 16Ω, SE
V_{RIPPLE} = 200mVp-p, A_V = 2.5V/V

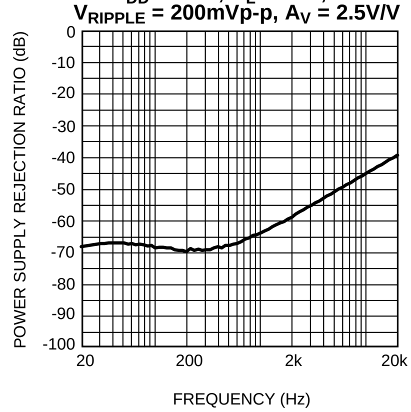


Figure 27.

Power Supply Rejection vs Frequency
V_{DD} = 3V, R_L = 8Ω, BTL
V_{RIPPLE} = 200mVp-p, A_{V-BTL} = 2V/V

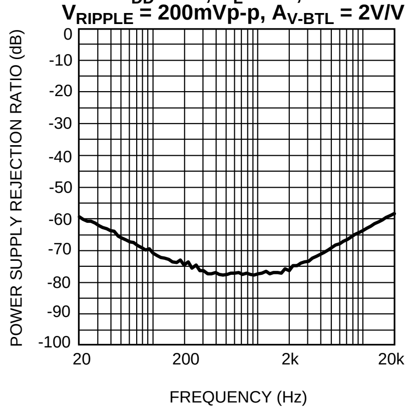


Figure 28.

Power Supply Rejection vs Frequency
V_{DD} = 3V, R_L = 16Ω, SE
V_{RIPPLE} = 200mVp-p, A_V = 2.5V/V

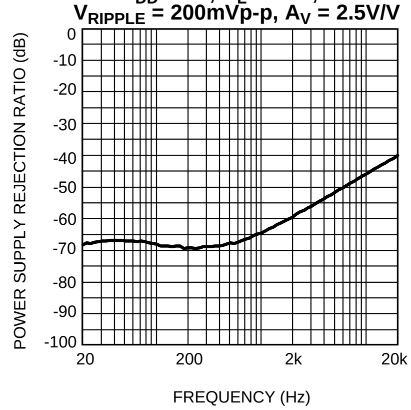


Figure 29.

APPLICATION INFORMATION

BRIDGE (BTL) CONFIGURATION EXPLANATION

The LM4925 is a stereo audio power amplifier capable of operating in bridged (BTL) mode. As shown in Figure 5, the LM4925 has two internal operational amplifiers. The first amplifier's gain is externally configurable, while the second amplifier should be externally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of Rf to Ri while the second amplifier's gain is fixed by the two external 20kΩ resistors. Figure 5 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

By driving the load differentially through outputs VoA and VoB, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground. A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the AUDIO POWER AMPLIFIER DESIGN section.

A bridge configuration, such as the one used in LM4925, also creates a second advantage over single-ended amplifiers. Since the differential outputs, VoA and VoB, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration.

MODE SELECT DETAIL

The LM4925 can be configured for either single ended (see Figure 4) or BTL mode (see Figure 5). When the $\overline{SE}$/BTL pin has a logic high (V_{DD}) applied to it, the LM4925 is in BTL mode. If a logic low (GND) is applied to $\overline{SE}$/BTL, the LM4925 operates in single-ended mode. The slew rate of V_{DD} must be greater than 2.5V/ms to ensure reliable Power on reset (POR). The circuit shown in Figure 30 presents an applications solution to the problem of using different supply voltages with different turn-on times in a system with the LM4925. This circuit shows the LM4925 with a 25-50kΩ. Pull-up resistor connected from the shutdown pin to V_{DD}. The shutdown pin of the LM4925 is also being driven by an open drain output of an external microcontroller on a separate supply. This circuit ensures that shutdown is disabled when powering up the LM4925 by either allowing shutdown to be high before the LM4925 powers on (the microcontroller powers up first) or allows shutdown to ramp up with V_{DD} (the LM4925 powers up first). This will ensure the LM4925 powers up properly and enters the correct mode of operation (BTL or SE). Please note that the $\overline{SE}$/BTL pin should be tied to GND for single-ended (SE) mode, and to Vdd for BTL mode.

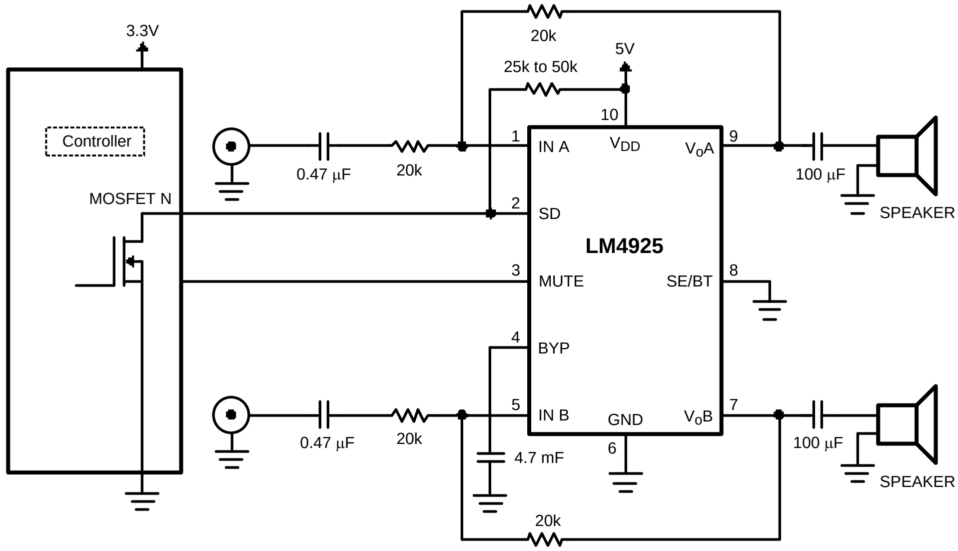


Figure 30. Recommended Circuit for Different Supply Turn-On Timing

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged (BTL) or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4925 has two operational amplifiers in one package, the maximum internal power dissipation in BTL mode is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$P_{DMAX} = 4 * (V_{DD})^{2} / (2\pi^{2}R_{L}) \quad (2)$$

When operating in single ended mode, Equation 3 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^{2} / (2\pi^{2}R_{L}) \quad (3)$$

Since the LM4925 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number that results from Equation 3.

The maximum power dissipation point obtained from either Equation 2 or Equation 3 must not be greater than the power dissipation that results from Equation 4:

$$P_{DMAX} = (T_{JMAX} - T_{A}) / \theta_{JA} \quad (4)$$

For package DGS, θ_{JA} = 175°C/W. T_{JMAX} = 150°C for the LM4925. Depending on the ambient temperature, T_A, of the system surroundings, Equation 4 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 or Equation 3 is greater than that of Equation 4, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 3.0V power supply, with an 16Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 129°C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible. Typical applications employ a battery (or 3.0V regulator) with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4925. A bypass capacitor value in the range of 0.1µF to 4.7µF is recommended.

MICRO POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4925's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the SHUTDOWN pin. When active, the LM4925's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. A voltage that is higher than ground may increase the shutdown current. There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by opening the switch. Closing the switch connects the SHUTDOWN pin to ground, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull-up resistor. Shutdown enable/disable times are controlled by a combination of C_{bypass} and V_{DD}. Larger values of C_{bypass} results in longer turn on/off times from Shutdown. Longer shutdown times also improve the LM4925's resistance to click and pop upon entering or returning from shutdown. For a 3.0V supply and C_{bypass} = 4.7µF, the LM4925 requires about 2 seconds to enter or return from shutdown. This longer shutdown time enables the LM4925 to have virtually zero pop and click transients upon entering or release from shutdown. Smaller values of C_{bypass} will decrease turn-on time, but at the cost of increased pop and click and reduced PSRR. When the LM4925 is in shutdown, the outputs become very low impedance (less than 5Ω to GND).

MUTE

The LM4925 also features a mute function that enables extremely fast turn-on/turn-off with a minimum of output pop and click. The mute function leaves the outputs at their bias level, thus resulting in higher power consumption than shutdown mode, but also provides much faster turn on/off times. Providing a logic low signal on the MUTE pin enables mute mode. Threshold voltages and activation techniques match those given for the shutdown function as well.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4925 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality. The LM4925 is unity-gain stable that gives the designer maximum system flexibility. The LM4925 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Very large values should not be used for the gain-setting resistors. Values for Ri and Rf should be less than 1MΩ. Please refer to the section, AUDIO POWER AMPLIFIER DESIGN, for a more complete explanation of proper gain selection. Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 4 and Figure 5. The input coupling capacitor, Ci, forms a first order high pass filter that limits low frequency response. This value should be chosen based on needed frequency response and turn-on time.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, Ci. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor. In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of Ci (in the range of 0.1µF to 0.47µF), is recommended.

AUDIO POWER AMPLIFIER DESIGN

A 25mW/32Ω Audio Amplifier

Given:	
Power Output	10mWrms
Load Impedance	16Ω
Input Level	0.4Vrms
Input Impedance	20kΩ

A designer must first choose a mode of operation (SE or BTL) and determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs. Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. 3.0V is a standard voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4925 to reproduce peak in excess of 10mW without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the POWER DISSIPATION section. Once the power dissipation equations have been addressed, the required gain can be determined from Equation 5.

$$A_V \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{orms} / V_{inrms} \tag{5}$$

From Equation 5, the minimum AV is 1; use A_V = 1. Since the desired input impedance is 20k, and with a A_V gain of 1, a ratio of 1:1 results from Equation 1 for R_f to R. The values are chosen with R_i = 20k and R_f = 20k. The final design step is to address the bandwidth requirements which must be stated as a pair of -3dB frequency points. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ± 0.25dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the PROPER SELECTION OF EXTERNAL COMPONENTS section, R_i in conjunction with C_i creates a

C_i ≥ 1 / (2π * 20kΩ * 20Hz) = 0.397µF; use 0.39µF.

The high frequency pole is determined by the product of the desired frequency pole, fH, and the differential gain, A_V. With an AV_V = 1 and f_H = 100kHz, the resulting GBWP = 100kHz which is much smaller than the LM4925GBWP of 3MHz. This example displays that if a designer has a need to design an amplifier with higher differential gain, the LM4925can still be used without running into bandwidth limitations.

LM4925 BOARD ARTWORK

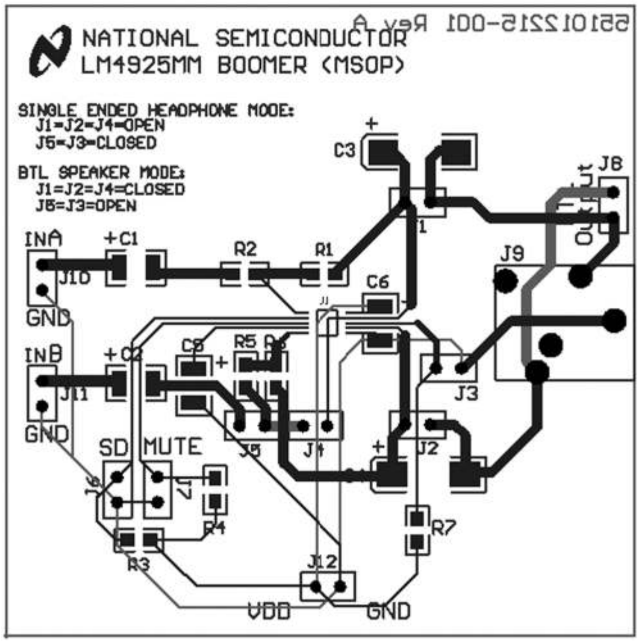


Figure 31. Composite View

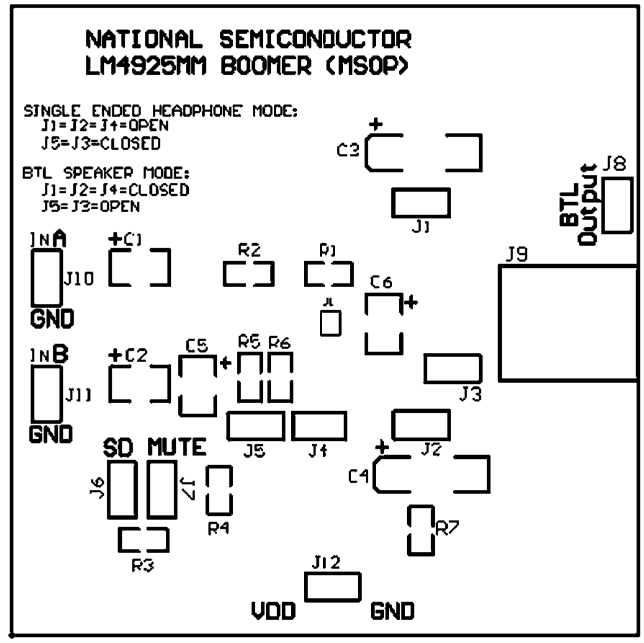


Figure 32. Silk Screen

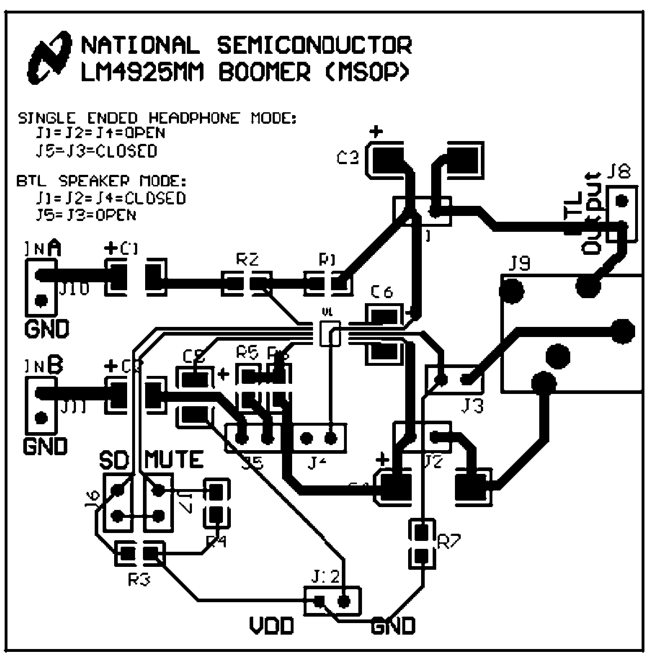


Figure 33. Top Layer

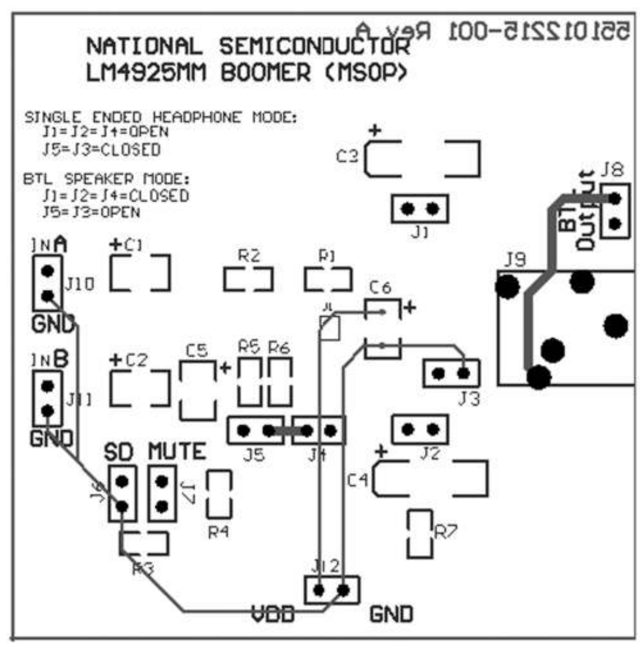


Figure 34. Bottom Layer

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4925MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		GB8	Samples
LM4925SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4925	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

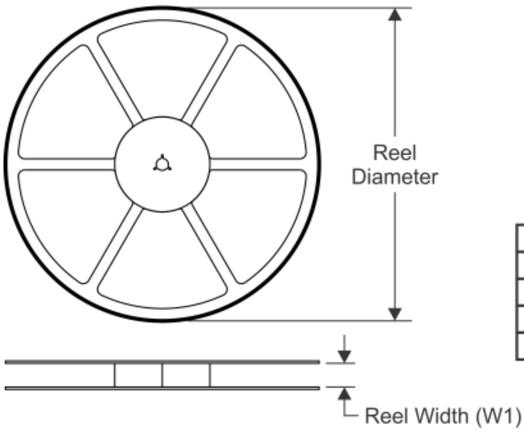
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

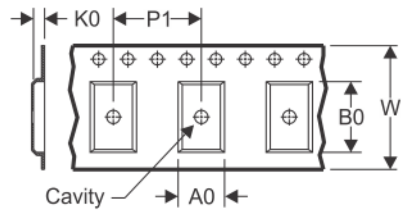
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

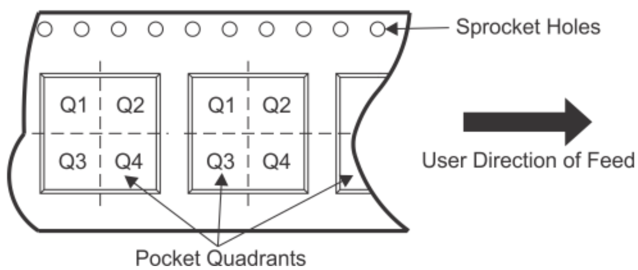


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

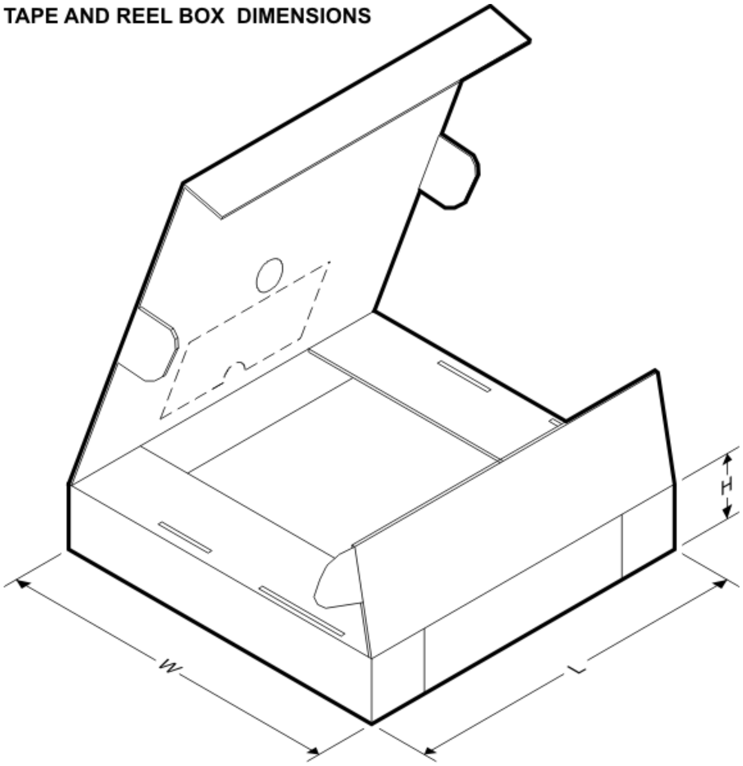
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4925MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4925SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

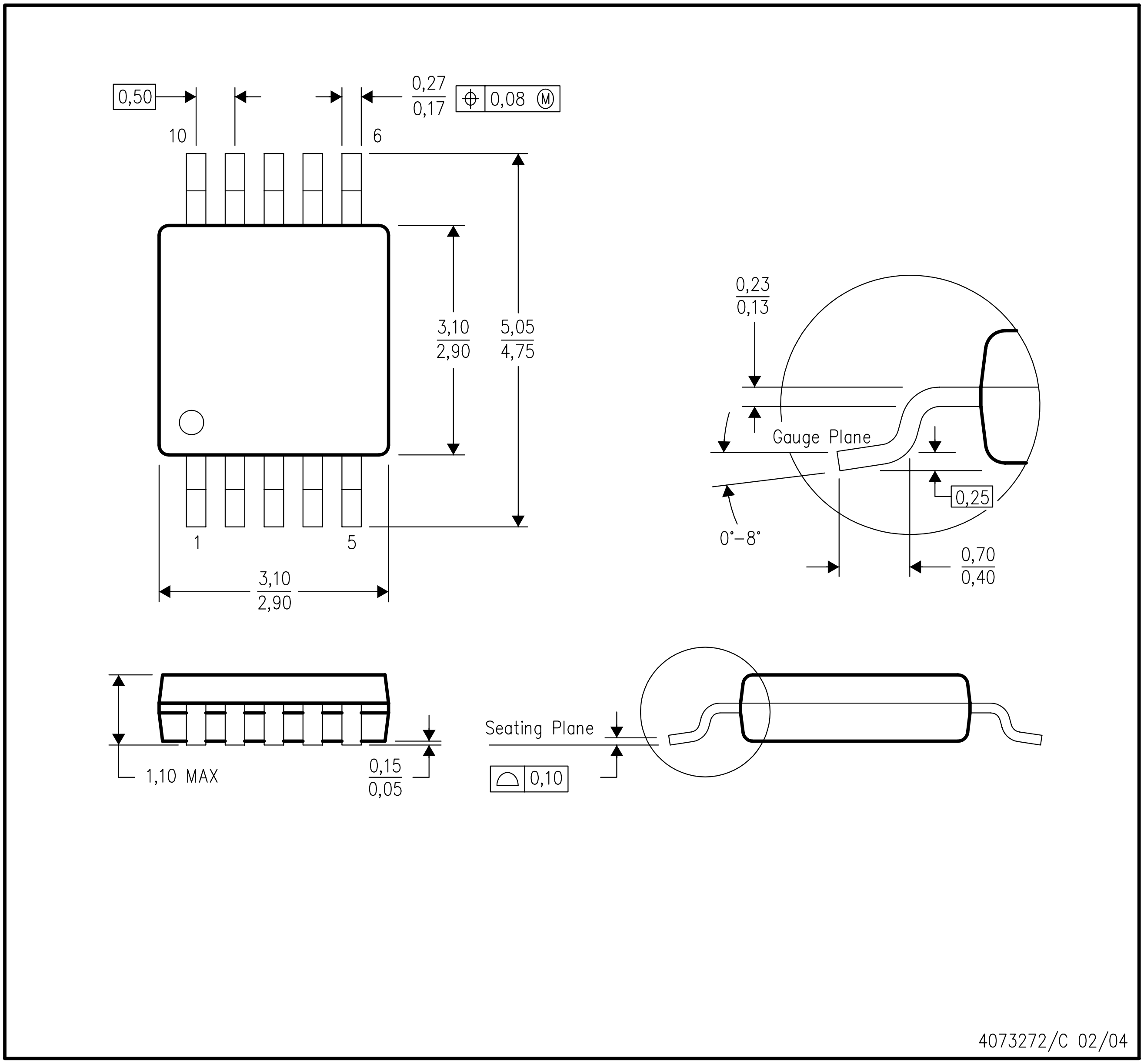
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

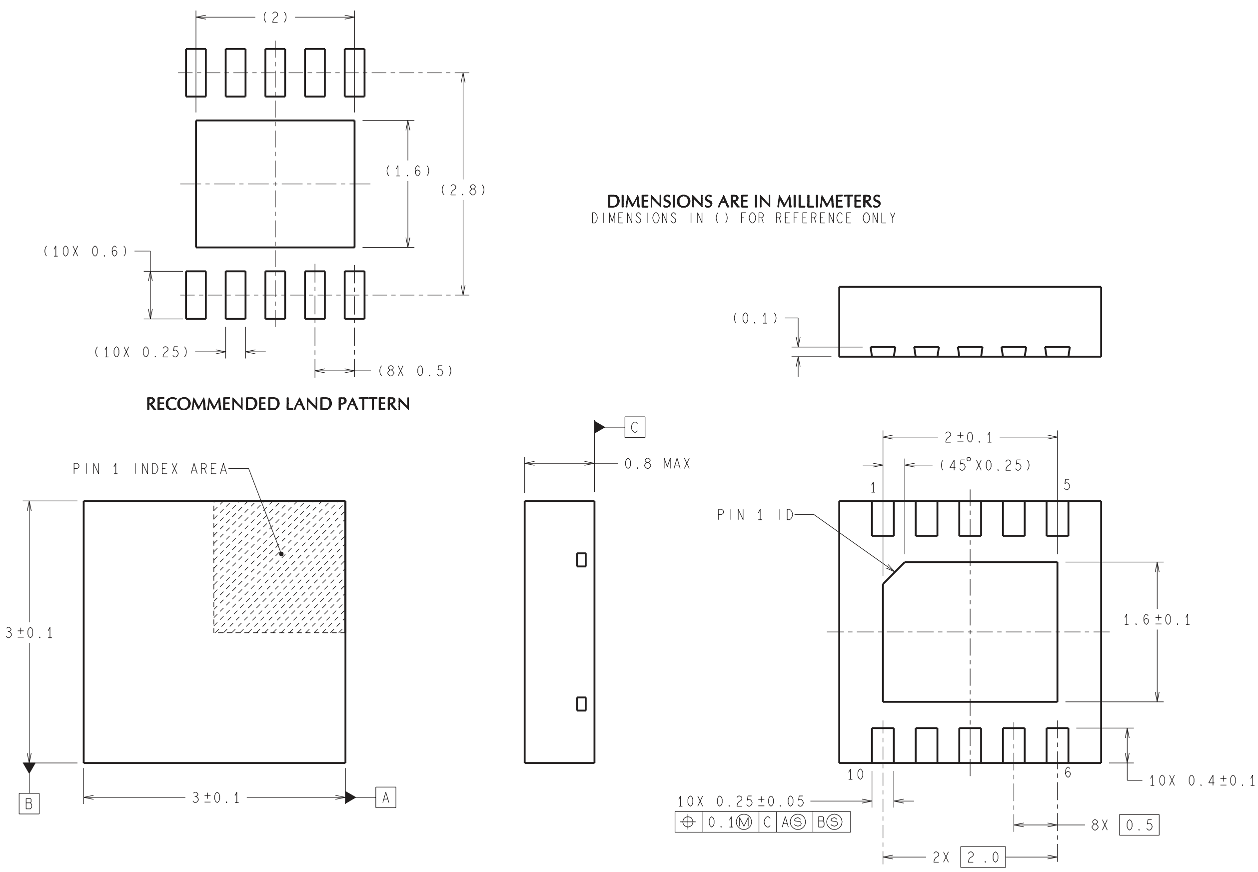
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4925MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM4925SD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.

DSC0010A



SDA10A (Rev A)

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265