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MOSFET - Power, N-Channel, SUPERFET® III, FRFET®

650 V, 40 A, 82 mΩ

NTBL082N65S3HF

ON Semiconductor®

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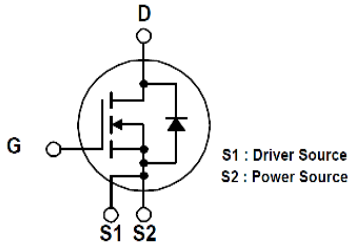
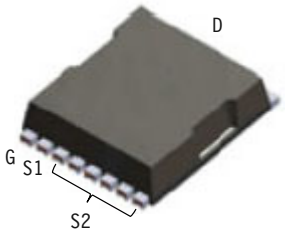
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	82 mΩ @ 10 V	40 A



N−Channel MOSFET



H−PSOF8L
CASE 100DC

Description

SUPERFET III MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency. SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability. The TOLL package offers improved thermal performance and excellent switching performance thanks to 4 pin Kelvin Source configuration and lower parasitic source inductance. TOLL offers Moisture Sensitivity Level 1 (MSL 1).

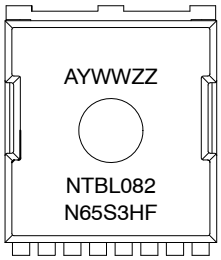
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 70 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 79 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 682 pF)
- 100% Avalanche Tested
- Kelvin Source Configuration and Low Parasitic Source Inductance
- MSL1 Qualified
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code
NTBL082N65S3HF	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25°C)	40	A
		– Continuous (T_C = 100°C)	25.5	
I_{DM}	Drain Current	– Pulsed (Note 1)	100	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		510	mJ
I_{AS}	Avalanche Current (Note 2)		4.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		3.13	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	313	W
		– Derate Above 25°C	2.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le$ 20 A, $V_{DD} \le$ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Steady State	0.40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Steady State (Note 4)	43	

4. Device on 1 in^2, 2 oz copper pad on 1.5 x 1.5 in. board of FR−4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
NTBL082N65S3HF	NTBL082N65S3HF	H−PSOF8L	13 mm	24 mm	2000 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.7	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, T_C = 125°C	–	124	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A	–	70	82	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A	–	24	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	3330	–	pF
C_{oss}	Output Capacitance		–	70	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	682	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	130	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 10 V (Note 5)	–	79	–	nC
Q_{gs}	Gate to Source Gate Charge		–	24	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	32	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.8	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 10 V R_g = 3 Ω (Note 5)	–	29.4	–	ns
t_r	Turn-On Rise Time		–	14.5	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	70.9	–	ns
t_f	Turn-Off Fall Time		–	2.47	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	40	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	100	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs	–	105	–	ns
Q_{rr}	Reverse Recovery Charge		–	434	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

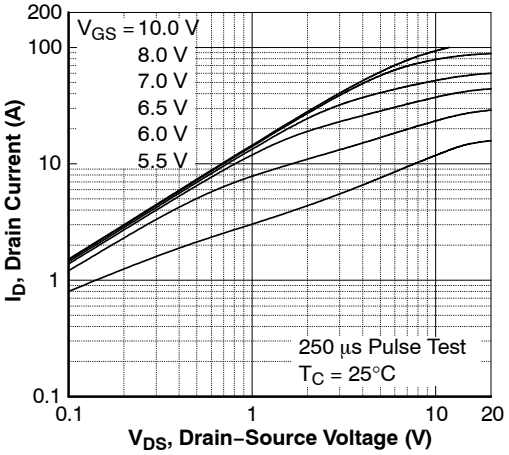


Figure 1. On−Region Characteristics

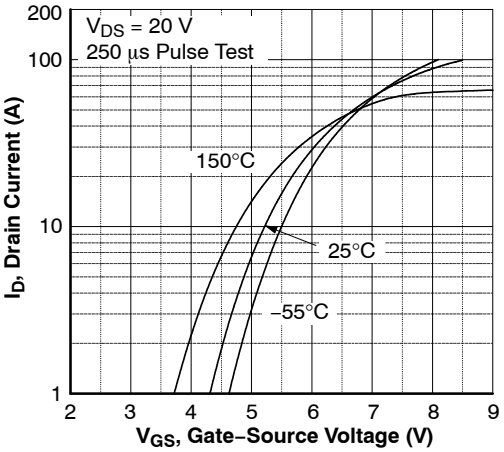


Figure 2. Transfer Characteristics

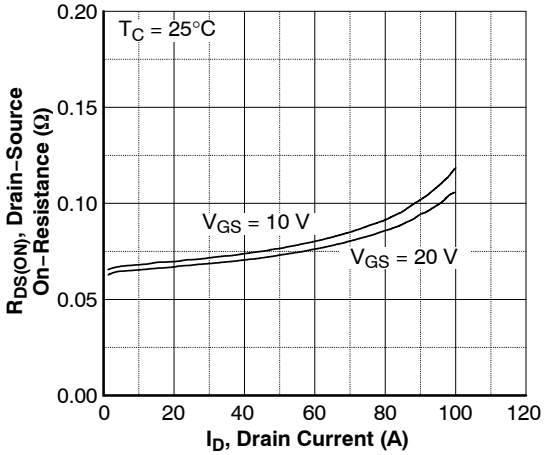


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

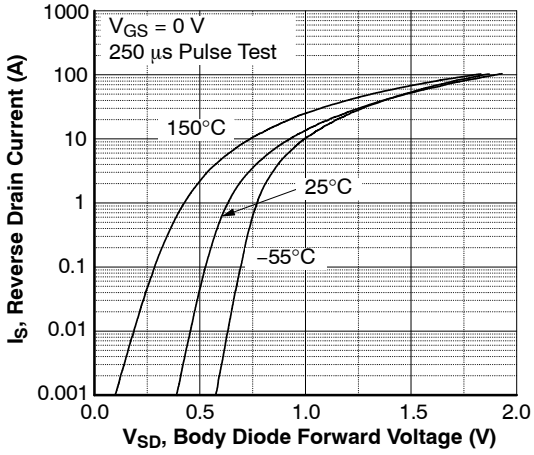


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

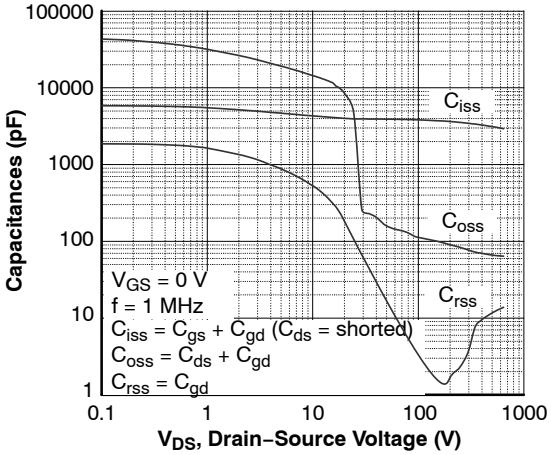


Figure 5. Capacitance Characteristics

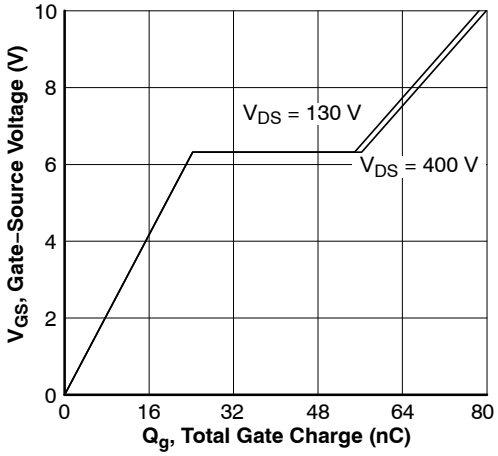


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

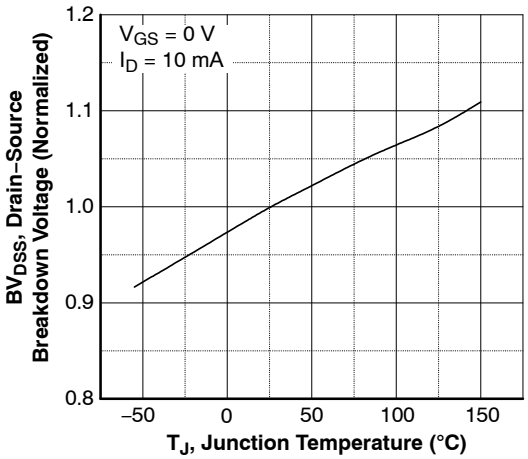


Figure 7. Breakdown Voltage Variation vs. Temperature

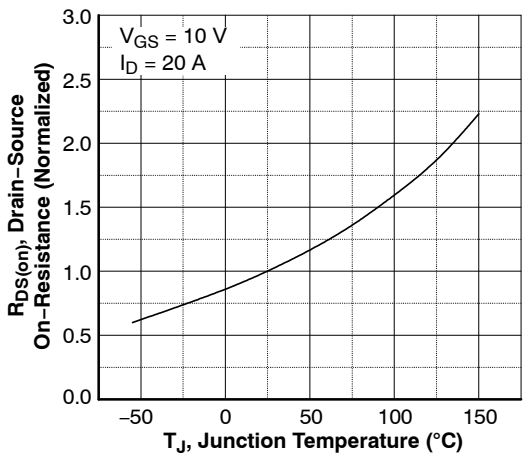


Figure 8. On−Resistance Variation vs. Temperature

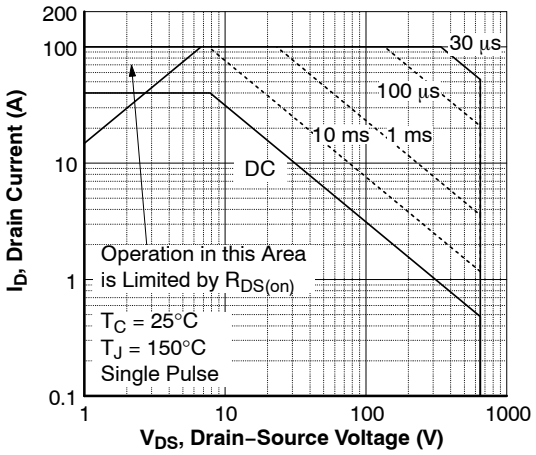


Figure 9. Maximum Safe Operating Area

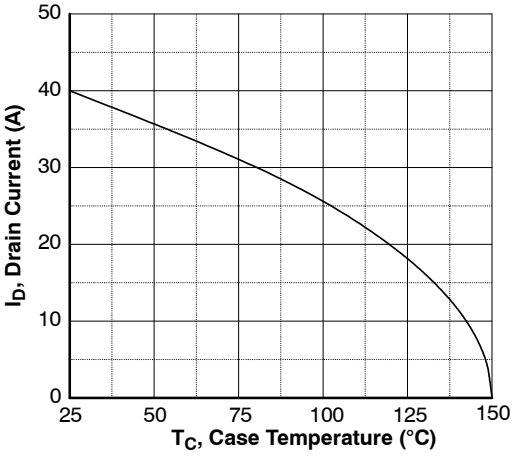


Figure 10. Maximum Drain Current vs. Case Temperature

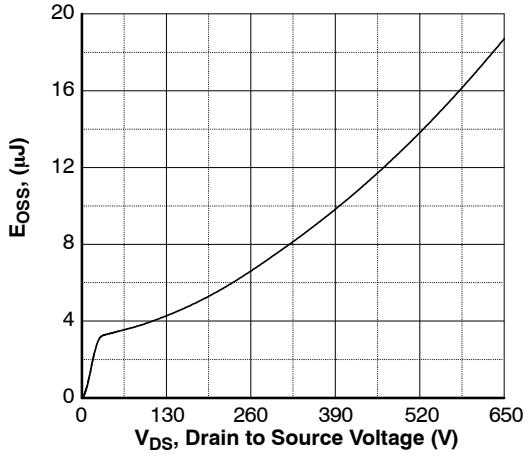


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

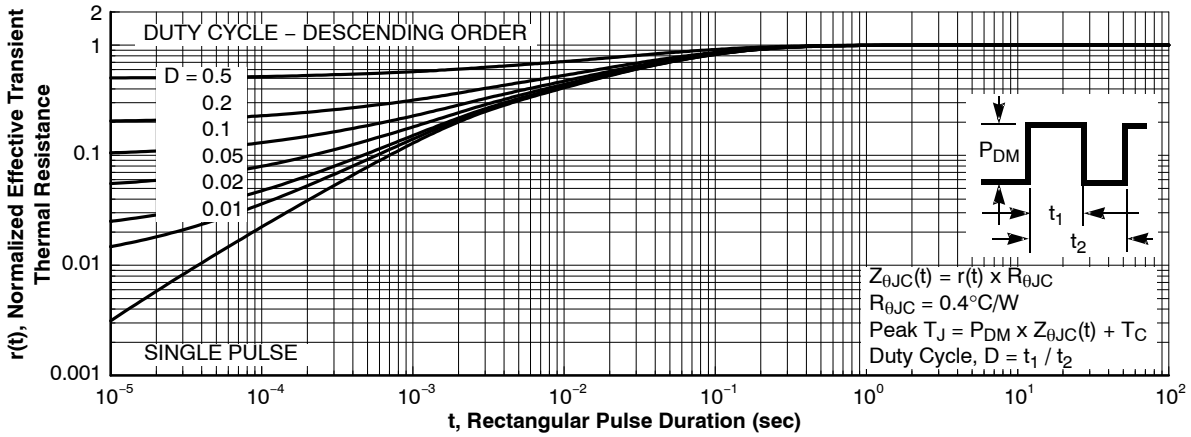


Figure 12. Transient Thermal Response Curve

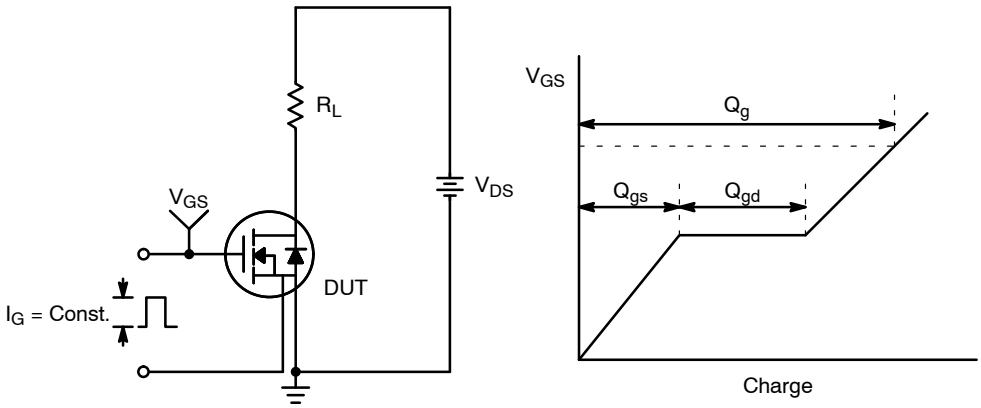


Figure 13. Gate Charge Test Circuit & Waveform

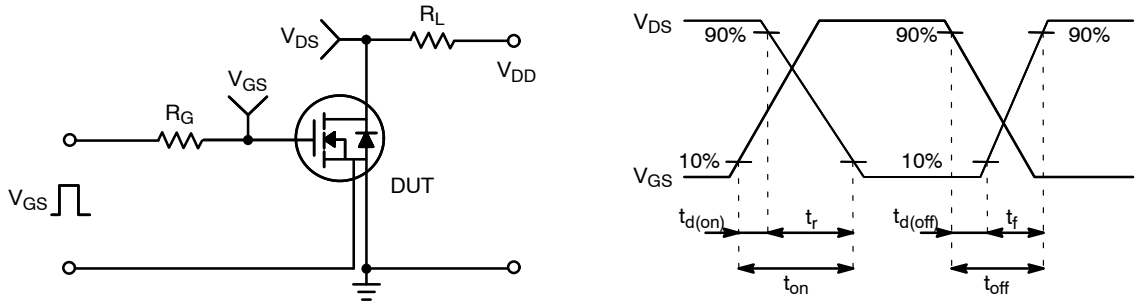


Figure 14. Resistive Switching Test Circuit & Waveforms

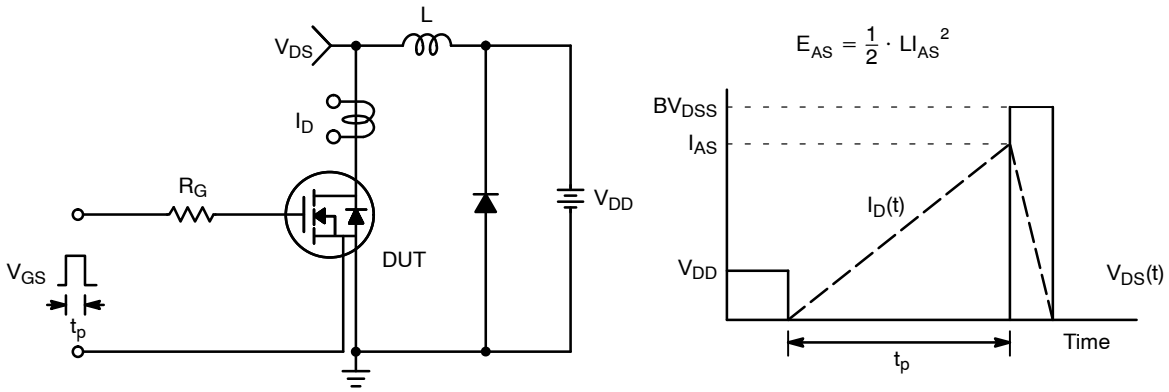


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

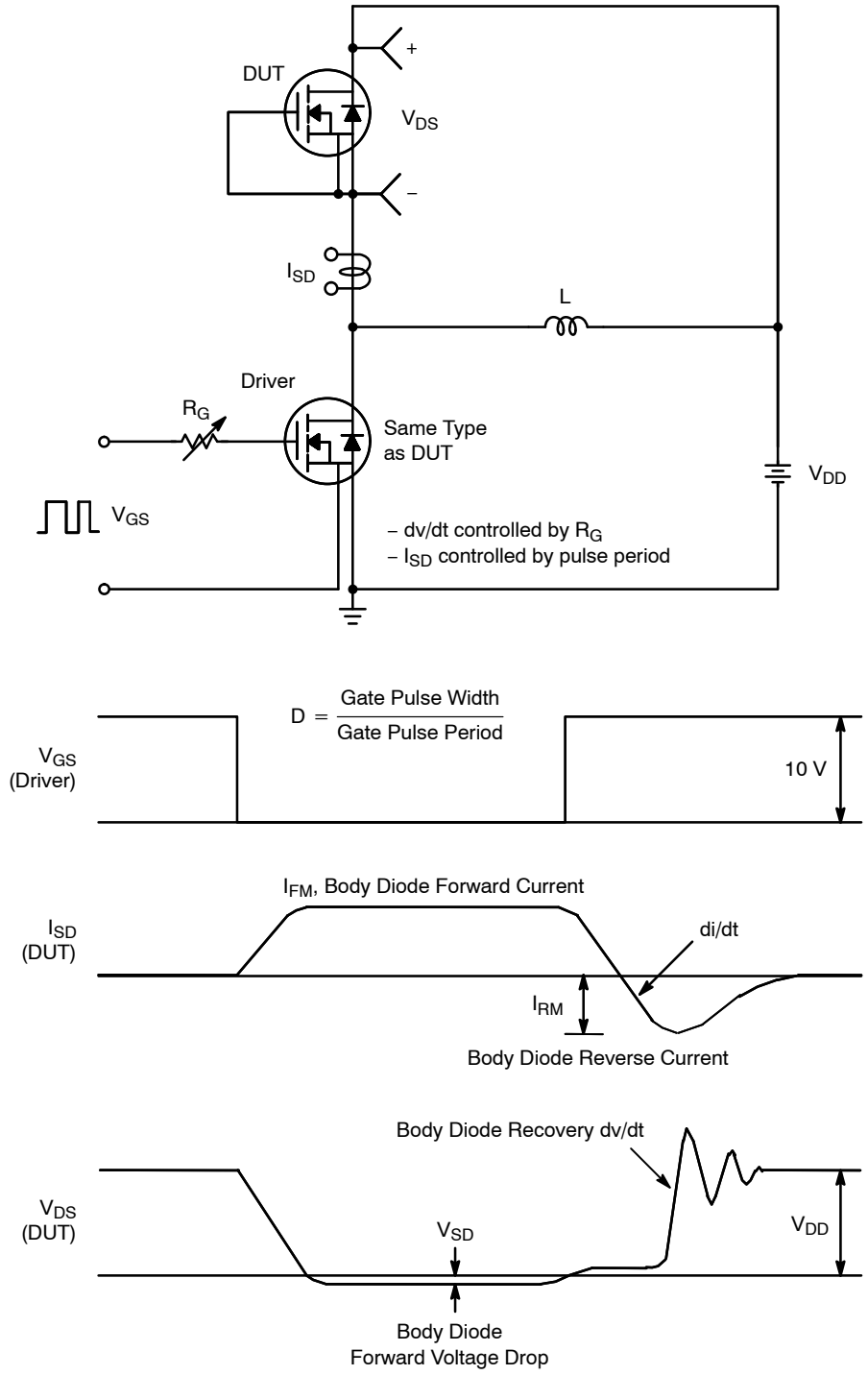
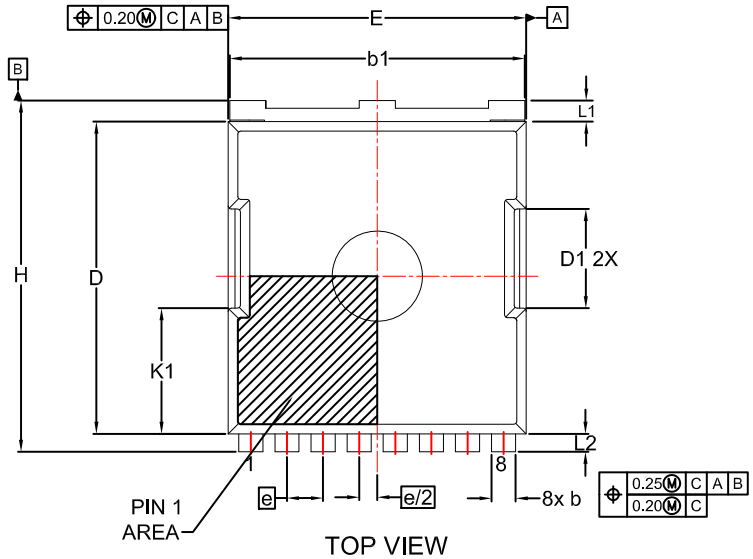


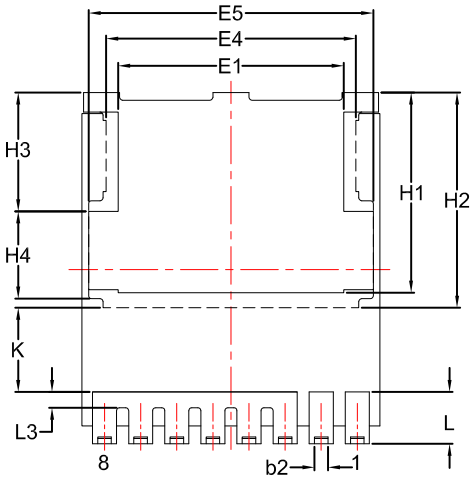
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE DIMENSIONS

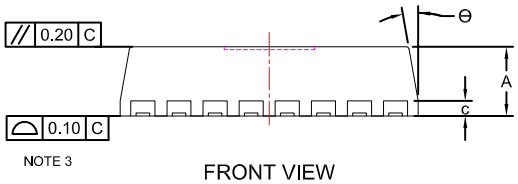
H−PSOF8L 9.90x11.68, 1.20P
CASE 100DC
ISSUE O



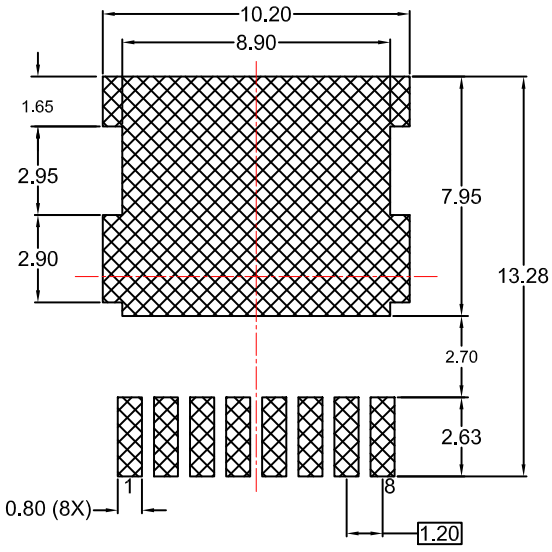
TOP VIEW



BOTTOM VIEW



FRONT VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.46	0.56
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1		3.30	
E	9.80	9.90	10.80
E1	7.40	7.50	7.60
E4		8.30	
E5		9.49	
e		1.20 BSC	
e/2		0.60 BSC	
H	11.58	11.68	11.78
H1	6.55	6.65	6.75
H2	7.05	7.15	7.25
H3		3.60	
H4		3.26	
K	2.70	2.80	2.90
K1		4.18	
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.10	1.20	1.30
Θ		10° REF.	

PUBLICATION ORDERING INFORMATION

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