

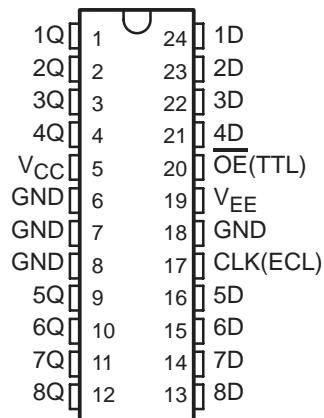
# SN100KT5574

## OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

SDZS009 – D3418, JANUARY 1990

- 100K Compatible
- ECL Clock and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin  $V_{CC}$ ,  $V_{EE}$ , and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include “Small Outline” Packages and Standard Plastic DIPs

DW OR NT PACKAGE  
(TOP VIEW)



### description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 100K ECL signal environment and a TTL signal environment.

This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN100KT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

A buffered output-enable input ( $\overline{OE}$ ) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input  $\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN100KT5574 is characterized for operation from 0°C to 85°C.

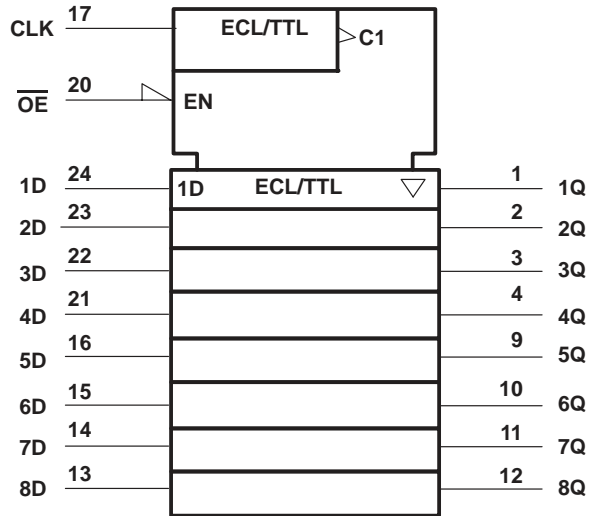
FUNCTION TABLE

INPUTS			OUTPUT (TTL)
$\overline{OE}$	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	$Q_0$
H	X	X	Z

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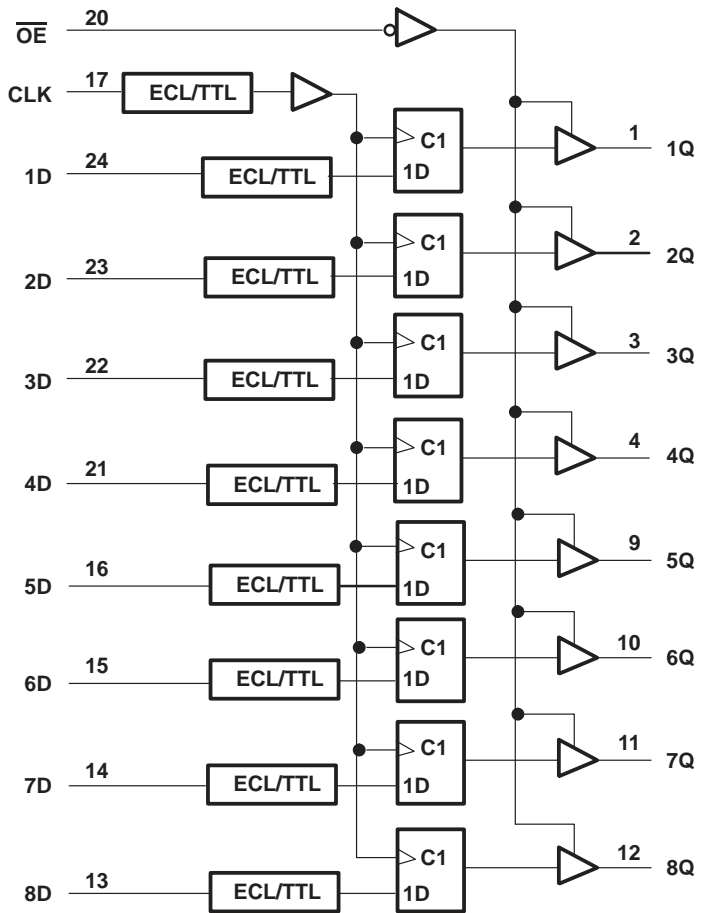
## OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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## OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IK</sub>	OE only	V <sub>CC</sub> = 4.5 V,	V <sub>EE</sub> = -4.2 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V,	V <sub>EE</sub> = -4.5 V ± 0.3 V,	I <sub>OH</sub> = -3 mA	2.4	3.3		V
		V <sub>CC</sub> = 4.5 V,	V <sub>EE</sub> = -4.5 V ± 0.3 V,	I <sub>OH</sub> = -15 mA	2	3.1		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	V <sub>EE</sub> = -4.5 V ± 0.3 V,	I <sub>OL</sub> = 48 mA		0.38	0.55	V
I <sub>I</sub>	OE only	V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>I</sub> = 7 V			0.1	mA
I <sub>IH</sub>	OE only	V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub>	OE only	V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>I</sub> = 0.5 V			-0.5	mA
I <sub>IH</sub>	Data inputs and CLK	V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>IH</sub> = -840 mV			350	μA
I <sub>IL</sub>	Data inputs and CLK	V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>IL</sub> = -1810 mV	0.50			μA
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>O</sub> = 2.7 V			50	μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>O</sub> = 0.5 V			-50	μA
I <sub>OS</sub> <sup>‡</sup>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V,	V <sub>O</sub> = 0 V	-100		-225	mA
I <sub>CCH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V			66	95	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V			76	110	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V			74	106	mA
I <sub>EE</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.8 V			-43	-61	mA
C <sub>i</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.5 V			5		pF
C <sub>o</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>EE</sub> = -4.5 V			7		pF

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, V<sub>EE</sub> = -4.5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

### timing requirements

		V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>EE</sub> = -4.2 V to -4.8 V, T <sub>A</sub> = MIN to MAX <sup>§</sup>		UNIT
		MIN	MAX	
t <sub>w</sub>	Pulse duration	CLK high	4	ns
		CLK low	4	
t <sub>h</sub>	Hold time after CLK↑	Data high	1	ns
		Data low	1	
t <sub>su</sub>	Setup time before CLK↑	Data high	1	ns
		Data low	1	

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN100KT5574**  
**OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE**  
**EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS**

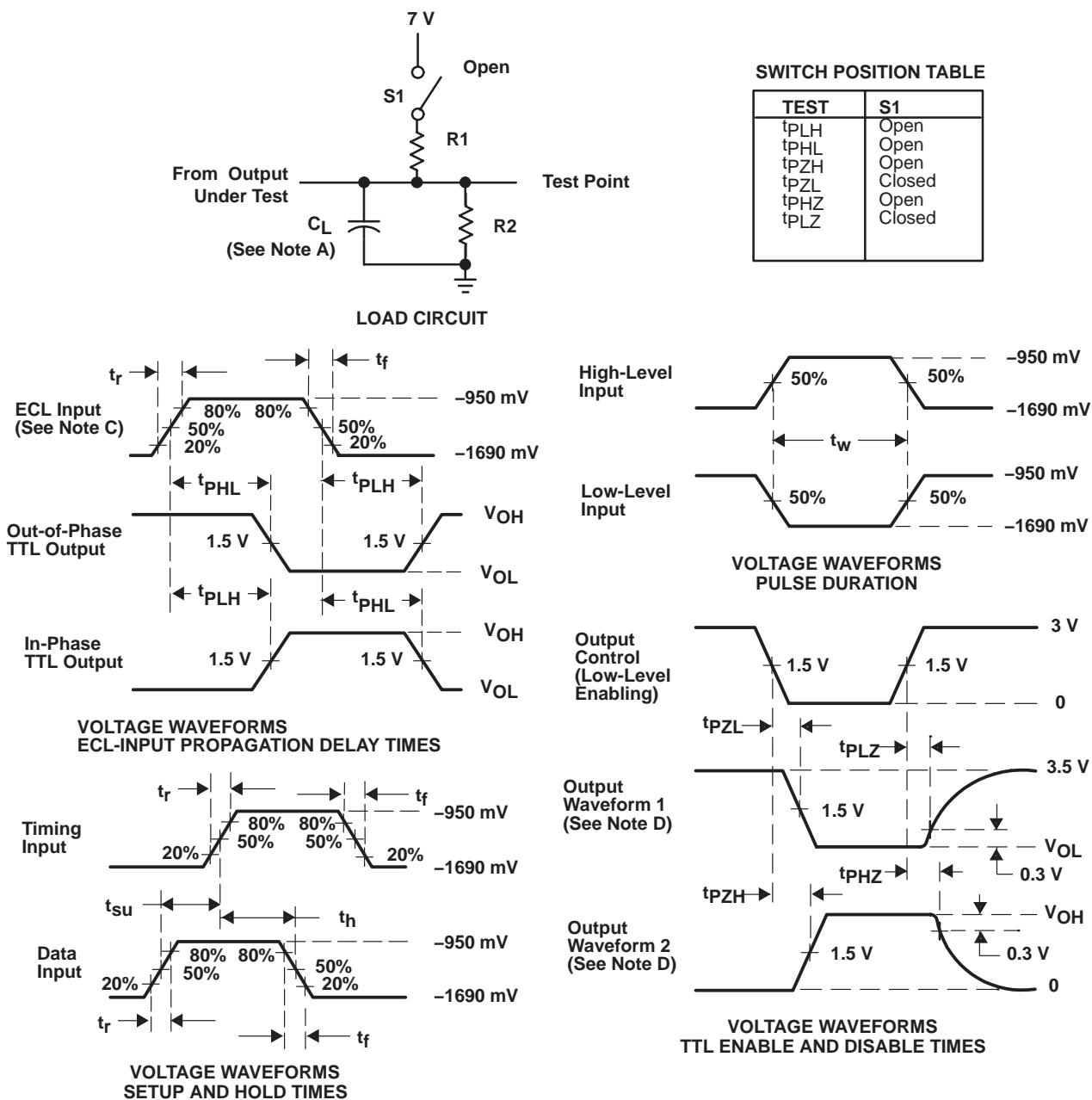
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
f <sub>max</sub>			200	300		MHz
t <sub>PLH</sub>	CLK	Q	2.3	4.1	7	ns
t <sub>PHL</sub>			2.9	4.6	7.4	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	1.9	3.6	6.3	ns
t <sub>PZL</sub>			2.7	4.8	7.7	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	2.1	3.9	6.1	ns
t <sub>PLZ</sub>			0.5	3.4	6.3	

† All typical values are at V<sub>CC</sub> = 5 V, V<sub>EE</sub> = -4.5 V, T<sub>A</sub> = 25°C.

# SN100KT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. For TTL inputs, input pulses are supplied by generators having the following characteristics PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>0</sub> = 50 Ω, t<sub>r</sub> ≤ 0.7 ns, t<sub>f</sub> ≤ 0.7 ns.  
 D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 E. The outputs are measured one at a time with one transition per measurement.

figure 1. load circuit and voltage waveforms

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