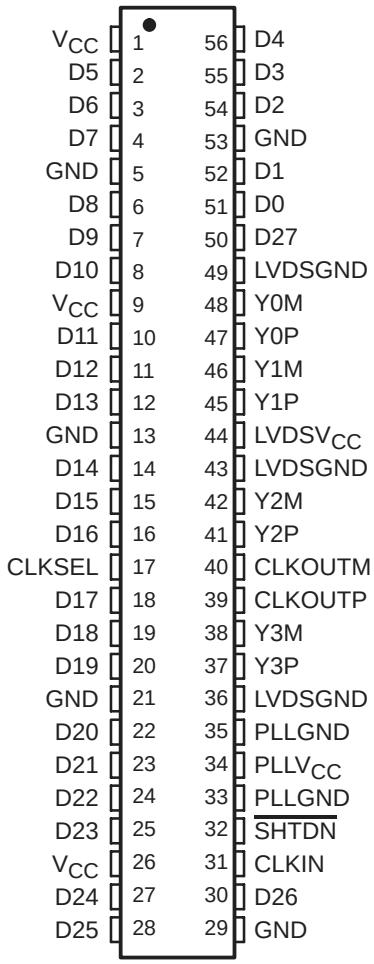
# SN75LVDS83
# FlatLink™ TRANSMITTER

SLLS271I − MARCH 1997 − REVISED MAY 2009

- **4:28 Data Channel Compression at up to 238 MBytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **28 Data Channels and Clock-In Low-Voltage TTL**
- **4 Data Channels and Clock-Out Low-Voltage Differential**
- **Operates From a Single 3.3-V Supply With 250 mW (Typ)**
- **ESD Protection Exceeds 6 kV**
- **5-V Tolerant Data Inputs**
- **Selectable Rising or Falling Edge-Triggered Inputs**
- **Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range . . . 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Outputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C581**

**DGG PACKAGE**
**(TOP VIEW)**




## description

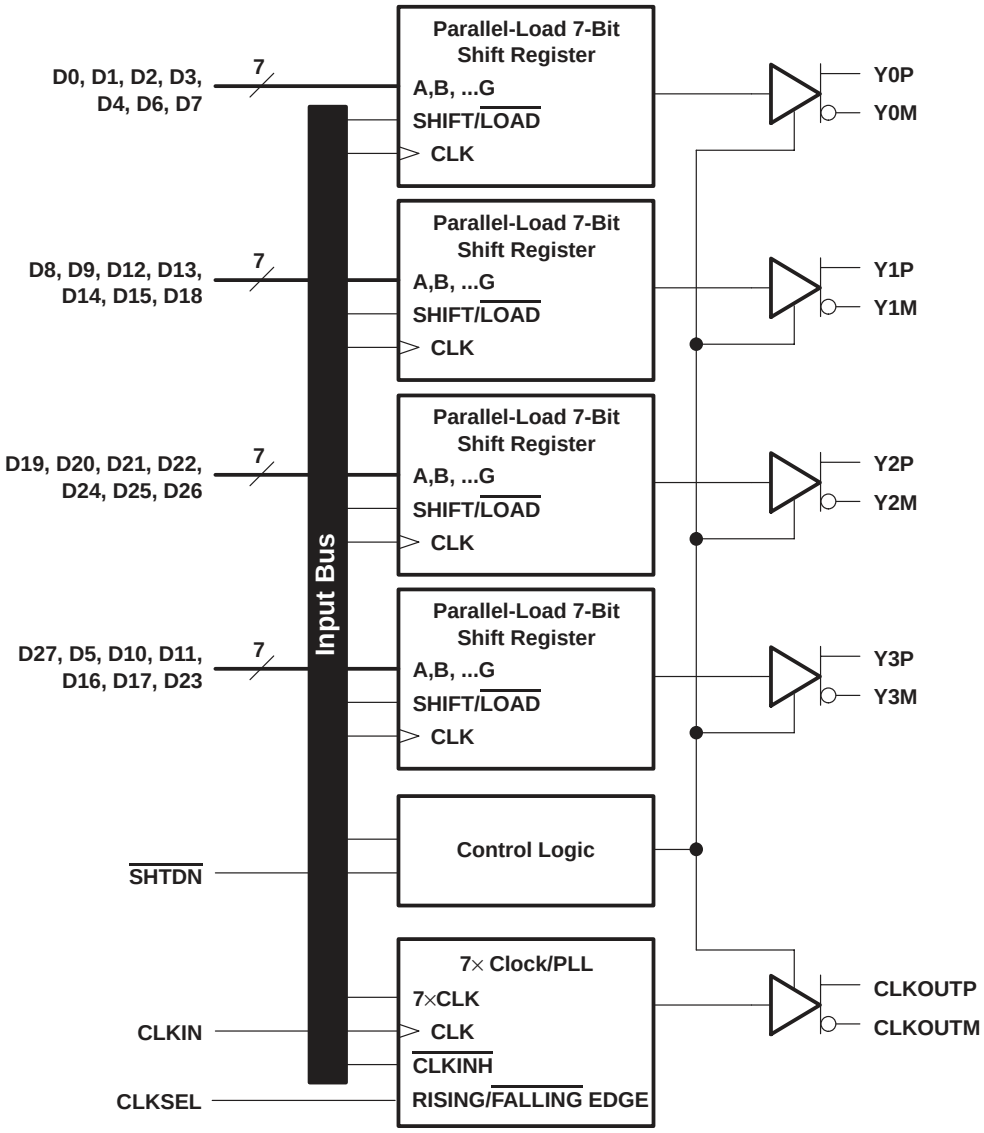
The SN75LVDS83 FlatLink transmitter contains four 7-bit parallel-load serial-out shift registers, a 7× clock synthesizer, and five low-voltage differential-signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82. The SN75LVDS83 can also be used in 21-bit links with the SN75LVDS86 receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected by way of the clock select (CLKSEL) terminal. The frequency of CLKIN is multiplied seven times (7×) and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

The SN75LVDS83 requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only user intervention is the possible use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level signal on $\overline{\text{SHTDN}}$ clears all internal registers to a low level.

The SN75LVDS83 is characterized for operation over free-air temperature ranges of 0°C to 70°C.

## functional block diagram



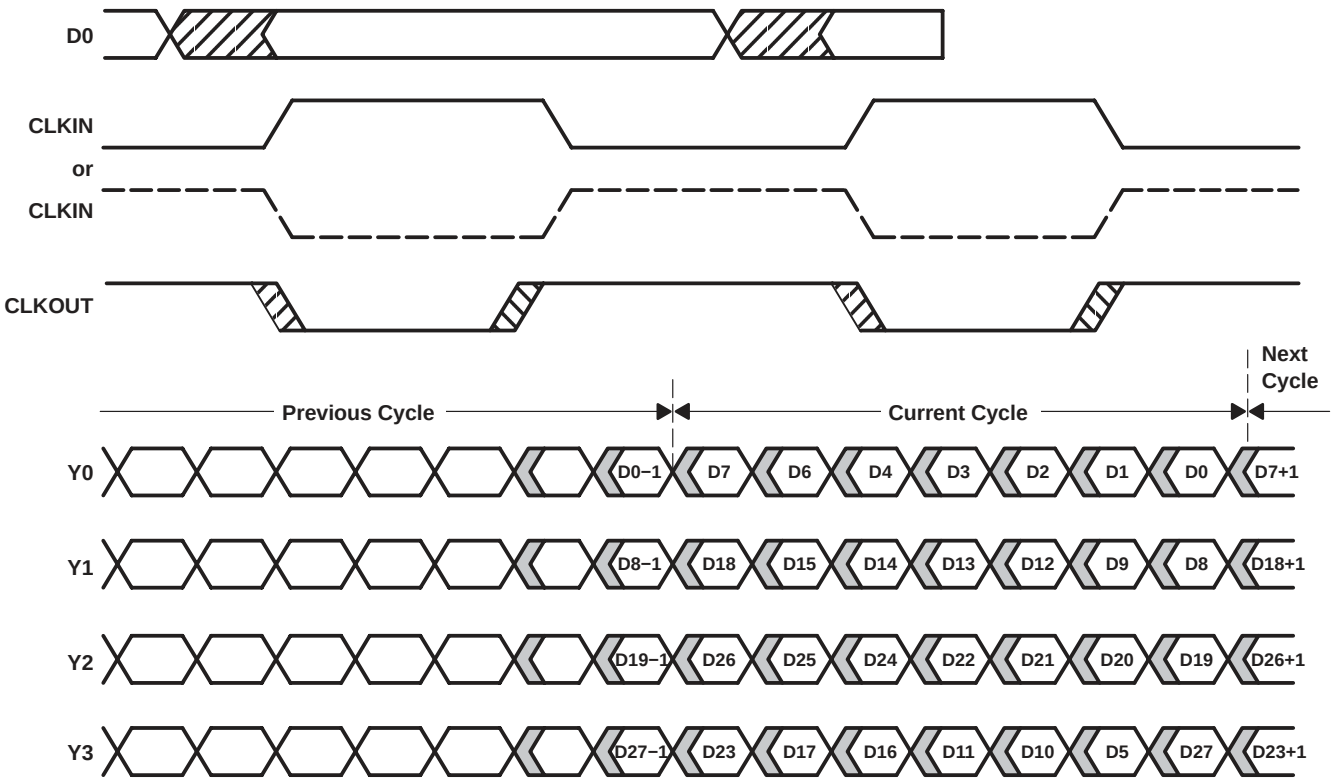
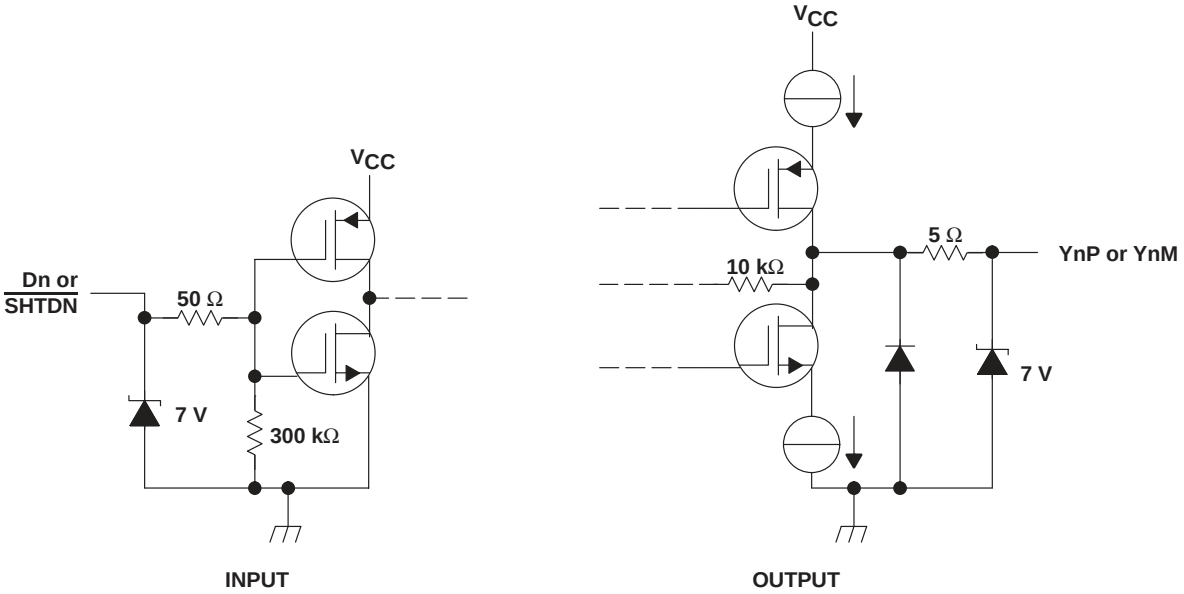



**Figure 1. SN75LVDS83 Load and Shift Timing Sequences**

## equivalent input and output schematic diagrams



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . −0.5 V to 4 V
Output voltage range, $V_O$ (all terminals) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input voltage range, $V_I$ (all terminals) . . . . . −0.5 V to 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| DGG | 1377 mW | 11.0 mW/°C | 822 mW |

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| Differential load impedance, $Z_L$ | 90 | | 132 | Ω |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## timing requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_c$ | Cycle time, input clock | 14.7 | | 32.3 | ns |
| $t_w$ | Pulse duration, high-level input clock | $0.4\,t_c$ | | $0.6\,t_c$ | ns |
| $t_t$ | Transition time, input signal | | | 5 | ns |
| $t_{su}$ | Setup time, data, D0 − D27 valid before CLKIN↑ or CLKIN↓ (see Figure 2) | 3 | | | ns |
| $t_h$ | Hold time, data, D0 − D27 valid after CLKIN↑ or CLKIN↓ (see Figure 2) | 1.5 | | | ns |

## electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT}$ | Input threshold voltage | | | 1.4 | | V |
| $\|V_{OD}\|$ | Differential steady-state output voltage magnitude | $R_L$ = 100 Ω, See Figure 3 | 247 | | 454 | mV |
| $\Delta\|V_{OD}\|$ | Change in the steady-state differential output voltage magnitude between opposite binary states | | | | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 3 | 1.125 | | 1.375 | V |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | | 150 | mV |
| $I_{IH}$ | High-level input current | $V_{IH} = V_{CC}$ | | | 25 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0 | | | ±10 | µA |
| $I_{OS}$ | Short-circuit output current | $V_{O(Yn)}$ = 0 | | | ±24 | mA |
| | | $V_{OD}$ = 0 | | | ±12 | mA |
| $I_{OZ}$ | High-impedance state output current | $V_O$ = 0 to $V_{CC}$ | | | ±10 | µA |
| $I_{CC}$ | Quiescent supply current | Disabled, All inputs at GND | | | 280 | µA |
| | | Enabled, $R_L$ = 100 Ω, Gray-scale pattern (see Figure 4), $V_{CC}$ = 3.3 V, $t_c$ = 15.38 ns | | 72 | 90 | mA |
| | | Enabled, $R_L$ = 100 Ω, Worst-case pattern (see Figure 5), $t_c$ = 15.38 ns | | 85 | 110 | mA |
| $C_I$ | Input capacitance | | | 3 | | pF |

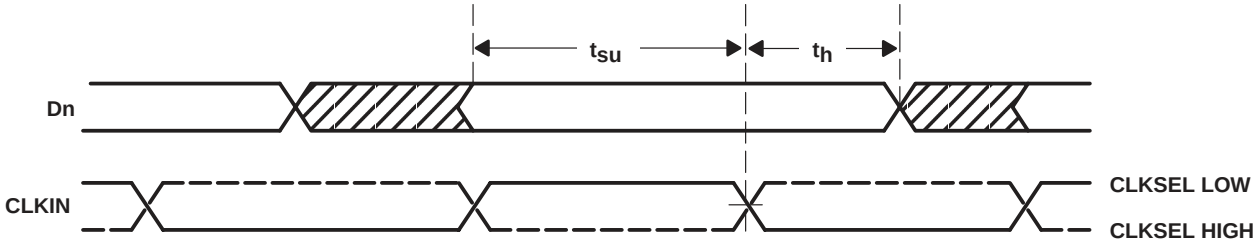
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d0}$ | Delay time, CLKOUT↑ to serial bit position 0 | $t_c$ = 15.38 ns (± 0.2%), \|Input clock jitter\| < 50 ps‡, See Figure 6 | −0.2 | 0 | 0.2 | ns |
| $t_{d1}$ | Delay time, CLKOUT↑ to serial bit position 1 | | $\frac{1}{7}t_c$ − 0.2 | | $\frac{1}{7}t_c$ + 0.2 | ns |
| $t_{d2}$ | Delay time, CLKOUT↑ to serial bit position 2 | | $\frac{2}{7}t_c$ − 0.2 | | $\frac{2}{7}t_c$ + 0.2 | ns |
| $t_{d3}$ | Delay time, CLKOUT↑ to serial bit position 3 | | $\frac{3}{7}t_c$ − 0.2 | | $\frac{3}{7}t_c$ + 0.2 | ns |
| $t_{d4}$ | Delay time, CLKOUT↑ to serial bit position 4 | | $\frac{4}{7}t_c$ − 0.2 | | $\frac{4}{7}t_c$ + 0.2 | ns |
| $t_{d5}$ | Delay time, CLKOUT↑ to serial bit position 5 | | $\frac{5}{7}t_c$ − 0.2 | | $\frac{5}{7}t_c$ + 0.2 | ns |
| $t_{d6}$ | Delay time, CLKOUT↑ to serial bit position 6 | | $\frac{6}{7}t_c$ − 0.2 | | $\frac{6}{7}t_c$ + 0.2 | ns |
| $t_{sk(o)}$ | Output skew, $t_n - \frac{n}{7}t_c$ | | −0.2 | | 0.2 | ns |
| $t_{d7}$ | Delay time, CLKIN↓ to CLKOUT↑ | $t_c$ = 18.51 ns (± 0.2%), \|Input clock jitter\| < 50 ps‡, See Figure 6 | 3.75 | 5.6 | 7.75 | ns |
| $\Delta t_{c(o)}$ | Cycle time, output clock jitter§ | $t_c$ = 15.38 ± 0.75 sin (2π500E3t) + 0.05 ns, See Figure 7 | | ±70 | | ps |
| | | $t_c$ = 15.38 ± 0.75 sin (2π3E6t) + 0.05 ns, See Figure 7 | | ±187 | | ps |
| $t_w$ | Pulse duration, high-level output clock | | | $\frac{4}{7}t_c$ | | ns |
| $t_t$ | Transition time, differential output ($t_r$ or $t_f$) | See Figure 3 | 260 | 700 | 1500 | ps |
| $t_{en}$ | Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid) | See Figure 8 | | 1 | | ms |
| $t_{dis}$ | Disable time, $\overline{SHTDN}$↓ to off state (CLKOUT low) | See Figure 9 | | 250 | | ns |

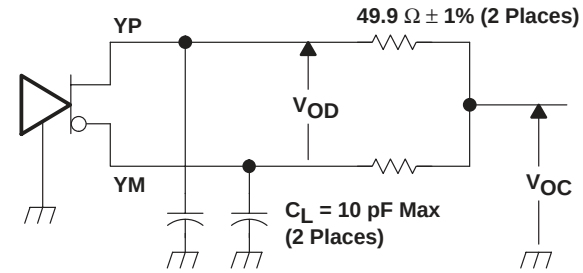
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ |Input clock jitter| is the magnitude of the change in the input clock period.
§ Output clock jitter is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

## PARAMETER MEASUREMENT INFORMATION



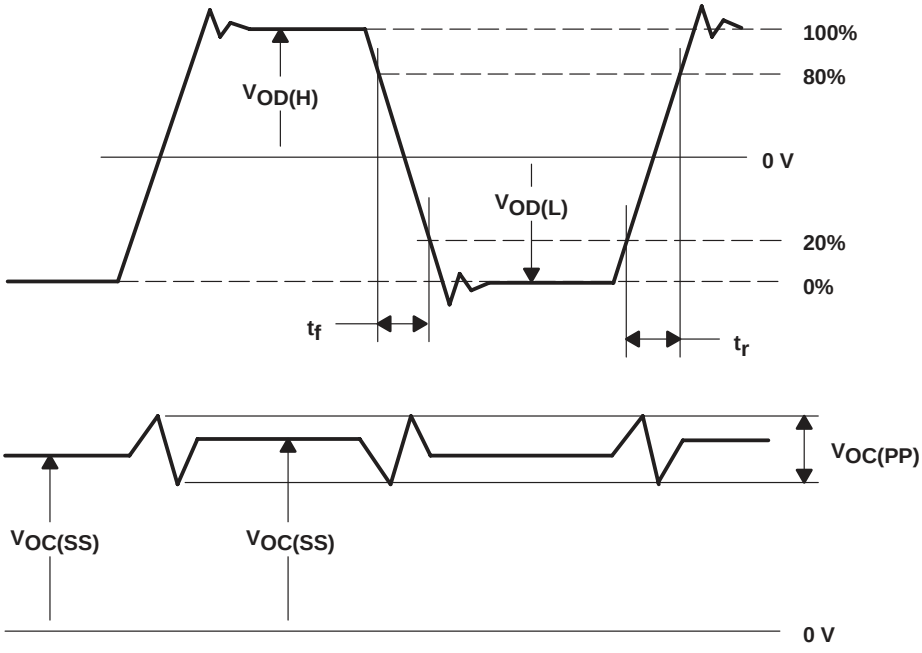

NOTE A: All input timing is defined at 1.4 V on an input signal with a 10%-to-90% rise or fall time of less than 5 ns.

**Figure 2. Setup and Hold Time Waveforms**




NOTE A: The lumped instrumentation capacitance for any single-ended voltage measurement is less than or equal to 10 pF. When making measurements at YP or YM, the complementary output is similarly loaded.

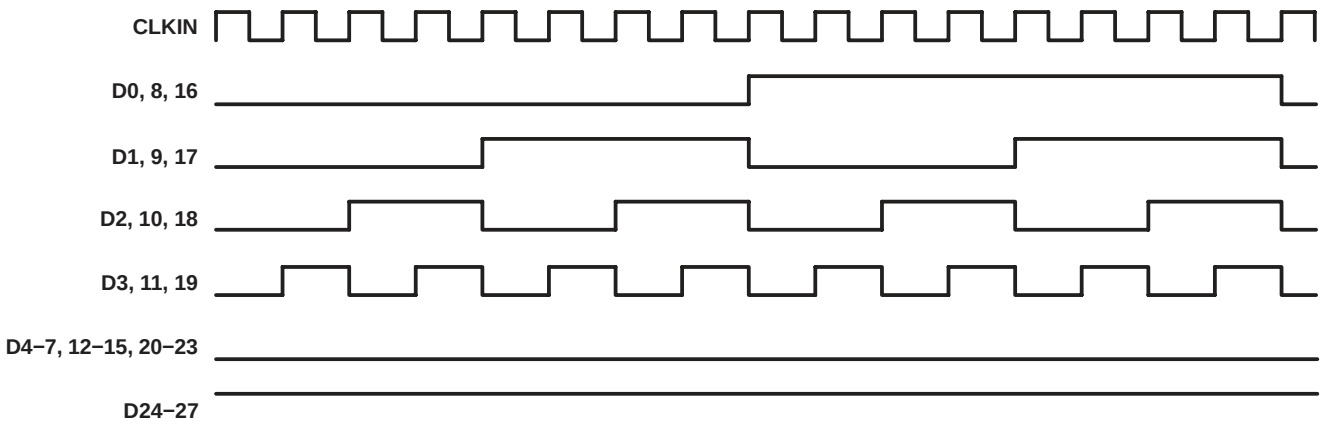
**(a) SCHEMATIC**




**(b) WAVEFORMS**

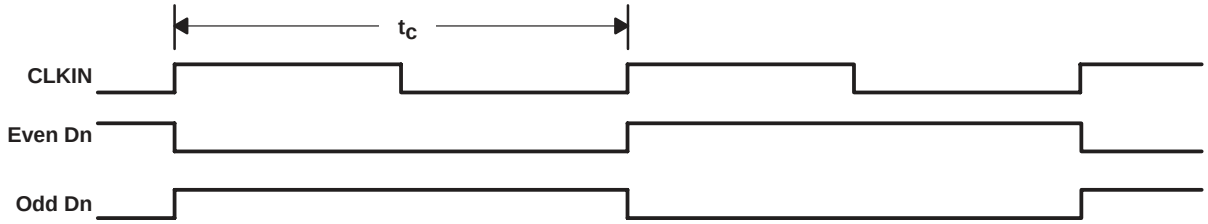
**Figure 3. Test Load and Voltage Waveforms for LVDS Outputs**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern. Pattern with CLKSEL low shown.

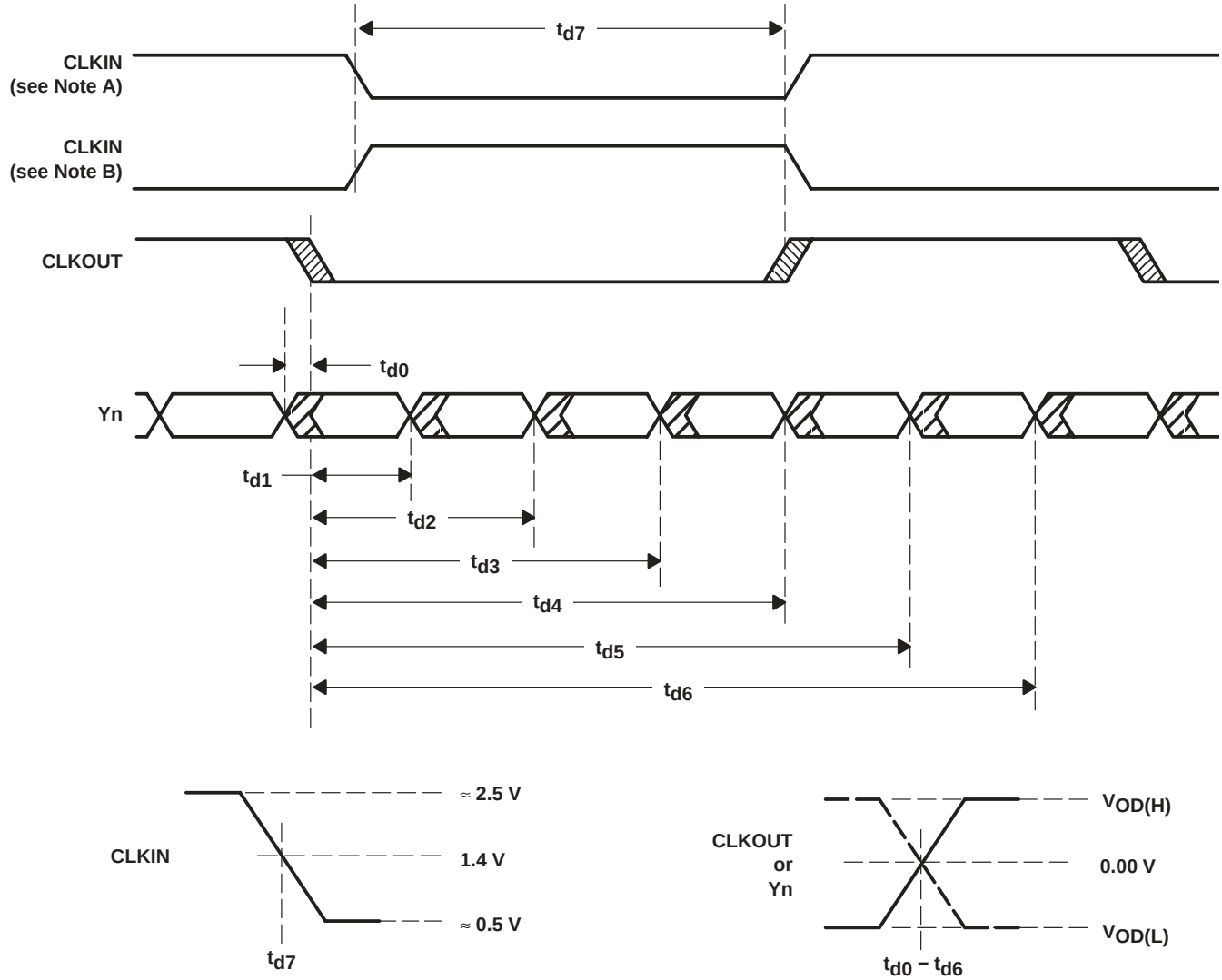
**Figure 4. 16-Grayscale Test-Pattern Waveforms**




NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs. Pattern with CLKSEL low shown.

**Figure 5. Worst-Case Test-Pattern Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. This wave form is valid when CLKSEL is low.
B. This wave form is valid when CLKSEL is high.

**Figure 6. SN75LVDS83 Timing Waveforms**

## PARAMETER MEASUREMENT INFORMATION

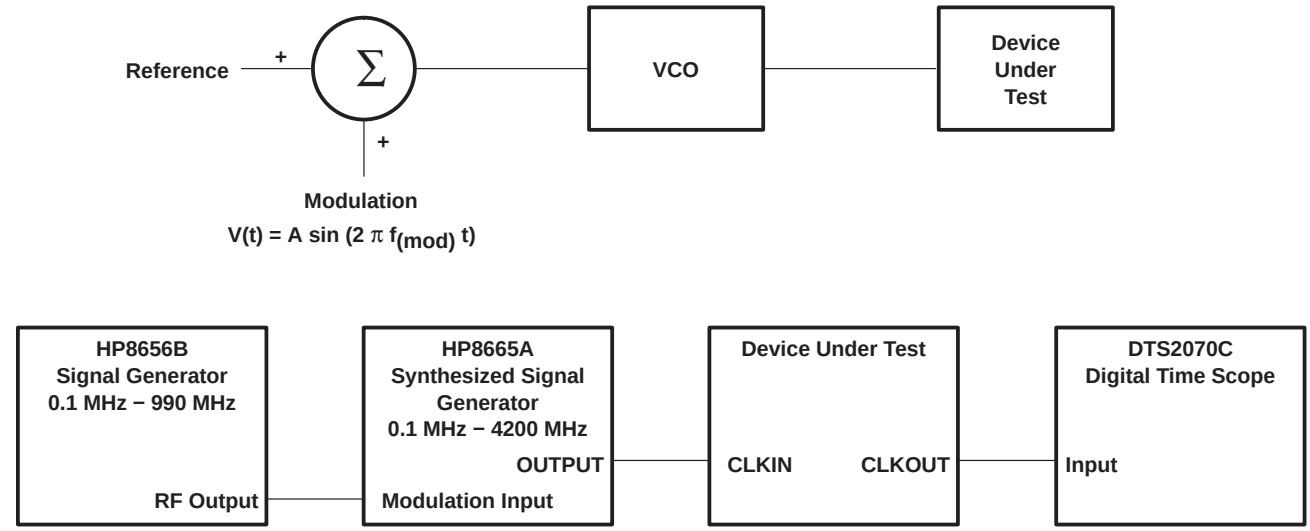



**Figure 7. Output Clock Jitter Testing**

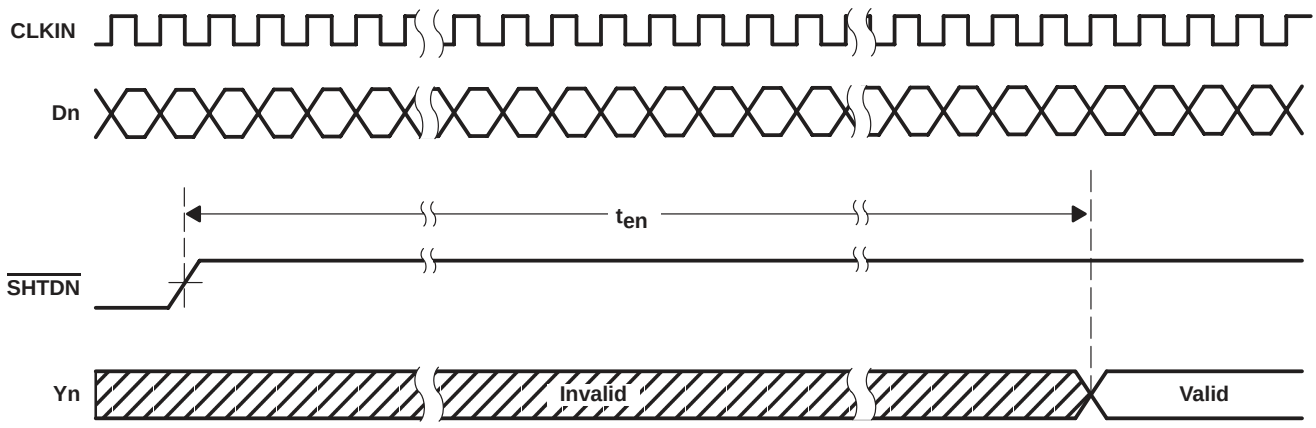



**Figure 8. Enable Time Waveforms**

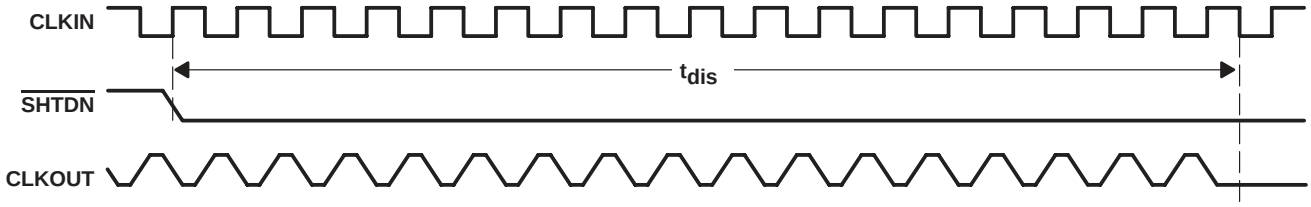



**Figure 9. Disable Time Waveforms**

## TYPICAL CHARACTERISTICS

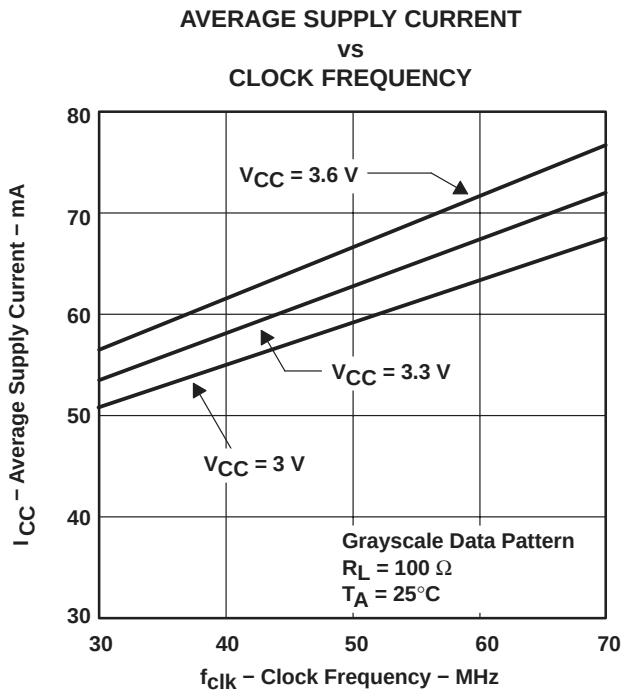



**Figure 10**

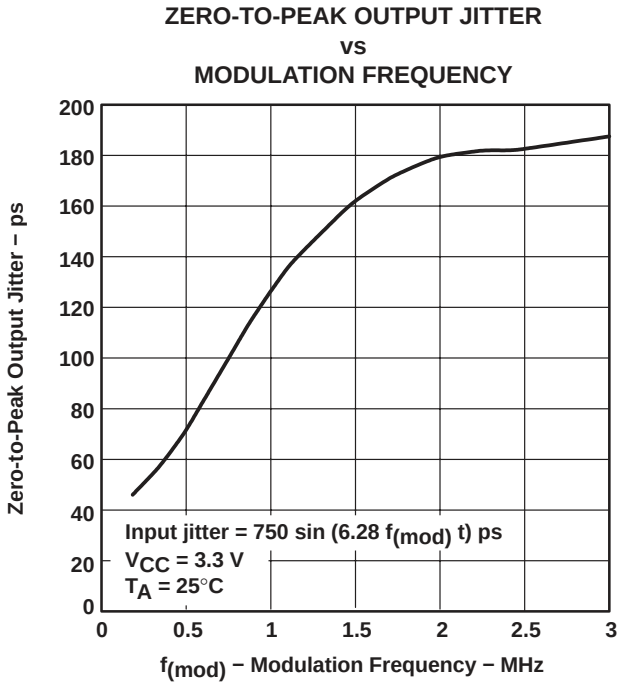
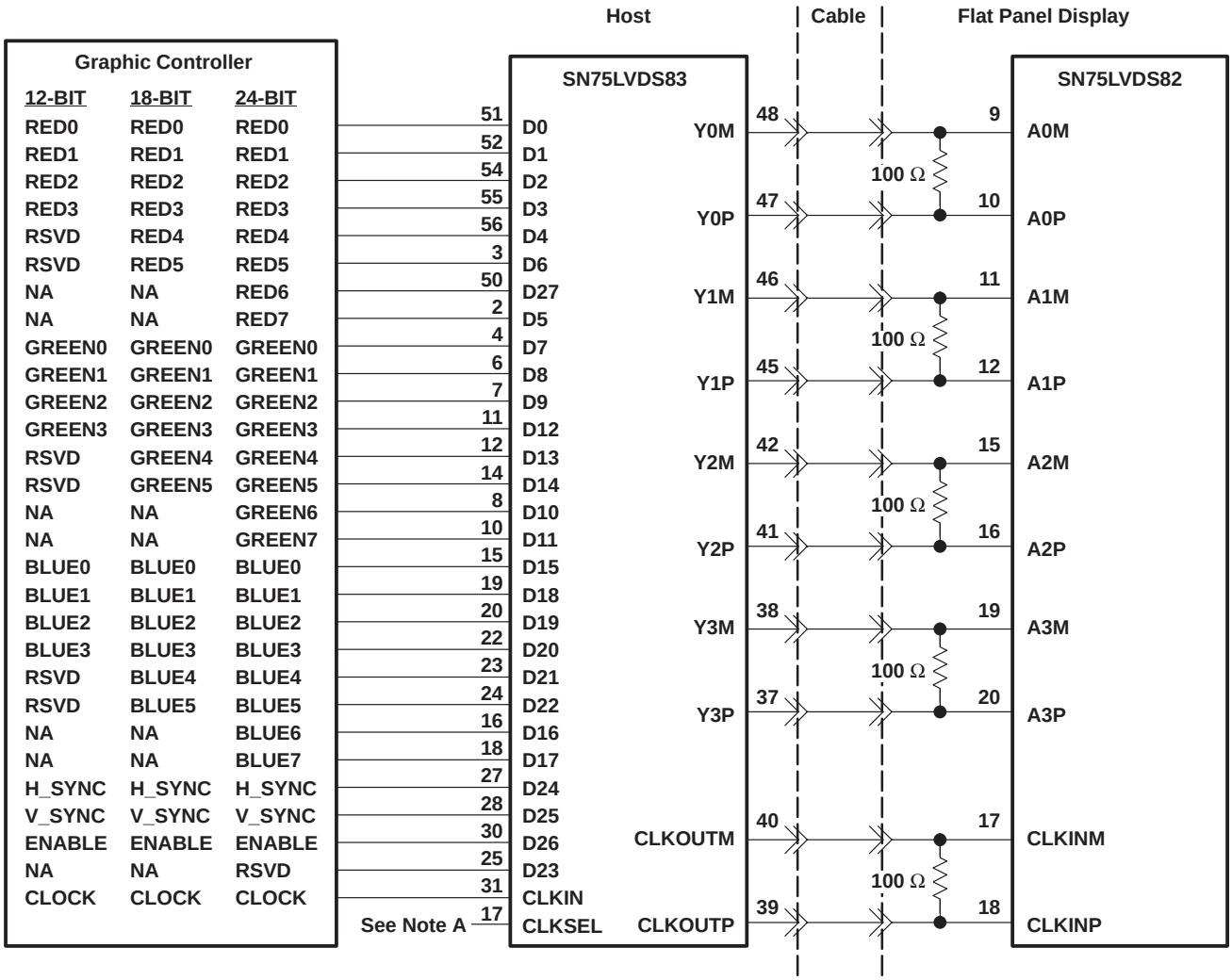



**Figure 11**

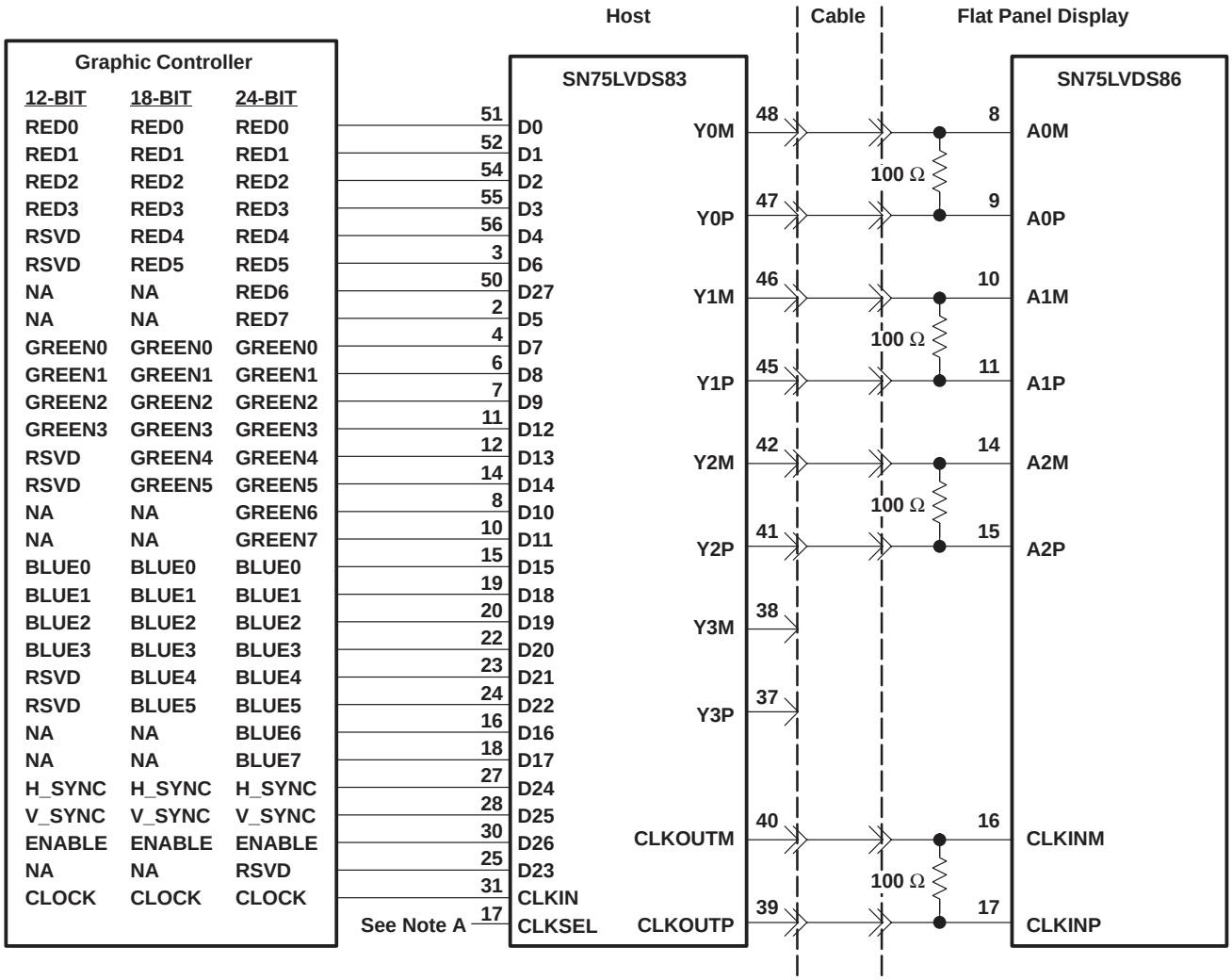
## APPLICATION INFORMATION




NOTES: A. Connect this terminal to $V_{CC}$ for triggering to the rising edge of the input clock and to GND for the falling edge.
B. The five 100-Ω terminating resistors are recommended to be 0603 types.

**Figure 12. 24-Bit Color Host To 24-Bit LCD Panel Display Application**

## APPLICATION INFORMATION




NOTES: A. Connect this terminal to $V_{CC}$ for triggering to the rising edge of the input clock and to GND for the falling edge.
B. The four 100-Ω terminating resistors are recommended to be 0603 types.

**Figure 13. 24-Bit Color Host To 18-Bit LCD Panel Display Application**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75LVDS83DGG | NRND | TSSOP | DGG | 56 | 35 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | SN75LVDS83 | |
| SN75LVDS83DGGG4 | NRND | TSSOP | DGG | 56 | 35 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | SN75LVDS83 | |
| SN75LVDS83DGGR | NRND | TSSOP | DGG | 56 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | SN75LVDS83 | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

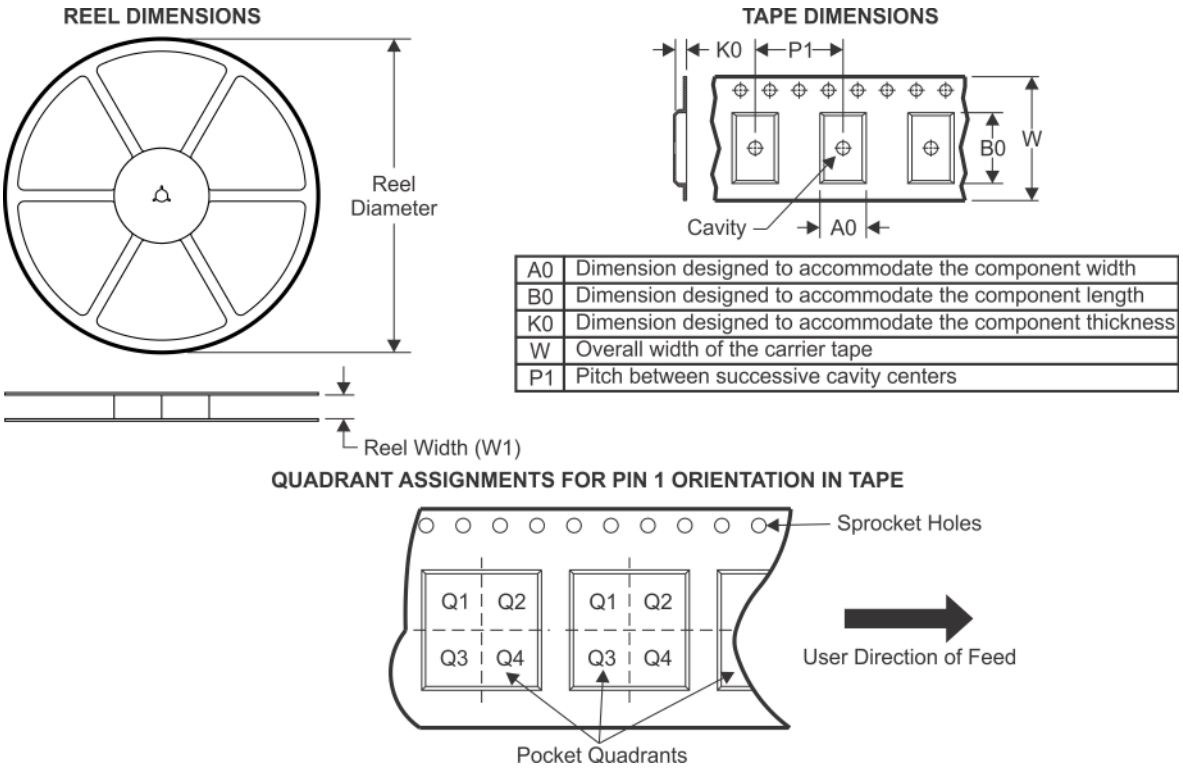
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

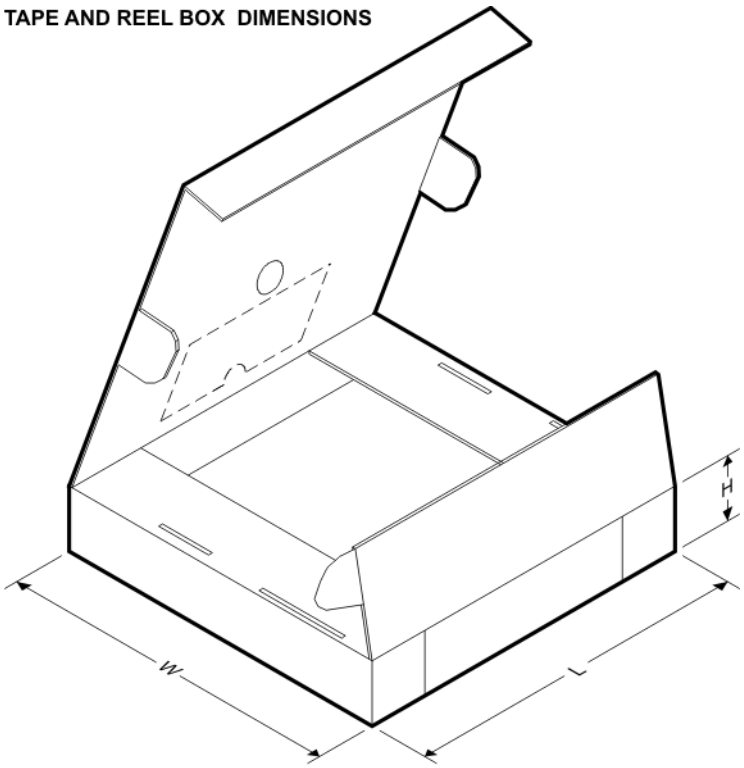



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75LVDS83DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

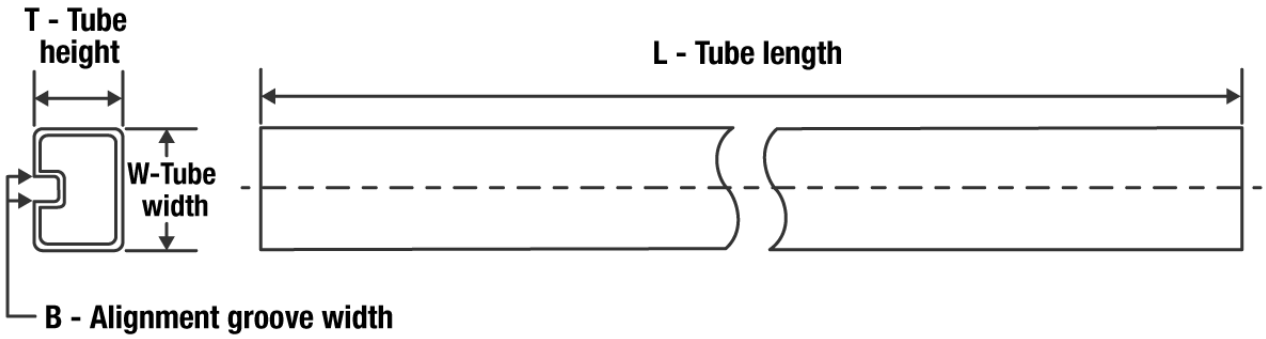
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75LVDS83DGGR | TSSOP | DGG | 56 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

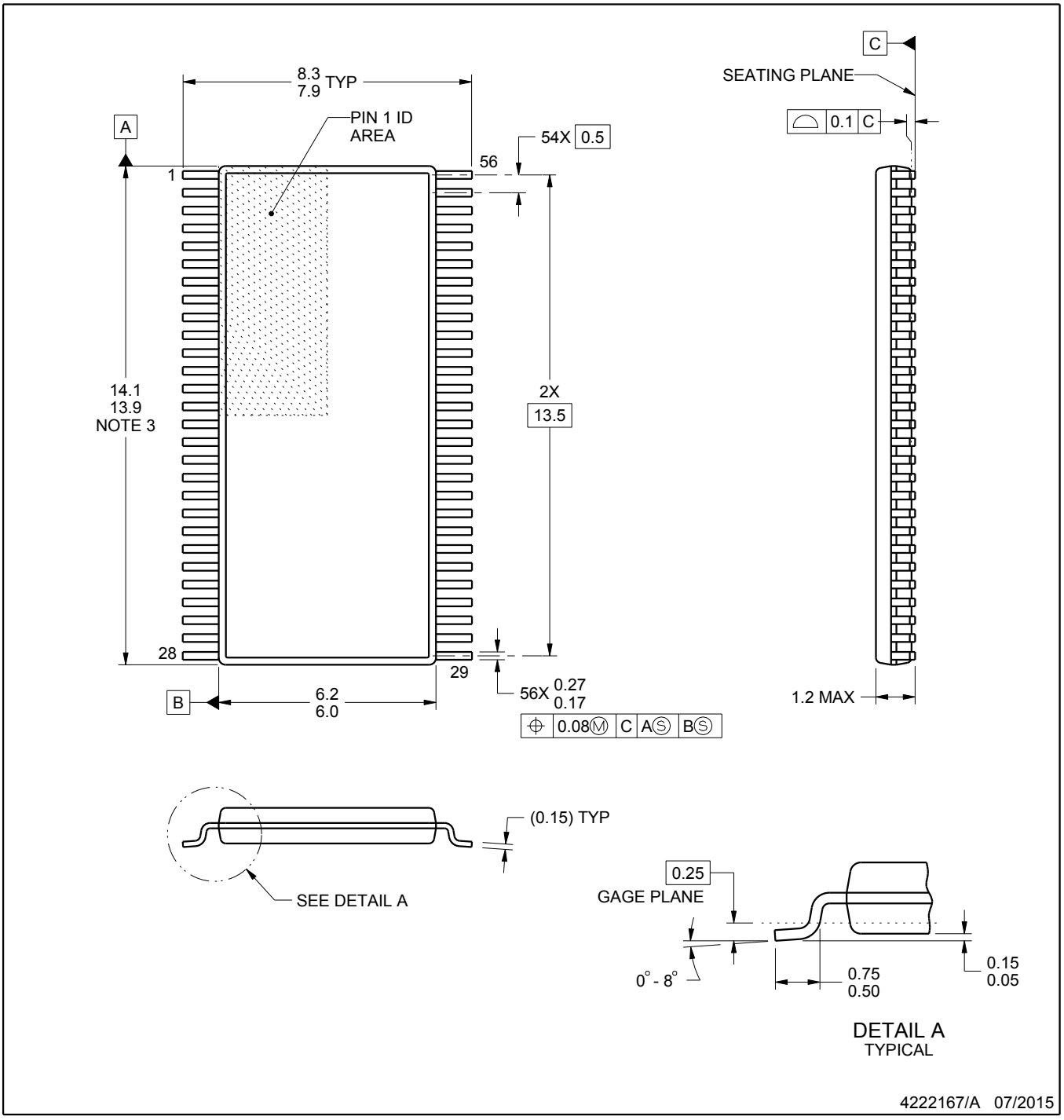
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN75LVDS83DGG | DGG | TSSOP | 56 | 35 | 530 | 11.89 | 3600 | 4.9 |
| SN75LVDS83DGGG4 | DGG | TSSOP | 56 | 35 | 530 | 11.89 | 3600 | 4.9 |

# PACKAGE OUTLINE

## DGG0056A

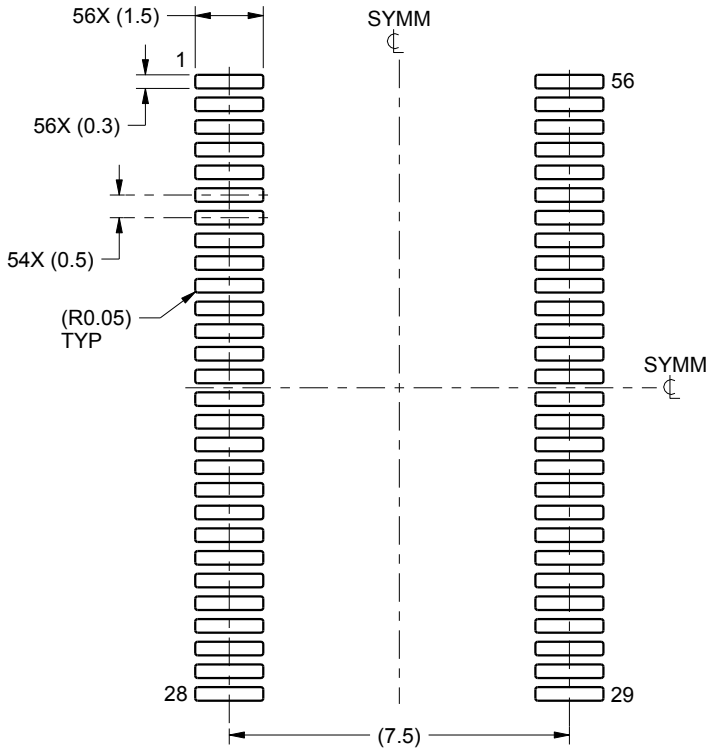
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

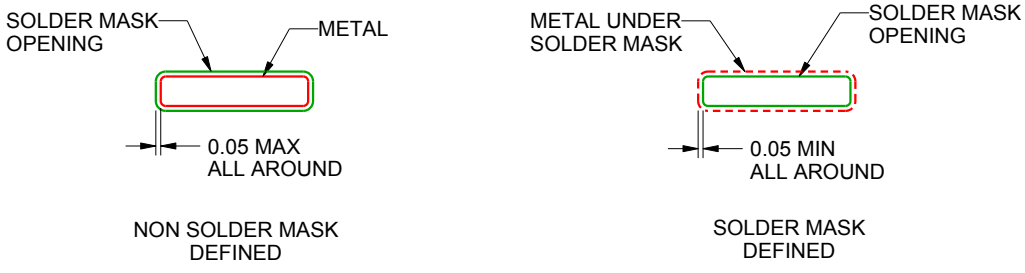



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

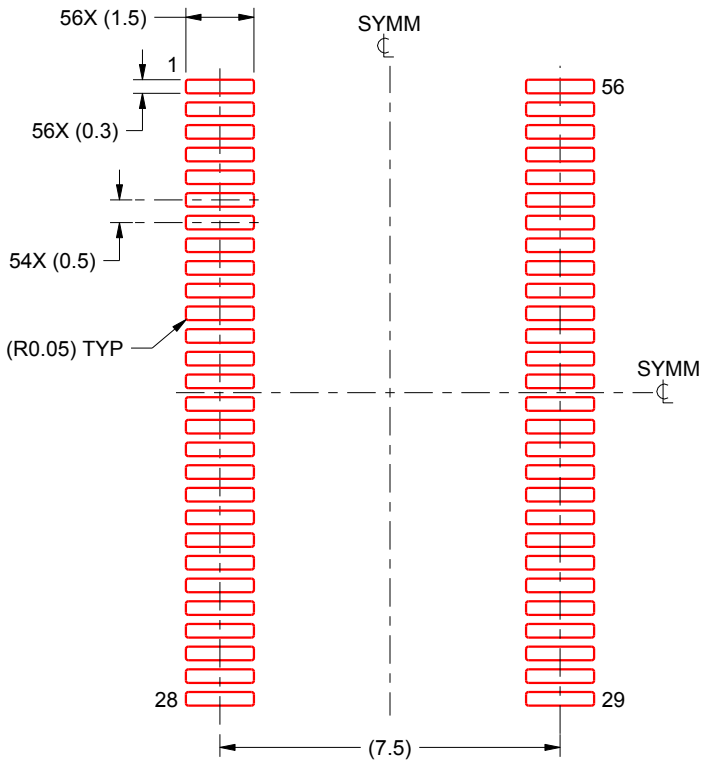



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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