LTC3312SA
3.3V to 1V 12A, 2MHz Dual-Phase Low Ripple Step-Down DC/DC Regulator

DESCRIPTION

Demo Circuit 3092A features the LTC®3312SA, 5V, dual 6A/dual-phase 12A step-down DC/DC regulator IC. This demo circuit is configured as a 2-phase, 2MHz, 3.3V input, single 1V output, 12A buck regulator. The top switches are 180-degree out of phase to reduce the output ripple.

The LTC3312SA features dual monolithic synchronous 6A step-down power stages in a 3mm × 4mm package for space saving applications with demanding performance requirements. Both bucks achieve high efficiency and fast transient response with low external component count. The LTC3312SA can also be configured as a dual output, 6A per output, step-down converter. Please refer to DC3091A as a dual output application example. The LTC3312SA data sheet gives a complete description of its operation and application information. The data sheet must be read in conjunction with this demo manual when evaluating or modifying this demo circuit.

DC3092A supports three operation modes, including pulse skip, forced continuous, and Burst Mode® operation. The clock frequency and the operation mode are shared by both buck phases. User can select desired operation mode with JP1 jumper. Setting JP1 to FC/SYNC position also allows the LTC3312SA to sync to a clock frequency from 1MHz to 3MHz, operating in forced continuous mode.

An EMI filter is included in this demo circuit for noise sensitive applications. To power with EMI filter, please apply input voltage via VIN EMI terminal.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}/V_{IN} EMI	DC3092A Input Voltage Range		2.25		5.5	V
V_{OUT}	DC3092A Output Voltage Range		0.98	1	1.02	V
I_{OUT}	DC3092A Output Current				12	A
f_{SW}	Switching Frequency		1.8		2.2	MHz
EFF	Efficiency	V_{IN} = 3.3V, I_{OUT} = 6A		91		%

BOARD PHOTO

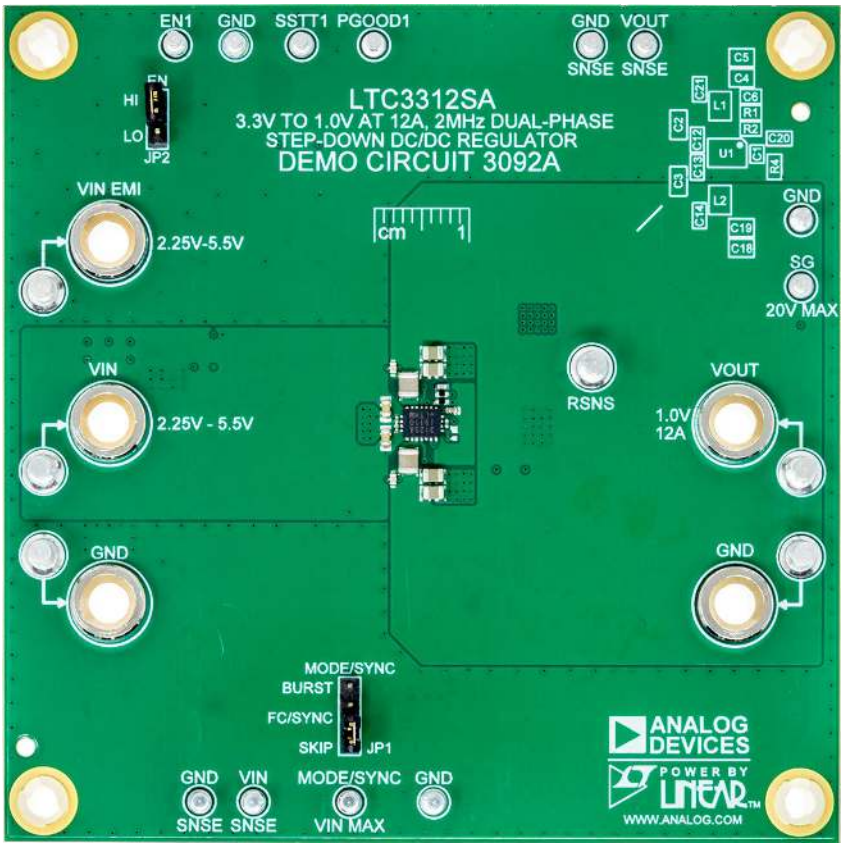


Figure 1. DC3092A Demo Board

QUICK START PROCEDURE

Refer to Figure 2 for the proper measurement equipment setup and follow the procedure below:

NOTE: For accurate V_{IN}, V_{OUT} and efficiency measurements, measure V_{IN} at the VIN SNSE and GND SNSN turrets, and measure V_{OUT} at the VOUT SNSE and GND SNSE turrets. When measuring the input or output ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. It is recommended to use technique shown in Figure 3a and Figure 3b for basic ripple measurement.

Prepare for The Test

A Select a power supply PS1 that can handle 5V of output voltage and 10A of output current, with internal current meter. If possible, connect PS1 Kelvin Sense terminals with VIN SNSE and GND SNSE turrets.

B Select an electronic load LD1 can handle 1.5V of load voltage and up to 12A of load current in constant current mode.

C Select an oscilloscope with two or more channels and two voltage probes.

QUICK START PROCEDURE

1. Connect PS1, LD1, VM1, VM2 and VM3 as shown in Figure 2. If the input EMI filter is desired, connect the input power supply to VIN EMI and GND.
2. Set the JP2 to HI position. Set LD1 to 0A. Slowly increase PS1 to 1.0V. If PS1 current reads less than 20mA, increase PS1 to 3.3V until VM1 reads 3.3V ±10mV. PS1 current should read between 1mA to 5mA. VM2 should read between 0.98V to 1.02V. VM3 should read above 3V.
3. Connect an oscilloscope voltage probe as shown in Figure 3a, between VOUT SNSE and GND SNSE turrets. Set channel to AC-coupled, voltage scale to 20mV, and time base to 10µs/div. Check VOUT ripple voltage. Output voltage ripple can also be measured with a low inductance connector on TP1, as shown in Figure 3b.
4. Increase the load by 1A intervals up to 12A and observe the voltage output regulation, ripple voltage, SW behavior and the voltage on the SSTT1 turret. Calculate Die temperature using the formula below:

$$T_J(°C) = \frac{V_{SSTT}}{4mV} - 273 \quad (1)$$

5. If other operation modes are desired. Turn off PS1, set LD1 to 0A and set JP1 to FC/SYNC or BURST position. Turn on PS1, slowly increase LD1 and observe the change in PS1 output current, SW behavior and output ripple.
6. Optional: To change the frequency, remove R9. Install the desired RT resistor in the R4 location. Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output. Refer to the LTC3312SA data sheet and LTPowerCAD for more information on choosing the required components.
7. Optional: To SYNC to a specific frequency, set JP1 to FC/SYNC position. Connect a waveform generator to MODE/SYNC turret. Please refer to LTC3312SA data sheet for synchronization signal requirements.
8. To test the transient response with a base load, add the desired resistor to produce a minimum load between VOUT and RSNS1 turrets (RL shown on Figure 2). Note that the total load resistance will be RL plus R11 (20mΩ). Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.
9. Measure the RSNS1 voltage to observe the current, V_{RSNS1}/20mΩ. Adjust the amplitude of the pulse to provide the desired transient. Connect signal generator SG1 between SG_INPUT and GND turrets. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Refer to the following equations for output current measurement:

$$I_{OUT} = \frac{V_{RSNS1}}{20m\Omega} \quad (2)$$

10. When done, turn off SG1, PS1 and Load.

TEST SETUP

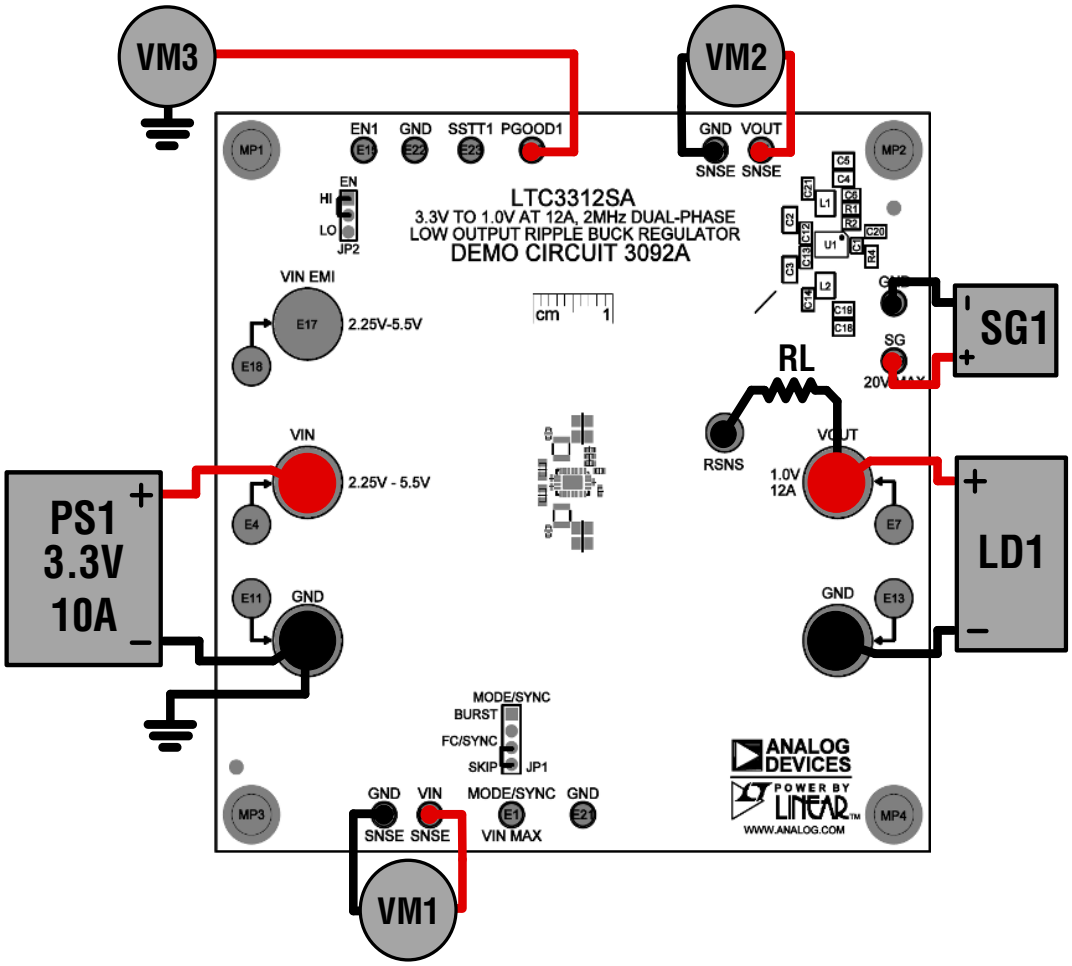


Figure 2. Test Setup for DC3092A Demo Board

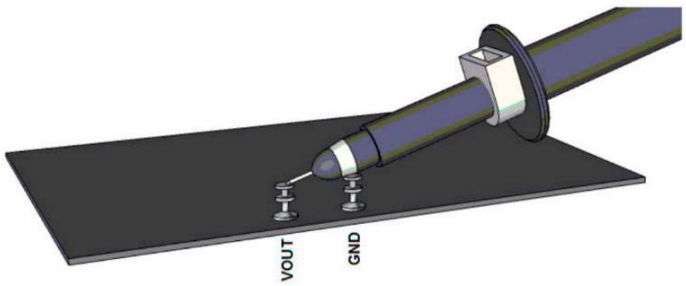


Figure 3a. Technique for Measuring Output Ripple and Step Response with a Scope Probe

Figure 3b. Technique for Measuring Output Ripple and Step Response with a Low Inductance Connector (Not Supplied)

TYPICAL PERFORMANCE CHARACTERISTICS

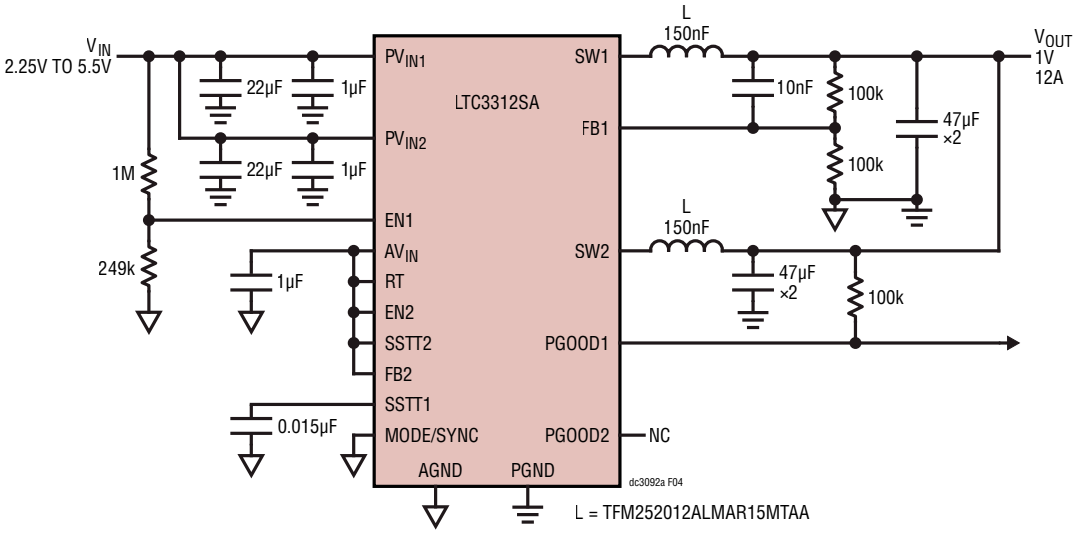


Figure 4. LTC3312SA 2-Phase 2MHz 12A Buck Typical Application Schematic

Dual Phase Efficiency vs Load, 3.3V to 1V, f_{SW} = 2MHz

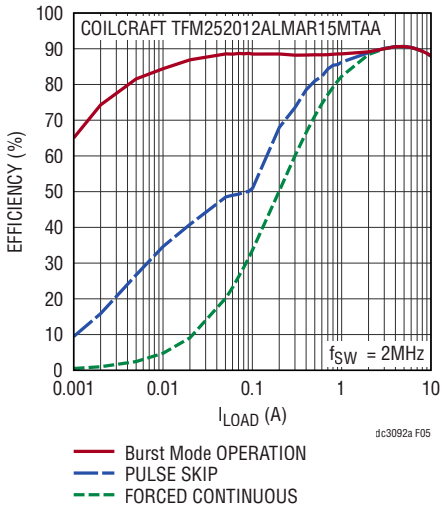
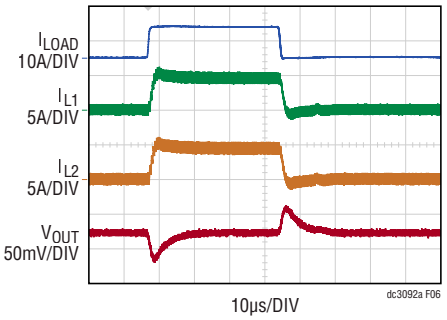


Figure 5. Efficiency vs Load

Dual Phase Configuration Load Transient Response, Forced Continuous Mode

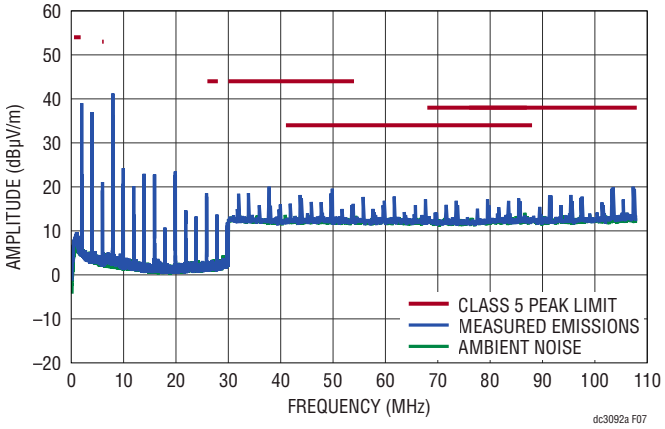


3.3V_{IN} TO 1.0V_{OUT}, 2MHz 2-PHASE APPLICATION
C_{OUT} = 47µF ×6, L = 150nH
LOAD STEP: 0.1A TO 9A IN 1µs

Figure 6. Load Step Response

EMI TEST RESULTS

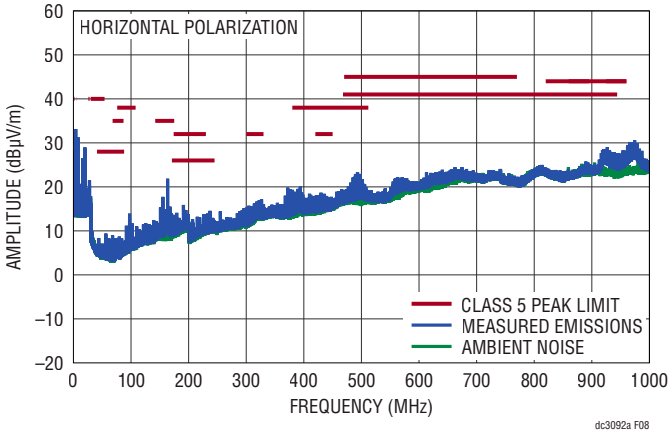
CISPR25 Conducted Emission Test with Class 5 Peak Limits (Voltage Method) (Supply)



DC3092A DEMO BOARD
(WITH VOLTAGE APPLIED TO V_{IN} EMI INPUT)
3.3V INPUT TO 1V OUTPUT AT 9.6A, f_{SW} = 2MHz

Figure 7. CISPR25 Conducted Emission Test with Class 5 Peak Limits (Voltage Method)

Radiated EMI Performance (CISPR25 Radiated Emissions Test with Class 5 Peak Limits)



DC3092A DEMO BOARD
(WITH EMI FILTER)
3.3V INPUT TO 1V OUTPUT AT 9.6A, f_{SW} = 2MHz

Figure 8. CISPR25 Radiated Emission Test with Class 5 Peak Limits

THEORY OF OPERATION

Introduction to the DC3092A

The DC3092A demonstration circuit features the LTC3312SA, 5V, Dual 6A/Dual-Phase 12A Step-Down DC/DC Regulator. The LTC3312SA contains two monolithic, constant frequency, current mode step-down DC/DC converters. An oscillator, shared by two converters, with frequency set by a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. The beginning of each clock cycle of the two converters are 180-degree out of phase. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current, at which the top switch turns off, is controlled by the voltage on the internal VC node, which is the output of the error amplifier. When operating in dual-phase mode, VC of Buck1 is used to control the peak current for both buck power stages. The internal VC node is connected with internal compensator to stabilize the control loop. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous bottom power switch turns on until the next clock cycle begins. In pulse skip mode and Burst Mode, the bottom switch also turns off when inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level. In Burst Mode, the error amplifier and most part of the internal circuitry is turned off until output voltage trips an output low comparator, during extreme light load condition, to improve light load efficiency.

If the EN1 pin is low, the DC3092A is in shutdown and in a low quiescent current state. When the EN1 pin is above its threshold, the DC3092A will be enabled.

The MODE/SYNC pin synchronizes the switching frequency to an external clock. It also sets the PWM mode. The PWM modes of operation are Burst, Pulse Skip and Forced Continuous. See the LTC3312SA data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of V_{OUT} to V_{IN} and the available inductor values. The maximum allowable operating frequency may be calculated in the formula below.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet t_{ON(MIN)}} \quad (3)$$

Select an operating switching frequency below $f_{SW(MAX)}$. Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3312SA single stage operating load, 6A. Use the formulas below to calculate the inductor value to obtain a 30% (1.8A) inductor ripple for the operating frequency.

$$L \geq \frac{V_{OUT}}{1.8A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5 \quad (4)$$

$$L \geq \frac{0.25 \bullet V_{IN(MAX)}}{1.8A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (5)$$

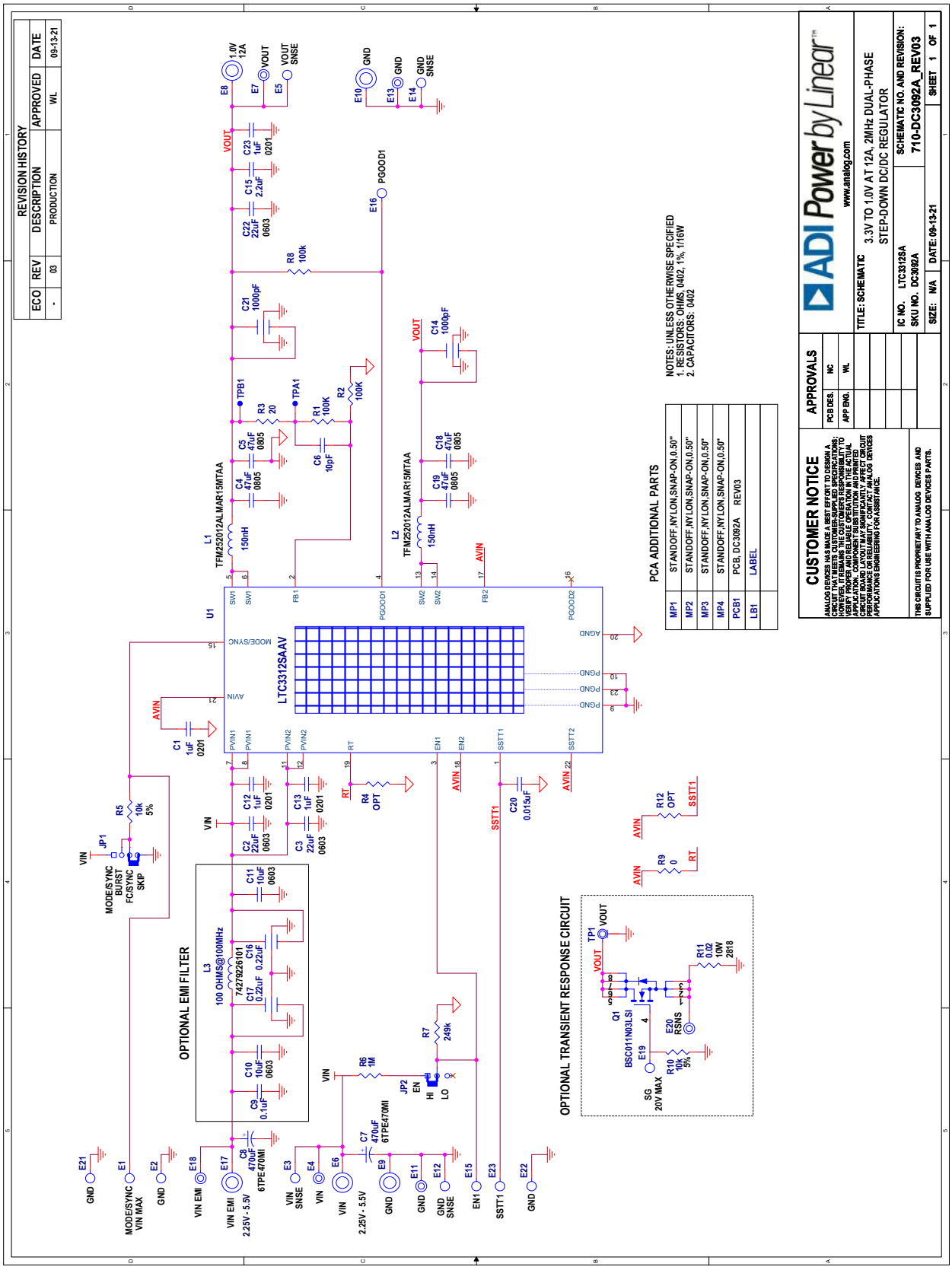
The overall control loop of the converter can be tuned by output capacitors and feedforward capacitors. The LTC3312SA has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces required output capacitance to meet the desired transient voltage range. C6 along with R1 provides a phase lead which will improve the phase margin.

Loop stability is generally measured using the Bode Plot method of plotting loop gain in dB and phase shift in degrees. The 0dB crossover frequency should be less the 1/6 of the operating frequency to reduce the effects of added phase shift of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	C1, C12, C13	CAP., 1µF, X7T, 6.3V, 20%, 0201	MURATA, GRM033D70J105ME01D
2	2	C2, C3	CAP., 22µF, X5R, 10V, 20%, 0603	MURATA, GRM188R61A226ME15D
3	4	C4, C5, C18, C19	CAP., 47µF, X6S, 6.3V, 20%, 0805	TAIYO YUDEN, JMK212BC6476MG-T
4	1	C6	CAP., 10pF, C0G/NP0, 50V, ±0.5pF, 0402	TDK, C1005C0G1H100D050BA
5	1	C20	CAP., 0.015µF, X7R, 16V, 10%, 0402	AVX, 0402YC153KAT2A
6	2	L1, L2	IND., 150nH, , 20%, 7.3A, 11mΩ	TDK, TFM252012ALMAR15MTAA
7	2	R1, R2	RES., 100k, 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F1003TRF
8	1	U1	IC, 5V, DUAL 6A/DUAL PHASE 12A STEP-DOWN DC/DC REGULATOR, LQFN	ANALOG DEVICES, LTC3312SAav#PBF
Additional Demo Board Circuit Components				
1	2	C7, C8	CAP., 470µF, TANT, POSCAP, 6.3V, 20%, 7343, 18mΩ	PANASONIC, 6TPE470MI
2	1	C9	CAP., 0.1µF, X7R, 25V, 10%, 0402	MURATA, GCM155R71E104KE02D
3	2	C10, C11	CAP., 10µF, X7S, 6.3V, 20%, 0603	TDK, C1608X7S0J106M080AC
4	2	C14, C21	CAP., 1000pF, X7R, 50V, 20%, 0402, 3-TERM, X2Y EMI FILTER	JOHANSON DIELECTRICS, 500X07W102MV4T
5	1	C15	CAP., 1µF, X7R, 6.3V, 10%, 0402	MURATA, GRM155R70J105KA12D
6	2	C16, C17	CAP., 0.22µF, X7R, 6.3V, 20%, 0603	JOHANSON DIELECTRICS, 6R3X14W224MV4T
7	1	L3	IND., 100Ω AT 100MHz, FERRITE BEAD, 25%, 8A, 6mΩ, 1812	WURTH ELEKTRONIK, 74279226101
8	1	Q1	XSTR., MOSFET, N-CH, 40V, 15.9A, PPAK SO-8	VISHAY, SIR426DP-T1-GE3
9	1	R3	RES., 20Ω, 1%, 1/16W, 0402	NIC, NRC04F20R0TRF
10	2	R5, R10	RES., 10k, 5%, 1/16W, 0402	NIC, NRC04J103TRF
11	1	R6	RES., 1M, 1%, 1/16W, 0402	NIC, NRC04F1004TRF
12	1	R7	RES., 249k, 1%, 1/16W, 0402	NIC, NRC04F2493TRF
13	1	R8	RES., 100k, 5%, 1/16W, 0402	YAGEO, RC0402JR-07100KL
14	1	R9	RES., 0Ω, 1/16W, 0402	NIC, NRC04Z0TRF
15	1	R11	RES., 0.02Ω, 1%, 10W, 2818, SENSE	VISHAY, WSHP2818R0200FEA
16	1	TP1	CONN., U.FL, RECEPT, ST SMD, 0Hz to 6GHz 50Ω	HIROSE ELECTRIC, U.FL-R-SMT-1(10)
17	1	TP1_PLUG	CONN U.FL PLUG STR 50Ω SMD	HIROSE ELECTRIC, U.FL-PR-SMT2.5-1(10)
Hardware: For Demo Board Only				
1	12	E1-E3, E5, E12, E14, E15, E16, E19, E21, E22, E32	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E11, E13, E18, E20	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E6, E8-E10, E17	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1×4, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000411121
5	1	JP2	CONN., HDR, MALE, 1×3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	WURTH ELEKTRONIK, 702935000
6	2	XJP1, XJP2	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM



Rev. 0

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.