MP6551

14V, 5A, H-Bridge Motor Driver

DESCRIPTION

The MP6551 is an H-bridge motor driver. Its 2.5V to 14V input voltage (V_{IN}) range allows the device to operate from a variety of battery power sources, including single-cell lithium-ion batteries, dual-cell lithium-ion batteries, and 3-cell to 6-cell alkaline batteries. Its low on resistance enables it to achieve up to 5A of output current (I_{OUT}) across its entire V_{IN} range.

The MP6551 can drive a brushed DC motor in bidirectional applications or two DC motors in unidirectional, speed-controlled applications.

Full protection features include over-current protection (OCP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The MP6551 is available in a QFN-14 (2.5mmx3mm) package.

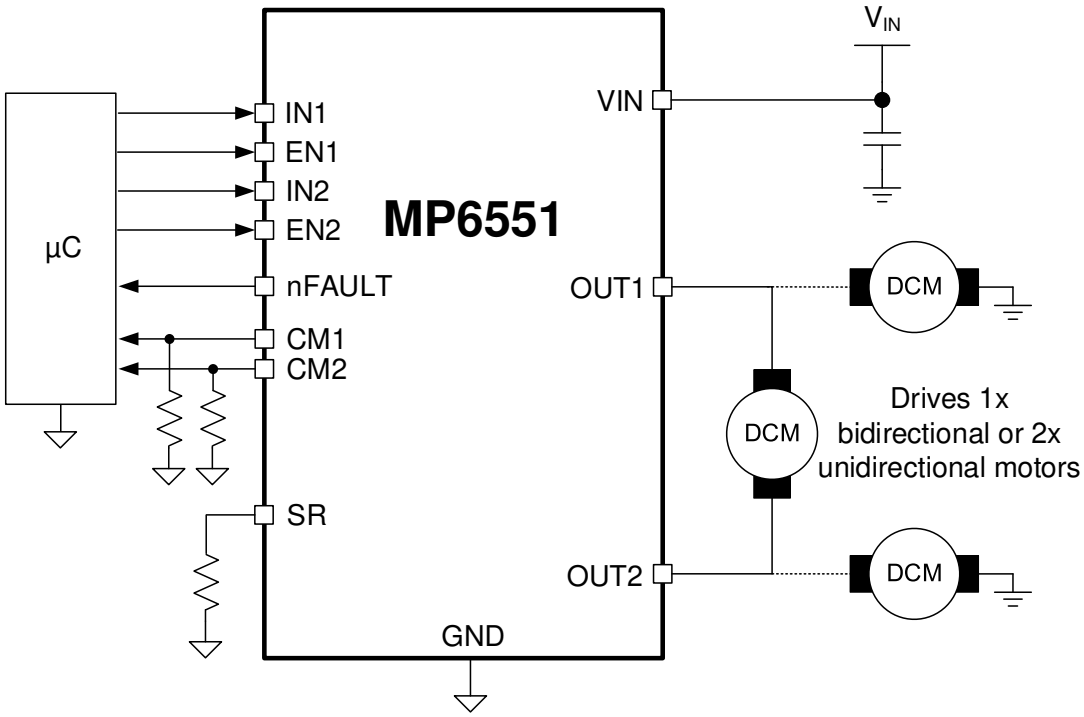
FEATURES

- 2.5V to 14V Operating Input Range
- Up to 5A Output Current (I_{OUT})
- Full H-Bridge or Dual Half H-Bridge Driver
- 15mΩ Low On Resistance per MOSFET
- Current Measurement
- Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO) Protection
- Thermal Shutdown
- Sleep Mode during Low-Power
- Fault Indication Output
- Available in a QFN-14 (2.5mmx3mm) Package

APPLICATIONS

- Mini Drones
- Battery-Powered Toys

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6551GQB	QFN-14 (2.5mmx3mm)	*See Below*	1

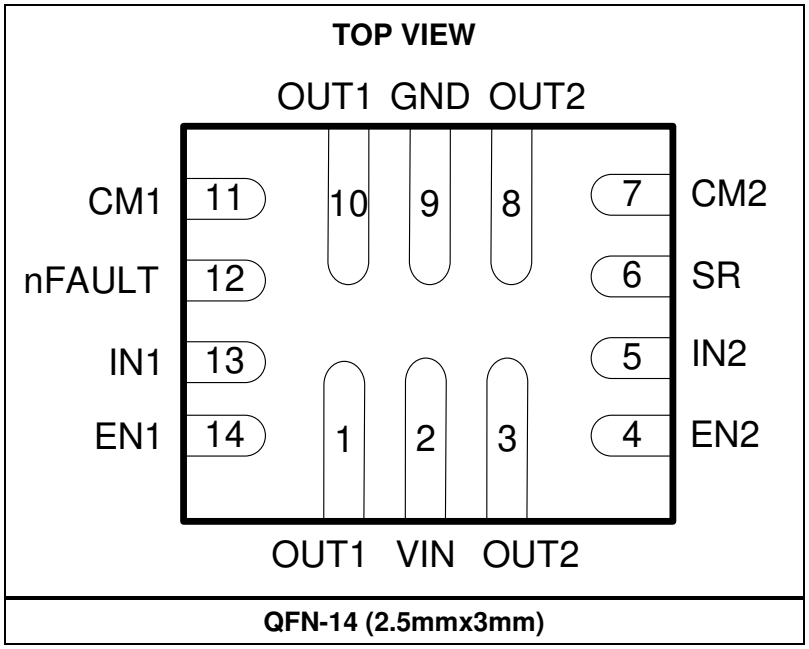
* For Tape & Reel, add suffix -Z (e.g. MP6551GQB-Z).

TOP MARKING

BCR
YWW
LLL

BCR: Product code of MP6551GQB
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2.5mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 10	OUT1 (1)	**Output terminal 1.**
2	VIN (1)	**Input supply voltage.** Decouple the VIN pin to GND using a ≥100nF ceramic capacitor. Additional bulk capacitance may be required.
3, 8	OUT2 (1)	**Output terminal 2.**
4	EN2	**OUT2 enable input.** Pull the EN2 pin high to enable OUT2; pull EN2 low to force OUT2 into a high-impedance (Hi-Z) state. EN2 is pulled down internally.
5	IN2	**OUT2 control input.** Pull the IN2 pin high to make OUT2 go high; pull IN2 low to make OUT2 go low. IN2 is pulled down internally.
6	SR	**Slew rate control.** Connect a resistor from SR to GND.
7	CM2	**OUT2 current measurement output.**
9	GND (1)	**System ground.**
11	CM1	**OUT1 current measurement output.**
12	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. If an over-current (OC) or over-temperature (OT) fault occurs, nFAULT is pulled low.
13	IN1	**OUT1 control input.** Pull the IN1 pin high make OUT1 go high; pull IN1 low to make OUT1 go low. IN1 is pulled down internally.
14	EN1	**OUT1 enable input.** Pull EN1 high to enable OUT1; pull EN1 low force OUT1 into a high-impedance (Hi-Z) state. EN1 is pulled down internally.

Note:

1) These pins should have as much PCB copper attached to them as possible. The copper removes the dissipated heat in the device.

ABSOLUTE MAXIMUM RATINGS (2)

Supply voltage (V_{IN}) ..... -0.3V to +16V
OUTx voltage (V_{OUTX}) ..... -0.7V to +16V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (3)…..
……...1.92W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 2.5V to 14V
Peak output current (I_{OUT}) .....±5A
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-14 (2.5mmx3mm)	65	13	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 4V, T_A = 25°C, unless otherwise noted.

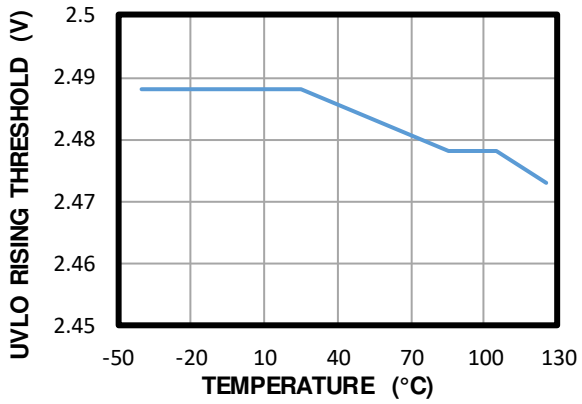
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		2.5		14	V
Quiescent current	I_Q	No load current		2.5	4	mA
	I_{SLEEP}	Sleep mode		10.5	14.5	µA
Internal MOSFETs						
High-side MOSFET (HS-FET) output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_J = 25°C		15	19	mΩ
Low-side MOSFET (LS-FET) output on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_J = 25°C		12	16	mΩ
Body diode forward voltage	V_F	I_{OUT} = 2A		0.8		V
Control Logic						
Input logic low threshold	V_{IN_LOW}				0.8	V
Input logic high threshold	V_{IN_HIGH}		1.5			V
Logic input current	I_{IN_HIGH}	V_{IH} = 5V	-20		+20	µA
	I_{IN_LOW}	V_{IL} = 0.8V	-20		+20	µA
Internal pull-down resistance	R_{PD}			500		kΩ
nFault Output (Open-Drain Output)						
Low output voltage	V_{OUT_LOW}	I_{OUT} = 5mA			0.5	V
High output leakage current	I_{OUT_HIGH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}			2.5	2.7	V
UVLO hysteresis	V_{UVLO_HYS}			500		mV
Peak current limit	I_{OCP1}	Sink	10	14		A
	I_{OCP2}	Source	8.5	11.5		A
Thermal shutdown (6)	T_{SD}			150		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			15		°C
Current Sense (CS)						
CS ratio				1 / 10,000		A/A
CS output current		LS-FET current = 1A		120		µA
		LS-FET current = -1A		-91		µA
CS output voltage swing				3.57		V
Sleep mode entry time	t_{SLEEP}	From EN1 = EN2 = 0		1		ms
Sleep mode exit time	t_{WAKE}	From EN1 = 1 or EN2 = 1		36		µs
Pulse-width modulation (PWM) frequency	f_{PWM}	R_{SR} = 0Ω		500		kHz
Output rise time (6)	t_{RISING}	R_{SR} = 3MΩ, 10Ω load to GND		3		µs
Output fall time (6)	$t_{FALLING}$					
Propagation delay (6)	t_{PD_RISING}	IN1/IN2 rising to OUT1/OUT2 rising		500		ns
	$t_{PD\_FALLING}$	IN1/IN2 falling to OUT1/OUT2 falling		400		ns
Output enable time (6)	t_{OUT_EN}	EN1/EN2 to OUT1/OUT2, active		95		ns
Output disable time (6)	t_{OUT_DIS}	EN1/EN2 to OUT1/OUT2, Hi-Z		170		ns

Note:

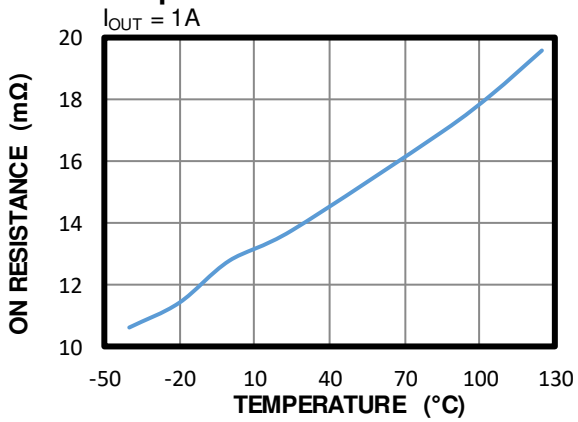
6) Not tested in production.

TYPICAL CHARACTERISTICS

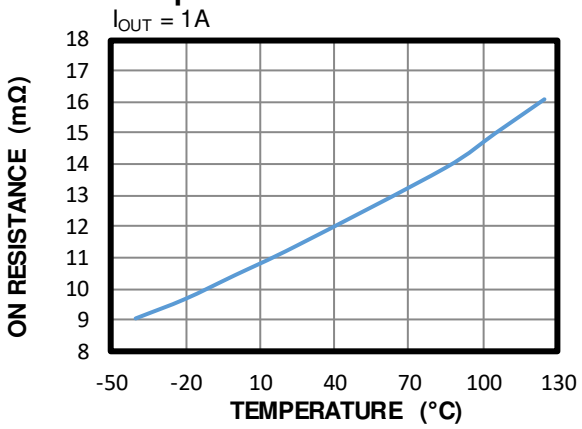
UVLO Rising Threshold vs. Temperature



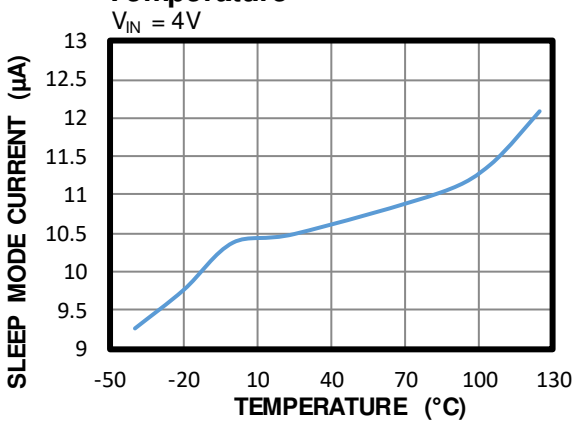
HS-FET On Resistance vs. Temperature



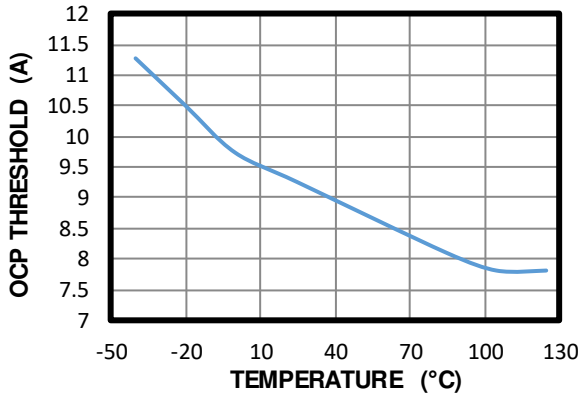
LS-FET On Resistance vs. Temperature



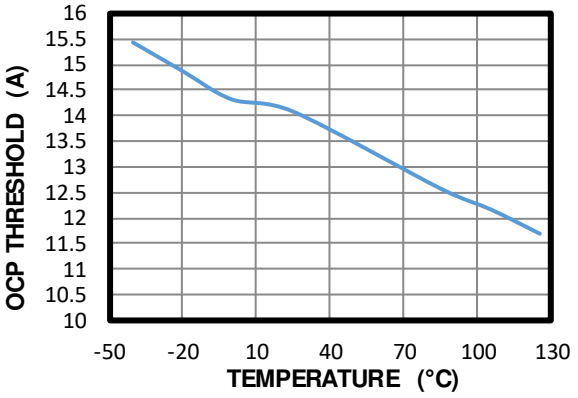
Sleep Mode Current vs. Temperature



HS-FET OCP Threshold vs. Temperature



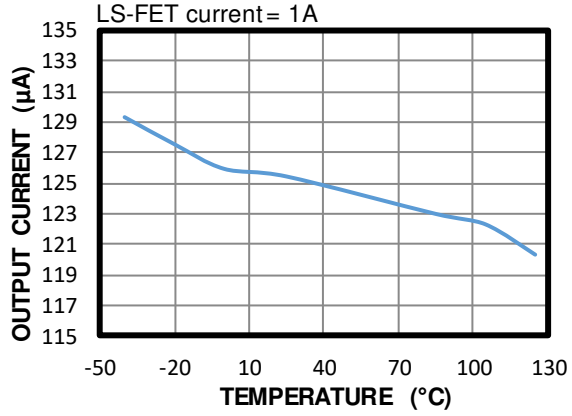
LS-FET OCP Threshold vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

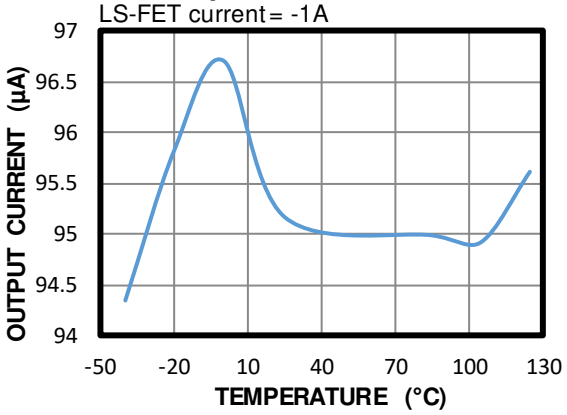
Current Sense Output Current vs. Temperature

LS-FET current = 1A



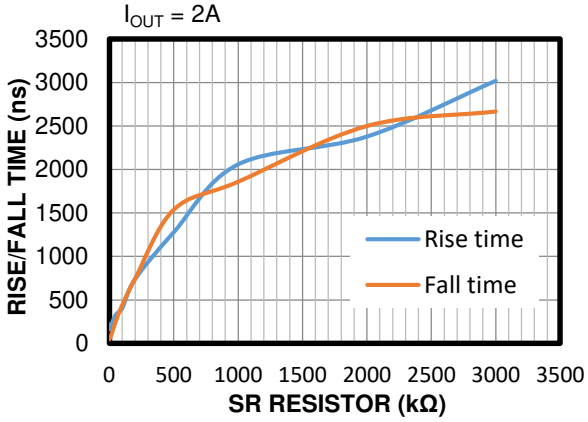
Current Sense Output Current vs. Temperature

LS-FET current = -1A



Rise/Fall Time vs. SR Resistor

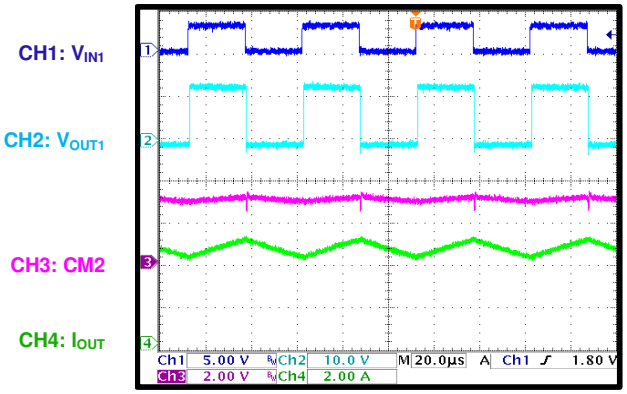
I_{OUT} = 2A



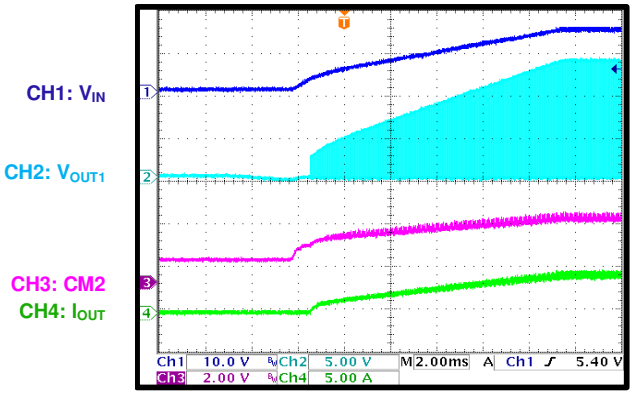
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 14V, I_{OUT} = 2A, OUT1 f_{SW} = 20kHz, OUT2 LS-FET on, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load = 1.4Ω + 0.19mH between OUT1 and OUT2.

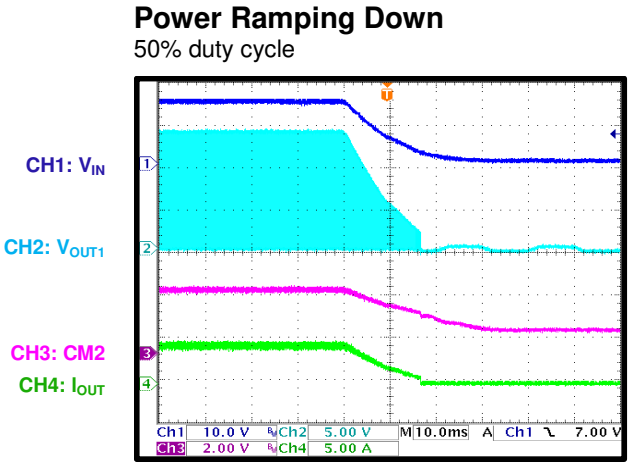
Steady State
50% duty cycle



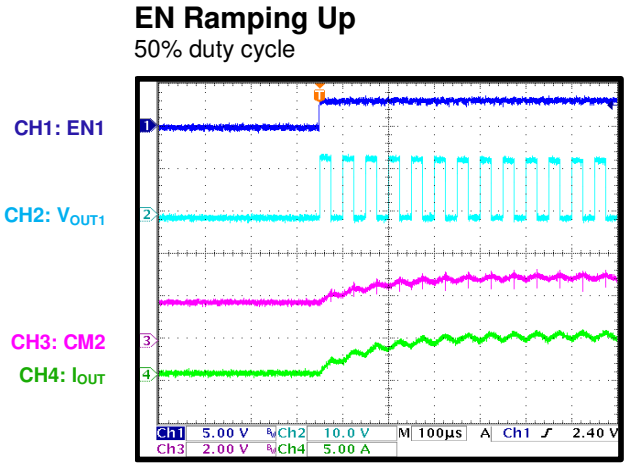
Power Ramping Up
50% duty cycle



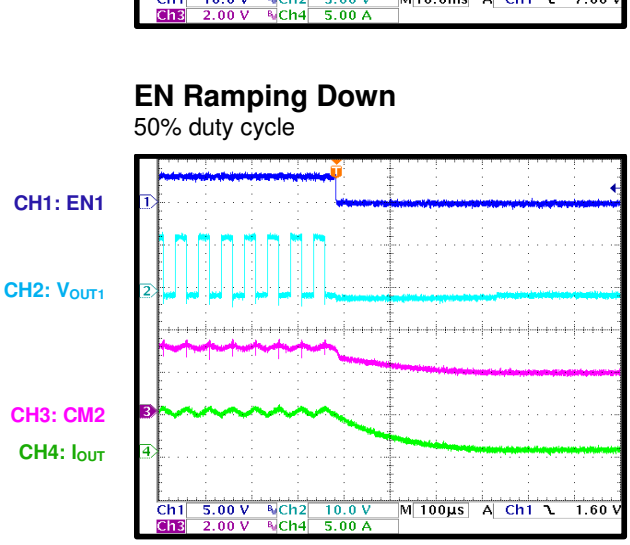
Power Ramping Down
50% duty cycle



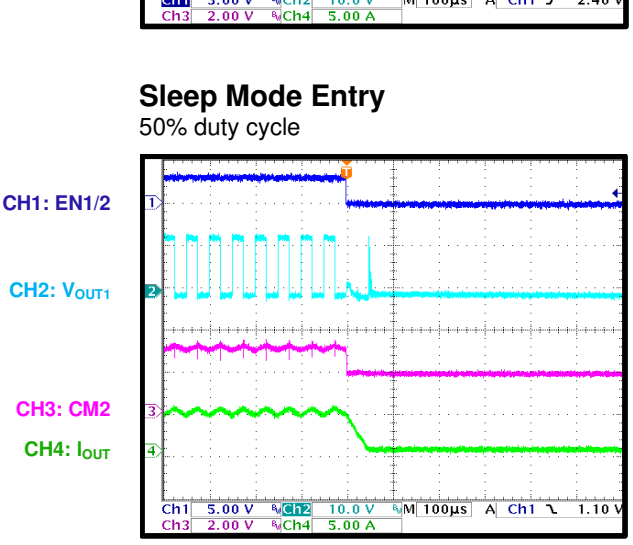
EN Ramping Up
50% duty cycle



EN Ramping Down
50% duty cycle



Sleep Mode Entry
50% duty cycle

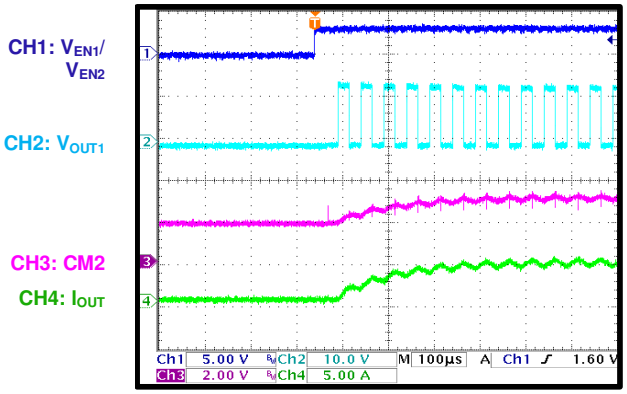


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 14V, I_{OUT} = 2A, OUT1 f_{SW} = 20kHz, OUT2 LS-FET on, V_{REF} = 3.3V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load = 1.4Ω + 0.19mH between OUT1 and OUT2.

Sleep Mode Recovery

50% duty cycle



FUNCTIONAL BLOCK DIAGRAM

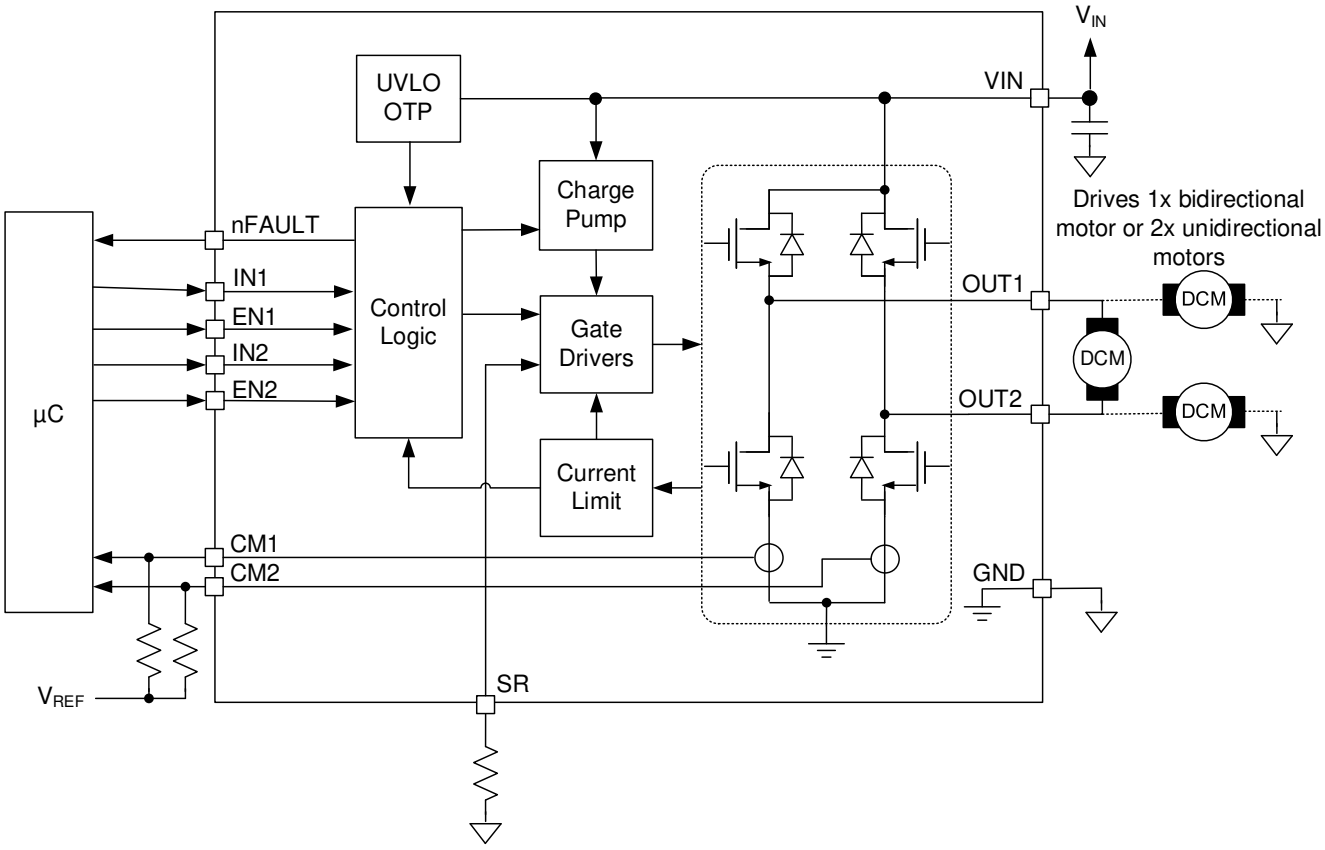


Figure 1: Functional Block Diagram

OPERATION

The MP6551 is an H-bridge motor driver that integrates four N-channel power MOSFETs. It can achieve 5A of peak output current (I_{OUT}) across a 2.5V to 14V input voltage (V_{IN}) range, and is designed to drive brushed DC motors, solenoids, and other loads.

Input Logic

Each of the MP6551's half H-bridges is controlled independently via the IN1, IN2, EN1, and EN2 input pins. Table 1 shows the control logic for each input pin.

Table 1: Input Pin Control Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

Sleep Mode

Pull the EN1 and EN2 pins low to enable sleep mode. In sleep mode, all internal circuitry (including the gate driver charge pump) is disabled, and the outputs are turned off. If either EN1 or EN2 is enabled again, then the device resumes normal operation. There is a short delay time (t_{WAKE}) before the output(s) are enabled again.

Slew Rate (SR) Control

The MP6551 has a slew rate (SR) control pin. Use a resistor to connect the SR pin to GND to adjust the slew rate (output rise/fall time). This feature can reduce electromagnetic interference (EMI) caused by output transitions.

The rise/fall time is proportional to the resistance used. Short SR to GND to generate a fast rise/fall time (about 100ns). A 3MΩ resistor generates a rise/fall time of about 3µs.

Fault Indication

The MP6551's fault indication (nFAULT) pin is an open-drain output that requires an external pull-up resistor. The nFAULT pin indicates if a fault has occurred. If an over-current (OC) or over-temperature (OT) fault occurs, nFAULT is pulled low. Once the fault condition is removed, nFAULT is pulled high via the pull-up resistor.

Current Measurement Outputs

The internal current-sensing circuitry senses the current flowing into each output. The CM1 and CM2 pins source or sink a current proportional to the current flowing into each of the half H-bridges' low-side MOSFETs (LS-FETs). The current flowing through the LS-FET is sensed in both the forward and reverse directions.

To convert this current into a voltage (e.g. to input to an analog-to-digital converter [ADC]), a termination resistor (R_{REF}) is required to create a reference voltage (V_{REF}). If no current is flowing, then the resultant output is equal to V_{REF}. If the current is flowing, then the voltage is above or below V_{REF}. (V_{OUT_SENSE}) can be calculated with Equation (1):

$$V_{OUT\_SENSE} = V_{REF} + (R_{REF} \times I_{LOAD}) / 10{,}000 \quad (1)$$

To terminate the outputs while using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and GND. The resulting ADC code is half-scale at zero current.

Figure 2 shows the current measurement circuit.

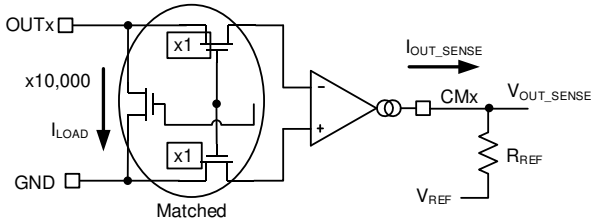


Figure 2: Current Measurement Circuit

If only the total current needs to be measured (e.g. the current of a full H-bridge driver), then the CM1 and CM2 pins can be connected to measure the sum of the two half H-bridge currents.

Over-Current Protection (OCP)

Over-current protection (OCP) protects the device from damage due to excessive current at the outputs. If the current through a MOSFET exceeds the current limit threshold, then the foldback current limit function limits I_{OUT} to a safe level and nFAULT goes low.

Over-current (OC) conditions are sensed on both the high-side MOSFET (HS-FET) and LS-FET, protecting the device from damage during a short to GND, short to supply, or a short across the motor winding.

Note that a sustained short circuit or OC fault can result in excessive die temperature, which may cause the device to go into thermal shutdown.

Under-Voltage Lockout (UVLO) Protection

If the V_{IN} drops below the under-voltage lockout (UVLO) threshold, all circuitry is disabled and the device's internal logic is reset. Once V_{IN} rises above the UVLO threshold again, the MP6551 resumes normal operation.

Thermal Shutdown

If the die temperature exceeds about 150°C, all MOSFETs are disabled and nFAULT goes low. Once the die temperature drops below about 135°C, the MP6551 resumes normal operation.

APPLICATION INFORMATION

External Component Selection

Bypass the VIN pin to GND using a 100nF ceramic X7R capacitor located as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor nearby the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize V_{IN}. The CM1 and CM2 pins are current measurement outputs. CM1 and CM2 are typically converted to a voltage via a termination resistor (R_{REF}) that creates a reference voltage (V_{REF}). A resistor divider connected between the ADC supply and GND can provide a ratiometric voltage for an AC/DC converter.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Bypass VIN to GND using a 100nF ceramic X7R capacitor located as close to the IC as possible.
2. Place an additional 1µF to 10µF ceramic capacitor nearby the 100nF capacitor. An electrolytic bulk capacitor may be required to stabilize V_{IN}.
3. The VIN, OUT1, and OUT2 pins dissipate heat from the motor driver. To reduce heat on the device, add as many copper planes to these pins as possible.
4. Solid planes on the inner layers of the device can also dissipate heat. Place multiple thermal vias on the VIN, OUTx, and GND copper planes to dissipate heat from the outer layers to the copper plane(s).

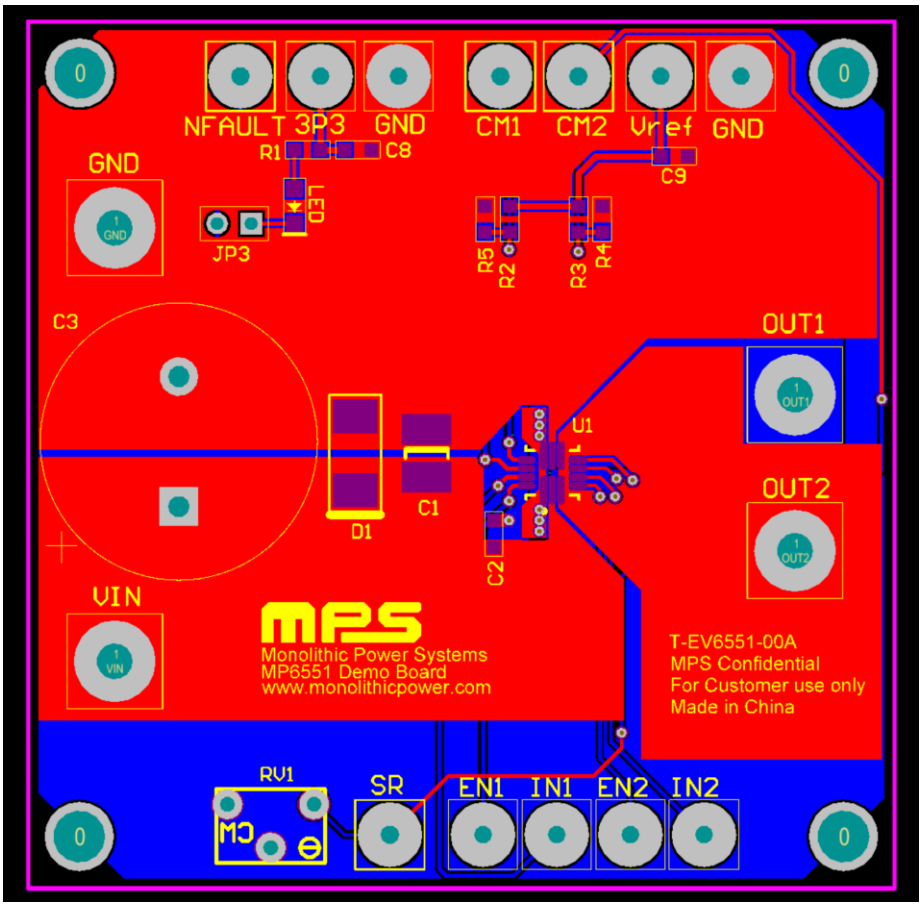


Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

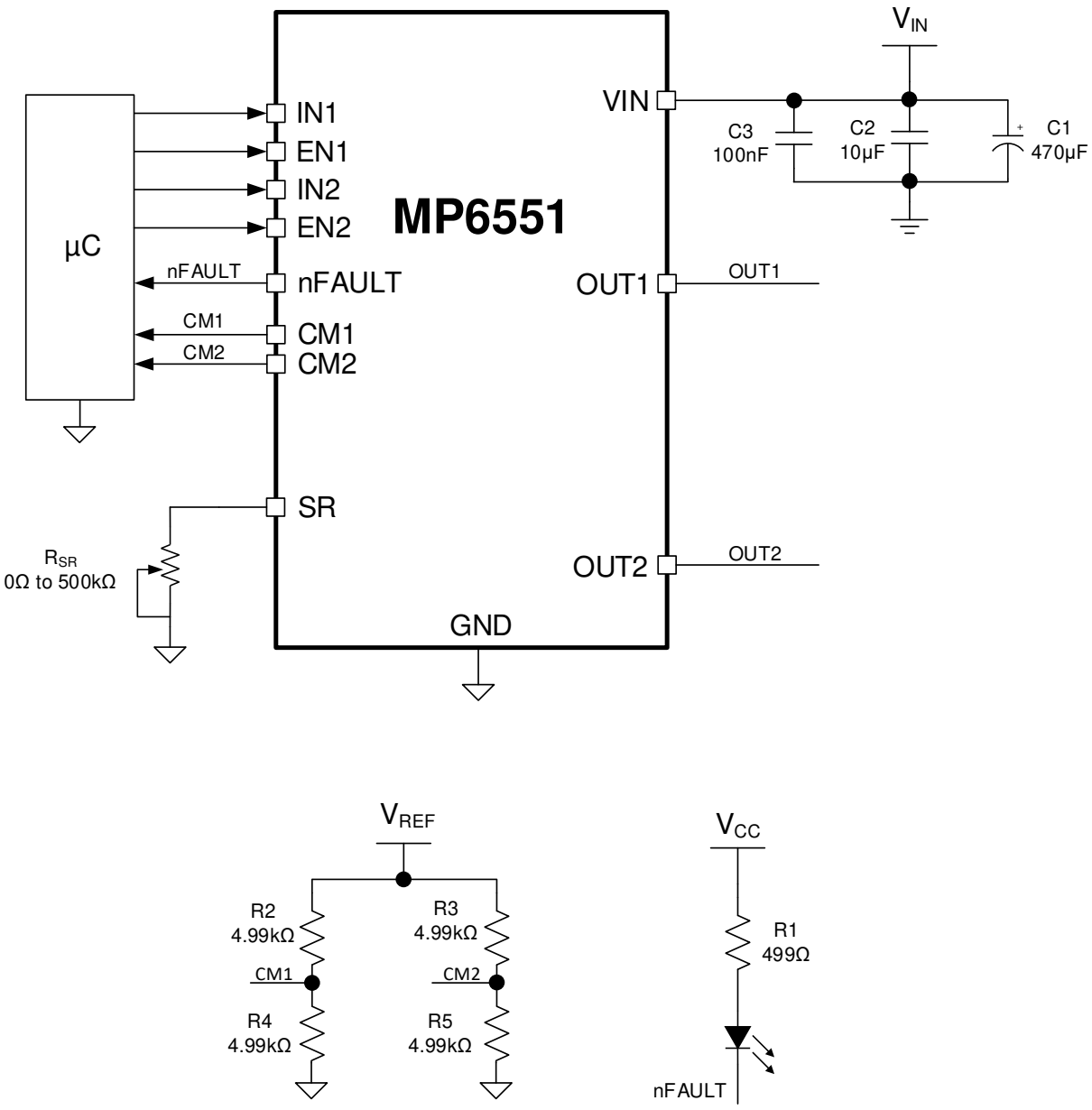
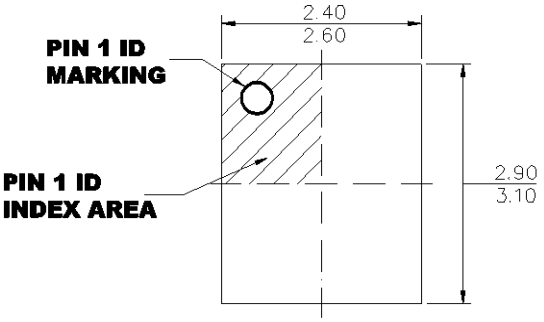


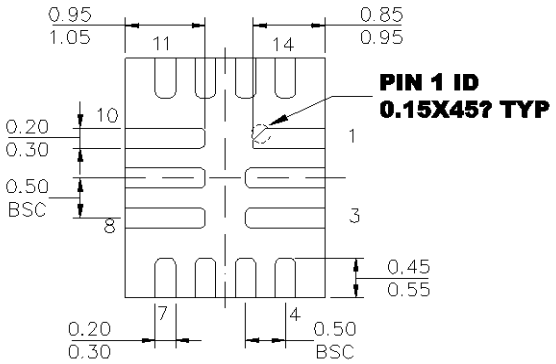
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

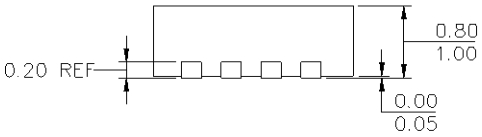
QFN-14 (2.5mmx3mm)



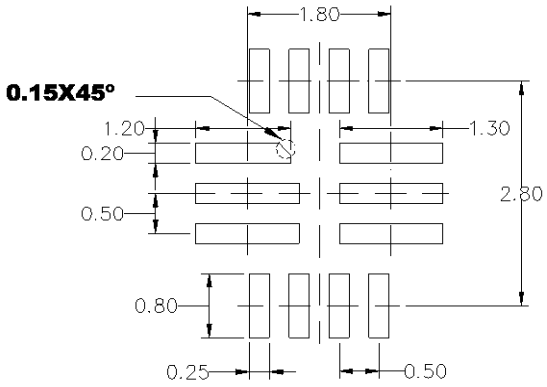
TOP VIEW



BOTTOM VIEW



SIDE VIEW

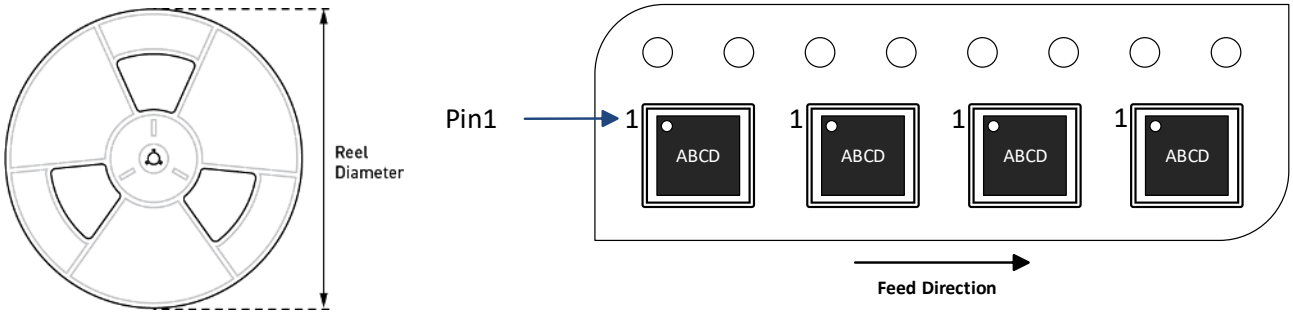


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN2~PIN3 AND PIN8~PIN10 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6551GQB-Z	QFN-14 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/07/2021	Initial Release	-