VoiceEdge

Le77D11

Voice Over Subscriber Line Interface Circuit
VE770 Series

APPLICATIONS

- **Short/Medium Loop: approximately 2000 ft. of 26 AWG, and 5 REN loads**
- **Voice over IP/DSL – Integrated Access Devices, Smart Residential Gateways, Home Gateway/Router**
- **Cable Telephony – NIU, Set-Top Box, Home Side Box, Cable Modem, Cable PC**
- **Fiber–Fiber In The Loop (FITL), Fiber to the Home (FTTH)**
- **Wireless Local Loop, Intelligent PBX, ISDN NT1/TA**

FEATURES

- **Integrated Dual-Channel Chip set**
  - — Built-in boost switching power supply tracks line voltage minimizing power dissipation
  - — Only +3.3 V and +12 V (nominal) required
  - — Wide range of input voltages (+8 V to +40 V) supported
  - — Minimum external discrete components
  - — 44-pin eTQFP package
- **Ringing**
  - — 5REN
  - — Up to 90 Vpk, Balanced
  - — Sinusoidal or trapezoidal with programmable DC offset
- **Subscriber Loop Test/Self-Test**
  - — GR-909 compliant drop test capability in both measurements and pass/fail
    - – Hazardous Potential
    - – Foreign Electromotive Force
    - – Resistive Faults
    - – Receive Off-hook
    - – Ringers Test
    - – Loop Length
- **World Wide Programmability:**
  - — Two-wire AC impedance
  - — Dual Current Limit
  - — Metering
  - — Programmable loop closure and ring trip thresholds
- **Six SLIC Device States, including:**
  - — Low power Standby state
  - — On-hook transmission
  - — Reverse Polarity

RELATED LITERATURE

- **080697 Le78D11 Data Sheet**
- **080716 Le77D11/Le78D11 Chip Set User's Guide**
- **081013 Layout Considerations for the Le77D11 and Le9502 Application Note**

ORDERING INFORMATION

An Le78D11 VoSLAC™ device must be used with this part.

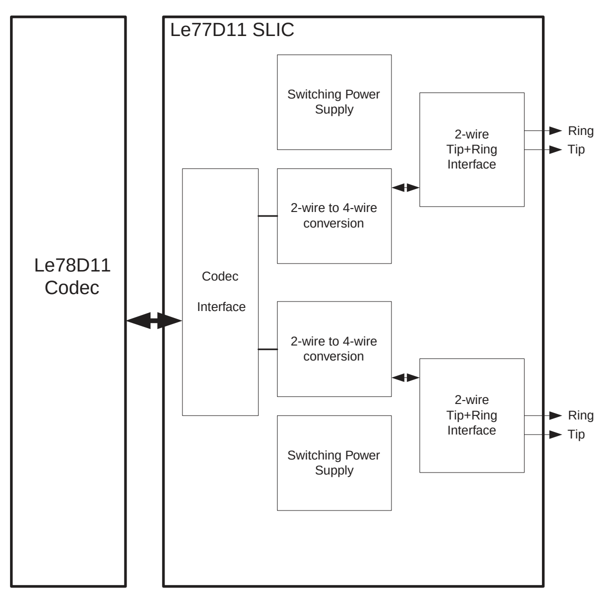
Device	Package
Le77D112TC	44-pin eTQFP
Le77D112BTC	44-pin eTQFP (Green package)*

**Green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*

DESCRIPTION

The Zarlink Le77D11 dual-channel Voice over Subscriber Line Interface Circuit (VoSLIC™) device has enhanced and optimized features to directly address the requirements of voice over broadband applications. Their common goal is to reduce system level costs, space, and power through higher levels of integration, and to reduce the total cost of ownership by offering better quality of service. The Le78D11/Le77D11 is a two-device chip set providing a totally software configurable solution to the BORSCHT functions for two lines. The resulting system is less complex, smaller, and denser, yet cost effective with minimal external components. The Le77D11 Dual VoSLIC device requires only two power supplies: +3.3 VDC and nominally +12 VDC, but can range from +8 to +40 VDC depending on the application. A single TTL-level clock source drives the two switching regulators that generate the required line voltage dynamically on a "per line" basis. Six programmable states are available: Low Power Standby, Disconnect, Normal Active, Reverse Polarity, Ringing and Line Test. Binary fault detection is provided upon application of fault conditions or thermal overload.

BLOCK DIAGRAM



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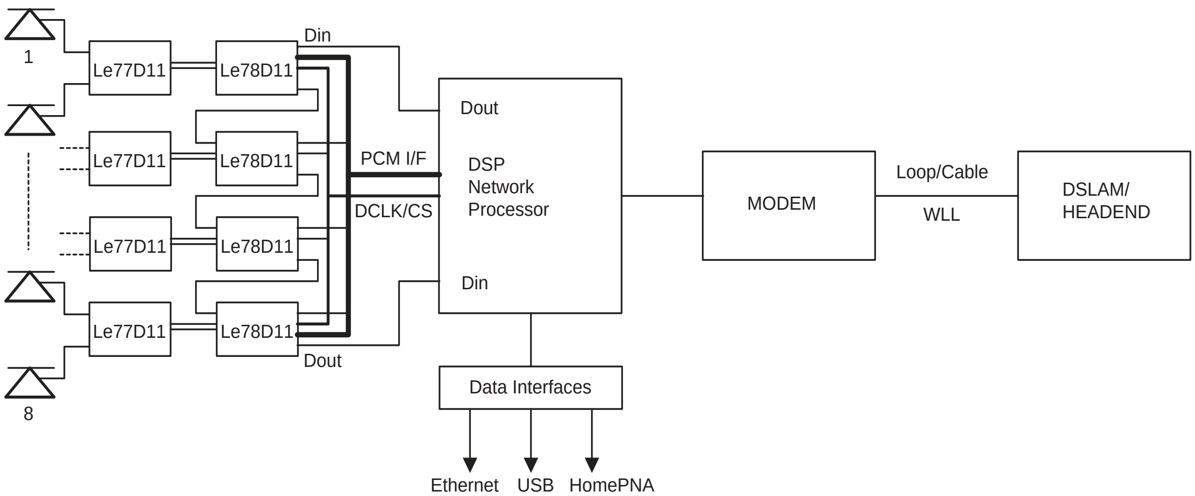
PRODUCT DESCRIPTION

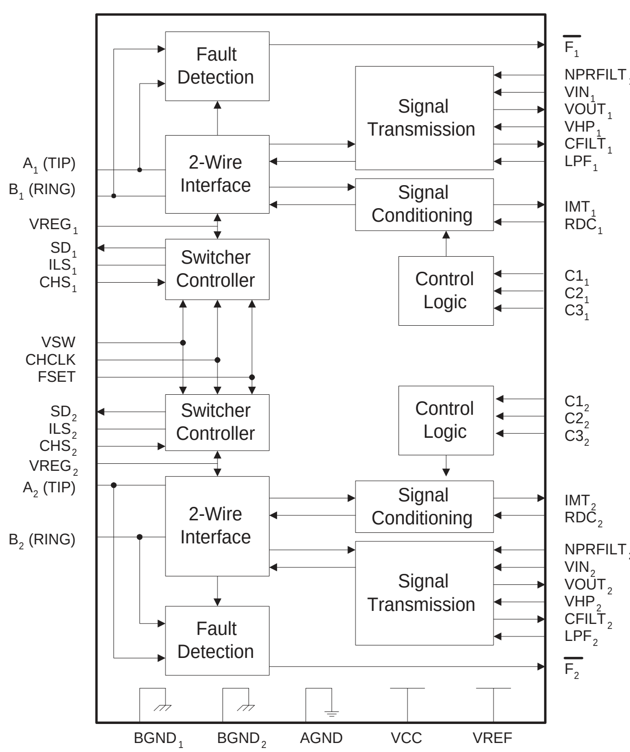
The dual channel Le77D11 VoSLIC device uses reliable, dielectrically isolated, fully complementary bipolar technology to implement BORSCHT functions for short loop applications. Internal power dissipation is minimized by two independent line voltage tracking, buck-boost switching regulators. Two power supplies are required: 3.3 V and a positive supply (V_{SW}). A TTL-level clock driven by the Le78D11 VoSLAC device is required for switcher operation. Six programmable states control loop signaling, transmission, and ringing. The Le77D11 Dual VoSLIC device DC current limit (I_{SC}) is programmable from 15 to 45 mA. The following diagram demonstrates a typical application.

Figure 1. Typical Le77D11 VoSLIC™ Device/Le78D11 VoSLAC™ device Application in an 8-Port Integrated Access Device in Customer Premises



BLOCK DESCRIPTIONS

Figure 2. Le77D11 VoSLIC™ Device Block Diagram



Two-Wire Interface

The two-wire interface block provides DC current and sends/receives voice signals to a telephone connected via the A_i (Tip) and B_i (Ring) pins. The A_i (Tip) and B_i (Ring) pins are also used to send the ringing signal to the telephone. The Le77D11 VoSLIC device can also be programmed in Disconnect state to place the A and B pins at high impedance with the Switching Regulator disabled.

DC Feed

DC feed control in the Le78D11/Le77D11 chip set is implemented in the Le77D11 VoSLIC device. The current limit threshold (I_{LTH}) can be programmed via the MPI interface of the Le78D11 VoSLAC device. The current limit threshold (I_{LTH}) can be programmed up to 30 mA using the recommended R_{DC} value.

Referring to Figure 3, the DC feed curve consists of two distinct regions. The first region is a flat anti-sat region that supplies a constant Tip-Ring voltage (V_{AB} open). The second region is a constant current region that begins when the loop current reaches the programmed current limit threshold (I_{LTH}). This region looks like a constant current source with 3.2 kΩ shunt resistor. The short circuit current is nominally 14.4 mA greater than I_{LTH}.

A block diagram of the DC feed control circuit is shown in Figure 4. In the anti-sat region, current source CS1 creates a constant reference current, which is limited to sub-voice frequencies by C_{LPFi}. This filtered current is then steered by the Polarity Control, depending on whether the VoSLIC device mode is Standby, Normal Active, or Reverse Polarity. The steered current then takes one of two paths to the Level Shift block, where it is used to set V_A (TIP) and V_B (RING). This voltage from the Level Shift block is buffered by the output amplifiers and appears at A_i (TIP) and B_i (RING).

When $I_{LOOP}/500$ becomes greater than $I_{LTH}/500$, the difference is subtracted from CS1, and again filtered by C_{LPFi}. This reduced current causes a reduced DC feed voltage. In Standby and Normal Active, A_i (TIP) is held constant, while B_i (RING) is changed to reduce the feed voltage. In Reverse Polarity, A_i (TIP) and B_i (RING) are swapped. When $(I_{LOOP}\text{-}I_{LTH})/500 = \text{CS1}]$, all of the current from CS1 is subtracted, making the TIP-RING voltage = 0 V. This is the short circuit condition. At least 100 Ω loop and fuse resistance are required to ensure stability of the A_i (TIP) and B_i (RING) output amplifiers.

The capacitor C_{LPFi}, in conjunction with an internal 25-kΩ resistor (not shown) is used to create a low pass filter for the DC feed loop. This capacitor should nominally be 4.7 µF, setting a 1.4 Hz pole. The purpose of this filter is to separate the operation of the DC feed from voice frequencies, preventing distortion and idle-channel noise.

Normal or Reverse Polarity is controlled by the Le78D11 VoSLAC device through the C3-1 state control pins. Some applications require slew rate control of the transition between these feed states. The capacitor, C_{NPRi}, may be used to increase the transition time and create a quiet polarity change. In the Normal Active state, the $NPRFILT_i$ pin is driven up to V_{CC}.

When Reverse Polarity is selected, C_{NPRi} is discharged by current I_{NPR}, and the transition time is:

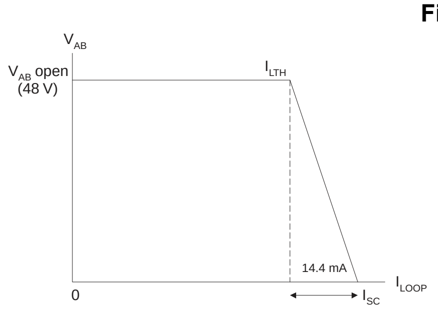
$$\Delta t = \frac{(V_{CC} - V_{REF}) \bullet C_{NPRi}}{I_{NPR}}$$

In the Reverse Polarity state, the $NPRFILT_i$ pin is discharged near ground. When Normal Active is selected, C_{NPRi} is charged by current I_{NPR}, and the transition time is:

$$\Delta t = \frac{V_{REF} \bullet C_{NPRi}}{I_{NPR}}$$

A 100-nF capacitor provides a nominal Normal Active to Reverse Polarity transition time of about 5 ms and a Reverse Polarity to Normal Active transition time of 3 ms.

Figure 3. DC Feed Curve



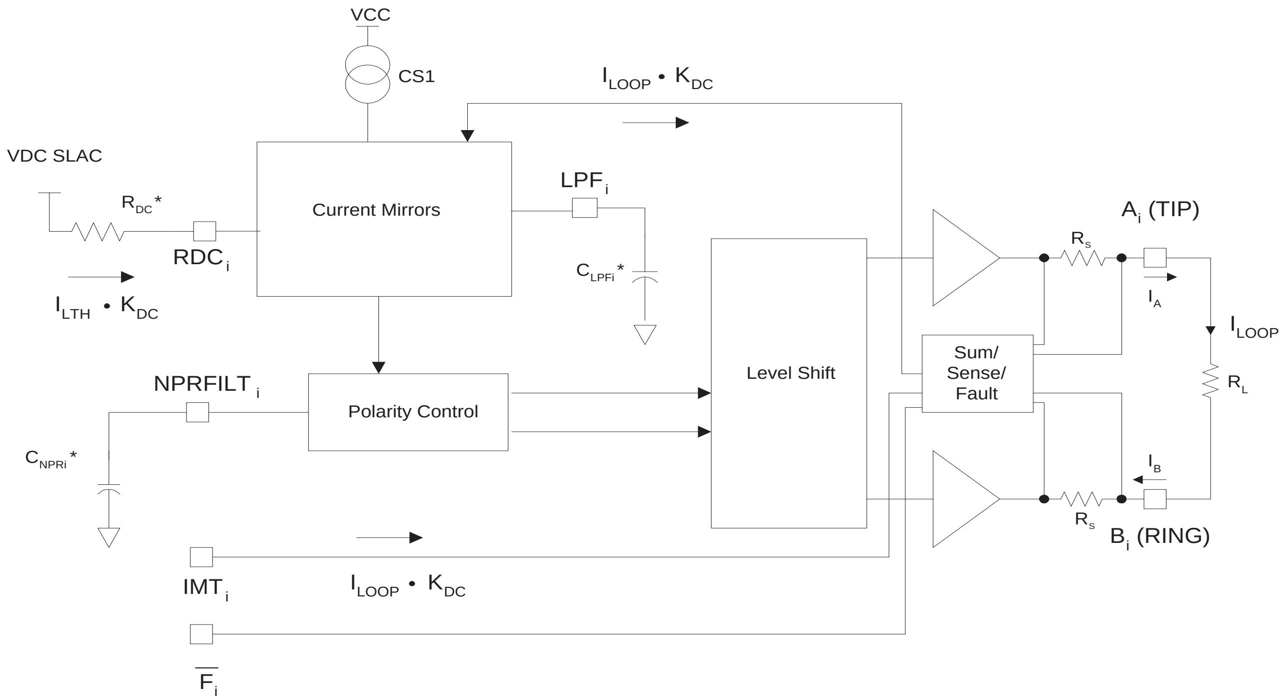
$$I_{SC} = I_{LTH} + 14.4\text{mA}$$

$$I_{LTH} = \frac{V_{DC}}{R_{DC}K_{DC}} = \frac{V_{DC}}{40}$$

Notes:

1. *V_{DC} is programmable via the Le78D11 VoSLAC device. (V_{DC} = 0.00 V to 1.20 V relative to V_{REF})*
2. *V_{REF} = 1.4 V nominal.*
3. *K_{DC} = Le77D11 VoSLIC device DC current gain.* $K_{DC} = \frac{I_{IMT}}{I_{LOOP}}$.
4. *R_{DC} = external resistor 20 kΩ nominal.*
5. *$V_{AB} = V_{Ai} – V_{Bi}$ Tip-Ring differential voltage.*
6. *I_{SC} = Loop short circuit current limit.*
7. *I_{LTH} = Loop current limit threshold. I_{LTH} should be programmed to 15 mA or less when in the Standby state.*
8. *These are nominal values for DC feed curve. See the "Device Specifications" table for tolerance values.*

Figure 4. DC Feed Block Diagram, Active and Standby Modes



Note:

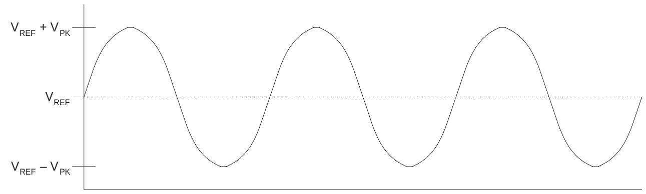
** denotes external components*

Ringing

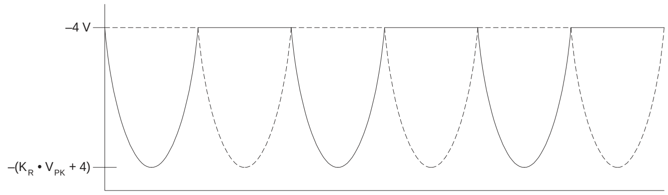
Ringing is accomplished by placing the Le77D11 VoSLIC device into the Ringing state via the Le78D11 VoSLAC device's MPI interface. Placing the Le77D11 VoSLIC device into the ringing state automatically enables signal generator A in the Le78D11 VoSLAC device which puts the ringing signal on the receive signal path (pin VIN). (For information on programming the Le78D11 VoSLAC device's signal generators, please refer to the *Le77D11 /Le78D11 Chip Set User's Guide*, document ID# 080716). When the Le77D11 VoSLIC device is in the ringing state, the gain from the input pin, VIN, to the output is K_R, the ringing voltage gain. The output waveform is a quasi-balanced waveform, as shown in Figure 5. On the positive half cycle of the input waveform, when ($V_{IN} – V_{REF}$) is positive, V_{AB} is positive with $V_{A(TIP)}$ near –4 V and $V_{B(RING)}$ brought negative. When ($V_{IN} – V_{REF}$) is negative, $V_{B(RING)}$ is held near –4 V and $V_{A(TIP)}$ is brought more negative. The waveform can be either sinusoidal or trapezoidal under the control of the Le78D11 VoSLAC device.

To provide 90-V ringing capability, the application of a PNP bipolar switching transistor is used. For the reference schematic, Zetex part FZT955 in a SOT-223 package is used. Its V_{CEO} rating is 140 V. Due to the switching efficiency and overhead voltage, one can achieve 90 Vpk sinusoidal ringing with a 5 REN load with V_{SW} = 12 V. See *Figure 6, Switching Power Supply Block Diagram, on page 7* for external filters recommended for a 90-V peak ringing application.

Figure 5. Ringing Waveforms



A. Voltage Applied to VIN Pin



B. Voltage Output at A (Tip) (dashed line) and B (Ring) (solid line) Pins

Switcher Controller

The switcher controller's main function is to provide a negative power supply (V_{REG}) that tracks Tip and Ring voltage for the two-wire interface. As Tip and Ring voltage decreases, the switcher will likewise lower V_{REG}. In doing so, the switcher saves power because the device is not forced to maintain static supply voltage in all states.

The switching power supply controller uses a discontinuous mode buck-boost voltage converter topology. The frequency of operation is programmed by the Le78D11 VoSLAC device and is typically 85.3 kHz (256 kHz/3). The Le78D11 VoSLAC device outputs a clock at its programmed frequency with approximately a 10% duty cycle which is fed into the CHCLK pin of the Le77D11 VoSLIC device. This clock signal controls the switching supply's operating frequency as well as the switching supply's maximum duty cycle. The Le77D11 VoSLIC device adjusts the actual duty cycle up to the maximum of 90% depending on the magnitude of the error voltage on the compensation (CHS) pin. The error signal is generated by integrating the difference in control current which is set by the Le77D11 VoSLIC device, and the feedback current. This error signal will converge to a value which in turn sets the duty cycle of the switching supply to satisfy feedback loop requirements.

A control current (See Figure 6, *Switching Power Supply Block Diagram*, on page 7) is generated on the Le77D11 VoSLIC device and is set to force V_{REG} to track Tip and Ring line conditions to optimize system power efficiency. In equilibrium, the control current, which is fed into the CHS summing node, is set to provide the required line voltage plus an offset to give headroom for the power amplifiers.

The error signal on CHS is compared to an internal ramp signal. The ramp rate of this internal ramp signal is set by a resistor, R_{RAMP}, to analog ground (AGND) on the FSET pin. A 1% resistor should be chosen to give the ramp precise control, and prevent internal nodes from going into saturation. R_{RAMP} is determined by the equation: $R_{RAMP} = (24 \cdot 10^9\ \Omega\text{-Hz})/(\text{CHCLK Frequency})$.

When the CHCLK signal goes from a logic high to a logic low, it will initiate a cycle by resetting the ramp, resetting a current limit latch, and turning on the external power switch. Then, on a cycle-by-cycle basis, one of three events will shut off the power switch depending on which event occurs first:

a) The ramp voltage exceeds the error voltage that is integrated on the CHS node (normal voltage feedback operation).
b) The CHCLK goes high (90% duty cycle point is reached).
c) The power switch current limit threshold is reached.

Cycle-by-cycle current limiting is provided by the current sense ILS pin which senses the external power switch current through the resistor R_{LIM}. If this pin exceeds −0.28 V with respect to V_{SW}, the switching supply will set the current limit latch and shut off the external switch drive until the CHCLK pin goes high to reset the latch. This peak inductor current, and also peak switching converter power output can be controlled on a cycle-by-cycle basis and set by the equation $I_{LIM} = |0.28\ V|/R_{LIM}$.

This sensing configuration has the added benefit that if the clock signal is removed for some reason, the power switch cannot be left on indefinitely.

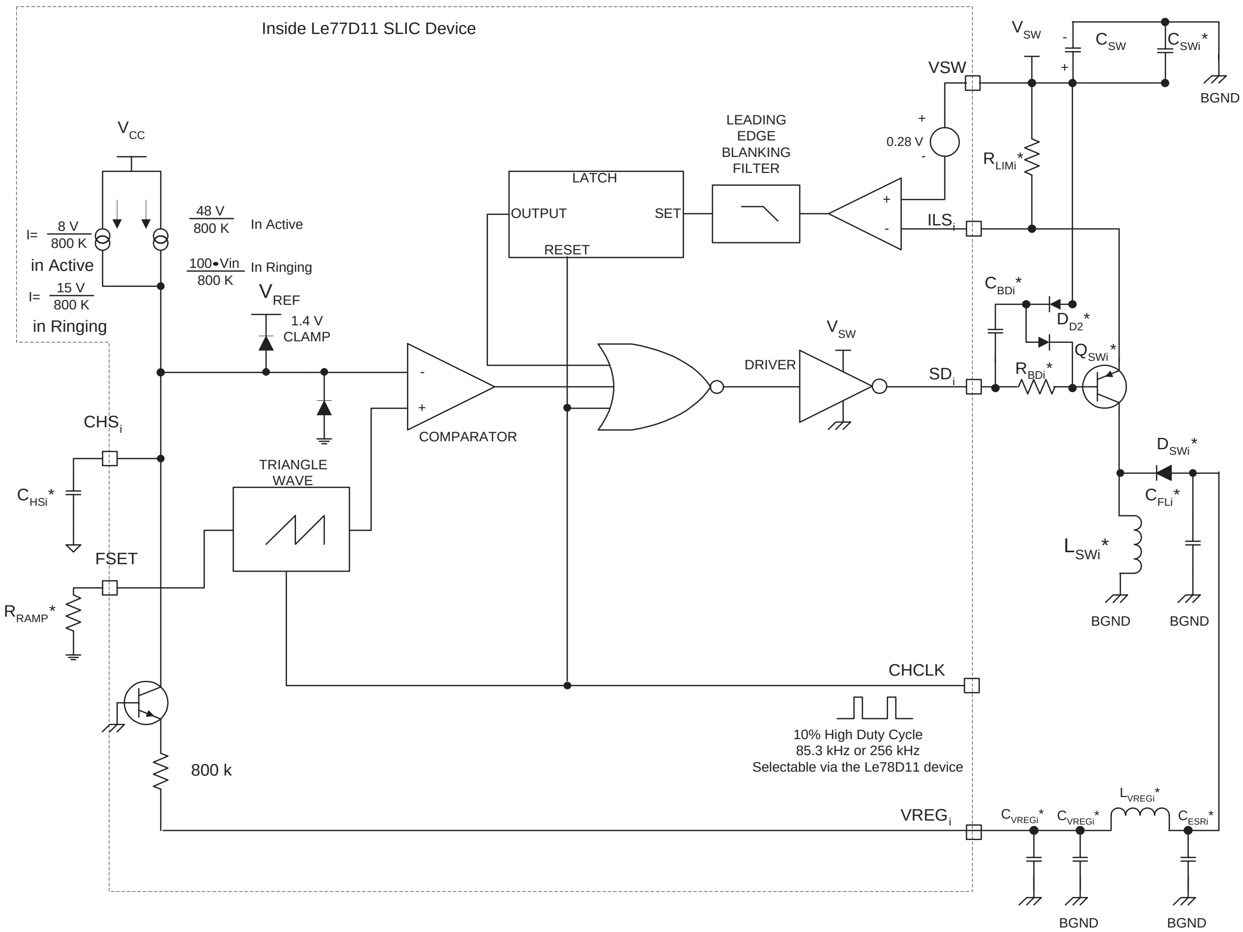
A leading edge blanking filter is added at the output of the latch to ignore the first 150 ns of a current limit event. This feature is used to ignore a false current trip that may be caused by the power switch driving the reverse recovery charge (Q_{RR}) of the external power rectifier.

This circuit has been optimized for operation to supply 20-Hz ringing of 90-V peak with a nominal supply voltage, V_{SW}, of 12 V.

The on chip driver is designed to drive an external PNP transistor. Its output drive is clamped between 7-9 V below V_{SW}, and can source or sink approximately 100 mA. The driver has approximately 50 Ω of source resistance. When a PNP transistor is used, additional resistance should be added from the SD_i pin to the base of the external power device.

For this application, R_{BD} is 180 Ω and capacitor C_{BD} is 27 nF to increase the switching speed and efficiency. This increases the power available during the Ringing state when the converter operates at the highest currents. The capacitors C_{FL} and C_{VREG} use very low ESR film capacitors to minimize ripple and noise on V_{REG}. The capacitance is sized to permit more rapid charging of the capacitors, and hence a faster slew rate. Reduction of switcher noise is accomplished by using lower ESR capacitors and increasing the value of the L_{VREG} inductor in the post filter. The power supply output is able to track the ringing waveform under these conditions.

Figure 6. Switching Power Supply Block Diagram



Note:

** denotes external components*

Signal Transmission

In Normal Active and Reverse Polarity states, the AC line current is sensed across the internal resistors, R_S (see *Figure 7, Transmission Block Diagram, on page 8*), summed, attenuated and converted to voltage at the CFILT pin. This voltage then goes through a high pass filter (with a nominal 13 Hz corner frequency), implemented using an on-chip 8 kΩ nominal resistor and an external C_{HP} capacitor, is amplified, and sent to the Le78D11 VoSLAC device at the VOUT pin. The output is proportional to the AC metallic component of the line voltage. Additionally, the signal transmission block receives the analog signal from the Le78D11 VoSLAC device. The analog signal is amplified and sent to the line.A proportion of the signal at V_{OUT} is also fed back to the line.

There are three parameters which define the AC characteristics of the Le77D11 VoSLIC device. First is the input impedance presented to the line or two-wire side (Z_{2WIN}), second is the gain from the four-wire (V_{IN}) to the two-wire (V_{AB}) side (G_{42}), and third is the gain from the two-wire side to the four-wire (V_{OUT}) side (G_{24}).

Input Impedance (Z_{2WIN})

Z_{2WIN} is the impedance presented to the line at the two-wire side, and is defined by:

$$Z_{2WIN} = 2R_F + K_V K_{OUT} R_{IMT}$$

where 2 • R_F is the total resistance of the external fuse resistors in the circuit, R_{IMT} is the impedance setting resistor, K_{OUT} is the gain from V_{OUT} to V_{AB}, and K_V is the voice current gain defined in the Transmission Specifications Table. Note that the equation reveals that Z_{2WIN} is a function of the selectable resistors, R_{IMT} and R_F. For example, if $R_F = 0\ \Omega$ and R_{IMT} is 100 k, the terminating impedance is 600 Ω. This is the configuration used in this data sheet for defining the device specifications. However, in a real application, $R_F = 50\ \Omega$ is recommended, producing a total input impedance of 700 Ω which is a good starting point for meeting worldwide requirements using the programmable filters of the Le78D11 VoSLAC device.

Two-Wire to Four-Wire Gain (G_{24})

The two-wire to four-wire gain is the gain from the phone line to the VOUT output of the Le77D11 VoSLIC device. To solve for G_{24}, the VIN pin is grounded (see Figure 7).

$$\frac{V_{OUT}}{V_{AB}} = G_{24} = \frac{1}{\frac{2R_F}{K_V R_{IMT}} + K_{OUT}}$$

or

$$G_{24} = -20\log\left(K_{OUT} + \frac{2R_F}{K_V R_{IMT}}\right) \text{ in dB}$$

Using the values of R_{IMT} and R_F from the application example, G_{24} for this circuit is –10.9 dB.

Four-Wire to Two-Wire Gain (G_{42})

G_{42} is the gain from the VIN input to the line. This gain is defined as V_{AB}/V_{IN}.

$$\frac{V_{AB}}{V_{IN}} = G_{42} = \frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT}R_{IMT}K_V}{R_L + 2R_F}\right)}$$

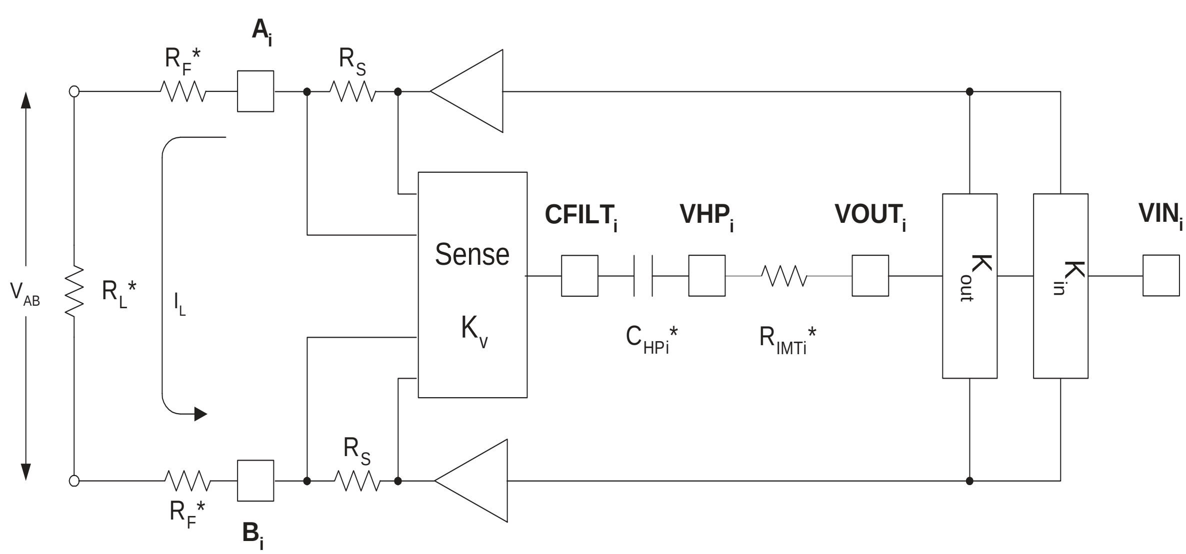
or

$$G_{42} = -20\log\left(\frac{K_{IN}\left(\frac{R_L}{R_L + 2R_F}\right)}{\left(1 + \frac{K_{OUT}R_{IMT}K_V}{R_L + 2R_F}\right)}\right) \text{ in dB}$$

where K_{IN} is the gain from VIN to V_{AB}. Using the values of R_{IMT} and R_F from the application example and $R_L = 600\ \Omega$, G_{42} for this circuit is 7.3 dB.

Note:
Equation derivations can be found in the Zarlink Le77D11/Le78D11 Chip Set User's Guide (document ID# 080716).

Figure 7. Transmission Block Diagram



Note:
** denotes external components*

Fault Detection

Each channel of the Le77D11 Dual VoSLIC device has a fault detection pin, $\overline{F}_1$ or $\overline{F}_2$. These pins are driven low when a longitudinal current fault or foreign voltage fault occurs (see Figure 4, *DC Feed Block Diagram, Active and Standby Modes*, on page 5). When not in Disconnect state, there are three conditions that will cause the $\overline{F}_i$ pin to indicate a fault condition:

- $|I_A - I_B| > I_{LONG}$
- In Normal Active and Standby state, a foreign voltage fault occurs in which V_A is above ground or V_B is close to V_{REG}.
- In Reverse Polarity state, a foreign voltage fault occurs in which V_B is above ground or V_A is close to V_{REG}.

In the Disconnect state, fault detection is not supported; however, fault conditions can be monitored by the Le78D11 device.

For more details on AC, DC fault detection, loss of power, or clock-failure alarm, please refer to the Zarlink *Le77D11/Le78D11 Chip Set User's Guide* (document ID# 080716).

Signal Conditioning

The RDC_i pin is used to set the DC feed current limit, as described in the DC feed section.

The IMT_i pin provides K_{DC} times the loop current to the Le78D11 VoSLAC device. The Le78D11 VoSLAC device implements all loop supervision and ring trip processing on this signal.

$$I_{IMT} = \frac{I_A + I_B}{2} \bullet K_{DC}$$

Thermal Overload

When the die temperature around the power amplifier of an Le77D11 Dual VoSLIC device channel reaches approximately 160°C, the IMT pin of that channel is pulled High. At the same time, all the blocks controlling that channel of the device are shut off, except for the logic interface block. The VoSLIC channel goes into a state similar to Disconnect, making the line current zero. When the temperature drops below 145°C, the VoSLIC channel returns to its previous state. It is important to recognize that even while a channel experiences thermal overload, the state of the device can be modified. At TSD, the switcher is turned off.

Control Logic

Each channel of the Le77D11 VoSLIC device has three input pins from the Le78D11 VoSLAC device (C3, C2, and C1). The inputs set the operational state of each channel. There are six operational VoSLIC device states (See Table 1): Low Power Standby, Disconnect, Normal Active, Reverse Polarity, Ringing and Line Test. This leaves two reserved logic states.

Table 1. Device Operating States

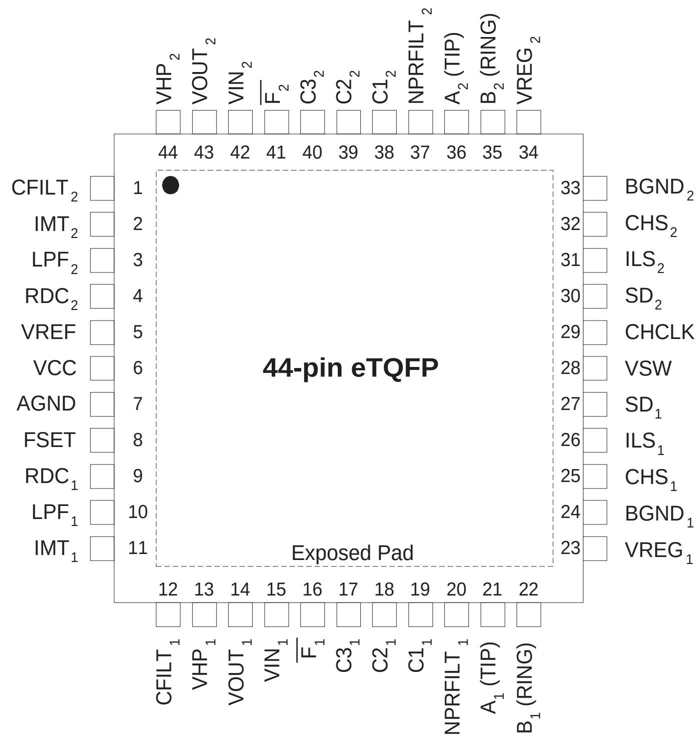
C3	C2	C1	Operating Mode	Description
0	0	0	Low Power Standby	Voice transmission disabled. Maximum loop current capability and loop current sensing range are reduced.
0	0	1	Disconnect	Le77D11 Dual VoSLIC device channel is shut down and switching power supply is shut off.*
0	1	0	Normal Active	Le77D11 Dual VoSLIC device channel fully operational. A_i (TIP) is more positive than B_i (RING). Also used for on-hook transmission.
0	1	1	Reverse Polarity	Similar to normal active, but DC polarity is reversed so that the B_i (RING) lead is more positive than the A_i (TIP) lead. Also used for on-hook transmission.
1	0	0	Ringing	Ringing state with V_{AB} set to $K_R \bullet V_{IN}$. The switching supply maintains minimum headroom for the sourcing and sinking amplifiers in order to maximize power efficiency.
1	0	1	Line Test State	Similar to ringing state with reduced bias currents for lower noise. Loop current sensing range is limited. See IMT pin specifications.
1	1	0	Reserved	Not used.
1	1	1	Reserved	Not used.

Note:

** When in Disconnect state, the DC-DC converter is disabled and the V_{REG} voltage will decay to 0 V. The A_i and B_i outputs are disabled; however, they still have ESD protection diodes to BGND and VREG which will provide a low impedance clamp to any line voltages >± 0.5 V.*

**When transitioning from any state to Disconnect, the Le77D11 device momentarily passes through Reverse Polarity, pulling the A-lead towards Vreg. During line testing, when the SLIC device is placed in the Disconnect state, wait >3 seconds before proceeding with line measurements.*

CONNECTION DIAGRAM



Note:

1. *Pin 1 is marked for orientation.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND	Ground	Analog and digital ground return for VCC circuitry (common to both channels).
$A_{1,2}$ (Tip)	Output	A (Tip) lead power amplifier outputs for channels 1 and 2.
$BGND_{1,2}$	Ground	Supply ground return for power amplifiers on channel 1 and 2.
$B_{1,2}$ (Ring)	Output	B (Ring) lead power amplifier outputs for channels 1 and 2.
$C1_1$, $C2_1$, $C3_1$	Input	Logic control inputs to control channel 1 state.
$C1_2$, $C2_2$, $C3_2$	Input	Logic control inputs to control channel 2 state.
$CFILT_{1,2}$	Output	AC coupling pins for 4-wire (VOUT) amplifiers of channels 1 and 2.
CHCLK	Input	Switching power supply clock input that sets the frequency and maximum duty cycle of the switcher (common to both channels).
$CHS_{1,2}$	Input	Compensation nodes for switching power supply channels 1 and 2.
$\overline{F}_{1,2}$	Output	Fault detect pins for channels 1 and 2. A low indicates a fault for the respective channel, which can be triggered by large longitudinal current, or ground key.
FSET	Input	Ramp rate control pin for 85.3 kHz operation.
$IMT_{1,2}$	Output	Current output equal to the loop current divided by 500. During thermal overload, IMT is forced High.
$ILS_{1,2}$	Input	Voltage sense pins to limit peak current in external switching power supply transistors (channels 1 and 2).
$LPF_{1,2}$	Output	A capacitor tied from these pins to AGND stabilizes the DC feed loop, and lowers Idle Channel Noise for channels 1 and 2.
$NPRFILT_{1,2}$	Output	An optional capacitor tied from these pins to AGND controls the reverse polarity slew rate of channels 1 and 2.
$RDC_{1,2}$	Input	Resistor connection to programmable VDC_i pin of Le78D11 VoSLAC device to set DC feed current limit threshold (I_{LTH}) of each channel.
$SD_{1,2}$	Output	Base (gate) drive for switching power supply transistor (channels 1 and 2).
VCC	Supply	A nominal 3.3 V power supply for internal VCC circuitry (common to both channels).
$VHP_{1,2}$	Output	High pass inverting summing nodes of the VOUT amplifiers driven by the AC current coming from $CFILT_1$ and $CFILT_2$.
$VOUT_{1,2}$	Output	Analog (4-wire side) VOUT amplifier output.
$VIN_{1,2}$	Input	Analog (4-wire side) voice or ringing signal inputs. These pins multiplex between 4-wire voice input and ringing input depending on the programmed state of the Le77D11 VoSLIC device channel.
VREF	Supply	A nominal 1.4 V reference supplied by the Le78D11 VoSLAC device for internal use (common to both channels).
$VREG_{1,2}$	Supply	Negative regulated power supplies generated by the Le77D11 VoSLIC device Switching Regulators. (Channels 1 and 2).
VSW	Supply	A positive supply used to generate the negative supplies of V_{REG1}, V_{REG2} (common to both channels).
Exposed Pad	Isolated	Exposed pad on underside of device must be connected to a heat spreading area. The AGND plane is recommended.

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150°C
Ambient temperature, under bias	-40° to 85°C
V_{CC} with respect to AGND	–0.4 to +6.5 V
V_{REG} with respect to BGND	+0.4 to –115 V
BGND with respect to AGND	–100 to 100 mV
A (Tip) or B (Ring) to BGND:	
Continuous	V_{REG} –1 to BGND +1
10 ms (F = 0.1 Hz)	V_{REG} –5 to BGND +5
1 µs (F = 0.1 Hz)	V_{REG} –10 to BGND +10
250 ns (F = 0.1 Hz)	V_{REG} –15 to BGND +15
Current from A (Tip) or B (Ring)	±150 mA
C1, C2, C3 to AGND	–0.4 to VCC + 0.4 V
CHCLK	AGND to VCC
V_{SW}	BGND to +44 V
V_{REF}	AGND to VCC
Maximum power dissipation, T_A = 85° C (See notes)	1.8 W
Thermal Data: In 44-pin eTQFP package	θ_{JA} 32° C/W
Thermal Data: In 44-pin eTQFP package	θ_{JC} 9.2° C/W
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165ºC. Continuous operation above 145ºC junction temperature may degrade device reliability.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through 16 0.3 mm diameter vias on a 1.27 mm pitch to a large (> 500 mm^2) internal copper plane. (Refer to Zarlink application note Layout Considerations for the Le77D112 and Le9502 Devices, document ID# 081013).

Package Assembly

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

OPERATING RANGES

Zarlink guarantees the performance of this device over commercial (0° to 70°C) and industrial (–40° to 85°C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	-40° to 85°C

Electrical Ranges

V_{CC}	3.3 V ± 5%
V_{SW}	8 to 40 V
V_{REF}	1.40 V ± 50 mV
V_{REG}	–7 to –110 V (0 V in Disconnect state)

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, test conditions are: V_{CC} = 3.3 V, V_{SW} = 12.0 V, V_{REF} = 1.4 V. For Active, Reverse Polarity, Line Test and Disconnect, V_{DC} = 0.6 V (I_{LTH} = 15 mA); for Standby, V_{DC} = 0.4 V (I_{LTH} = 10 mA). AGND = BGND, there are no fuse resistors, R_L = 600 Ω, –40°C < T_A < 85°C, 85.3 kHz CHCLK. Ringing configuration is V_{IN} = 0.7 Vpk 20-Hz sinusoidal. Line Test configuration is V_{IN} = 0.5 Vdc. Please refer to the test circuit on page 18 for all other component values.

Supply Currents and Power Dissipation

Operation States	Condition	3.3 V VCC Supply Current (mA)			VREG Supply Current (mA) (Note 4)			VREG Supply Power (mW)			SLIC Device Power (mW) (Note 5)			VSW Pin Current (mA)	Note
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Typ	
Standby	R_L = open V_{IN} =0 V	2	5	7	0.25	0.9	2.2	15	50	105	20	65	110	2.0	1
Disconnect	R_L = open V_{IN} = 0 V	1	3	5	—	0.1	—	0	0.5	3	5	10	15	0.1	1
Active	R_L = open V_{IN} = 0 V	3	6	9	1	3	4.2	75	160	245	80	165	250	2.5	1
	R_L = 900 Ω V_{IN} = 0 V	—	7	—	—	26	—	—	820	—	—	360	—	4.6	1, 2
	R_L = 300 Ω V_{IN} = 0 V	4	7	10	26	33	40	500	730	1000	300	430	565	4.1	1
Pol Rev	R_L = open V_{IN} = 0 V	3	6	9	1	3	4.2	75	160	245	80	165	250	2.5	1, 2
	R_L = 900 Ω V_{IN} = 0 V	—	7	—	—	26	—	—	833	—	—	360	—	4.6	1, 2
	R_L = 300 Ω V_{IN} = 0 V	4	7	10	26	33	40	500	730	1000	300	430	565	4.1	1
Ringing	R_L = open V_{IN} = 0.7 Vac	—	6	—	—	3	—	—	152	—	—	180	—	2.1	1, 2
	R_L = 1400 Ω V_{IN} = 0.7 Vac	4	7	9	33	38	42	2000	2500	2900	600	750	900	5.7	1, 3
Line Test	R_L = open V_{IN} = 0.5 Vdc	2	5	8	1	2	5	90	170	280	90	170	280	2.6	1

Notes:

1. *Values shown are for one channel only but are tested with both channels in the same state.*
2. *Not tested in production. Parameter is guaranteed by characterization or correlation to other tests.*
3. *Production test forces Vin=0.5 Vdc which is equivalent to Vin=0.7 Vac.*
4. $I_{VSW} = \frac{V_{REG} \bullet I_{VREG}}{\eta \bullet V_{SW}}$ *, where* η *= efficiency. For our recommended circuit, an efficiency of 0.6 can be assumed under heavy loads.*
5. *VoSLIC device power is defined as the power delivered through the VCC and VREG pins minus the power delivered to the load. It does not include any power associated with the VSW pin and the external switcher.*

SPECIFICATIONS

System Specifications

The performance targets defined in this section are for a system using the Le78D11/Le77D11 chip set. Specifications for the Le78D11 VoSLAC device are published separately.

Item	Condition	Min	Typ	Max	Unit	Note
Output Impedance during internal ringing	Ringing mode, Le78D11 VoSLAC device generating internal ringing		2 • RF		Ω	4.
Sinusoidal Ringing THD	Ringing mode, R_L = 1500 Ω generating internal sinusoidal ringing		2		%	4.
Signaling Performance Limits						
Hook switch threshold	ITH = 10 mA	7		13	mA	4.
Hook switch hysteresis	All ITH settings		10		%	3.
Internal Ring-trip Accuracy	RTSL = 2.2 W (07h)	–20		+20	%	4.

Device Specifications

Specification	Condition	Min	Typ	Max	Unit	Note
Line Characteristics						
V_A, Active V_B, Reverse Polarity	R_L = open		–4		V	
V_A	Standby, R_L = open		–1			
V_{AB}	Active or Reverse Polarity, R_L = open	45	48	51		1.
V_{AB} open	Standby, R_L = open	45	48	54.5		1.
V_{REG}	Active or Reverse Polarity, R_L = open	–50	–58	–66		
V_{REG}	Standby, R_L = open	–49.5	–54	–62		
Current limit threshold I_{LTH} accuracy	Active or Reverse Polarity	13	15	17	mA	4.
	Standby	8	10	12		
Loop Current, I_L accuracy	Active or Reverse Polarity, R_L = 600 Ω; I_{LTH} = 15 mA	I_{LTH} + 7	I_{LTH} + 11.3	I_{LTH} + 20		
	Standby R_L = 600 Ω; I_{LTH} = 10 mA	I_{LTH} + 7	I_{LTH} + 11.5	I_{LTH} + 20		
Short circuit loop current, I_{SC}	Active or Reverse Polarity, R_L = 100 Ω; I_{LTH} = 15 mA	I_{LTH} + 7.8	I_{LTH} + 17	I_{LTH} + 29		
	Standby R_L = 100 Ω; I_{LTH} = 10 mA	I_{LTH} + 10	I_{LTH} + 16	I_{LTH} + 25		
LPF_i	Output impedance		25		kΩ	3.
	Bias voltage with respect to GND		2.4		V	
	Leakage current for capacitor value of 4.7 µF ± 20%			0.1	µA	
$NPRFILT_i$ drive capability	$\|I_{NPR}\|$	20	50	100	µA	
Ringing and Line Test State						
V_A, V_B	V_{IN} = 0 V, with respect to V_{REF}, R_L = 1400 Ω		–4		V	3.
V_{AB} offset	V_{IN} = 0 V, with respect to V_{REF}, R_L = 1400 Ω	–2		+2	V	
Voltage gain, K_R	R_L open, $K_R = \frac{V_{AB}}{V_{IN}}$ R_L = 1400 Ω, V_{IN} = 0.9 Vpk	95	100	105	V/V	1.
Ringing distortion	R_L = 1400 Ω, V_{IN} = 0.9 Vpk		0.5	3.5	%	

Specification	Condition	Min	Typ	Max	Unit	Note
Ringing current limit	R_L = 100 Ω	90	135	180	mApk	4.
Switching Power Supply						
CHCLK			85.3		kHz	3.
Chopper Clock Duty Cycle		7.5	10	12.5	%	3.
ILS_i Offset (current limit sense threshold)		0.25	0.28	0.31	V	3.
ILS_i	Input impedance		7000		Ω	
	Bias current	–1		+1	µA	
SD_i	Output impedance		50		Ω	
	Slew Rate negative	3			V/µsec	
	Slew Rate positive	25				
	V_{OH} where $V_{SW} \geq 12$ V, R_{BD} = 330 Ω		$V_{SW} - 0.3$ V	$V_{SW} - 0.2$ V	V	
	V_{OL} where $V_{SW} \geq 12$ V, R_{BD} = 330 Ω	$V_{SW} - 7.2$ V	$V_{SW} - 6.3$ V	$V_{SW} - 5.4$ V		
CHS_i	Input impedance		1		MΩ	
	Line test and Ringing			180	µA	
	Standby and Active			75		
	Disconnect			1		
FSET	Input impedance, tied to V_{REF}		10		Ω	
	Offset voltage with respect to V_{REF}	–5		+5	mV	
Power Supply Rejection Ratio at the Two-wire interface						
V_{CC} to V_{AB}	200 to 4000 Hz	25	45		dB	
	4 to 20 kHz, 50 mV_{RMS}	25	30			
V_{REG} to V_{AB}	200 to 4000 Hz, 100 mV_{RMS}	25	45			
	4 to 50 kHz	20	40			4.
	50 to 100 kHz	15	30			4.
Longitudinal Capability						
Longitudinal balance	R_L = 600 Ω, 300 to 3400 Hz, 0 dBm, Active and Reverse Polarity	46	63		dB	
T-L balance	1 kHz, 0 dBm	40	50			
Longitudinal current per pin	A(TIP) or B(RING)	30			mA	4.
Longitudinal impedance	A(TIP) or B(RING), 0 to 100 Hz		1	5	Ω/pin	4.
Longitudinal current detect, I_{LONG}	$\overline{\text{Fi}}$ Low, R_L from B(RING) to GND, Standby, Active, or Reverse Polarity	18	27	35	mA	
Transmission Performance						
2WRL	300 to 3400 Hz, for 600 Ω	26			dB	4.
K_{DC} DC current gain (IMT accuracy)	$K_{DC} = \frac{I_{IMT}}{I_{LOOP}}$, R_L = 600 Ω, Active, Standby, Reverse Polarity	$-\frac{1}{525}$	$-\frac{1}{500}$	$-\frac{1}{475}$	A/A	6.
K_V Voice Current gain	Line Test:, Standby $I_L < \|40$ mA| Active or Rev. Pol. $I_L < \|55$ mA| Ringing $I_L < \|90$ mA|	$\frac{1}{520}$	$\frac{1}{500}$	$\frac{1}{480}$	A/A	4.

Specification	Condition	Min	Typ	Max	Unit	Note
V_{IN} to V_{AB} (K_{IN})	R_L = open, 0dBm, two-wire	13.7	14	14.3	dB	
V_{OUT} to V_{AB} (K_{OUT})		9.34	9.54	9.74	dB	4.
Gain accuracy 4- to 2-Wire	0 dBm, 1 kHz	7.76	7.96	8.16	dB	
Gain accuracy 2- to 4-Wire	0 dBm, 1 kHz	–9.74	–9.54	–9.34	dB	
Gain accuracy 4- to 4-Wire	0 dBm, 1 kHz	–1.78	–1.58	–1.38	dB	
Gain accuracy over frequency	300 to 3400 Hz, Relative to 1 kHz	–0.1		+0.1	dB	
Gain tracking at 1kHz, relative to 0 dBm	–30 to +3 dBm, 2-Wire	–0.1		+0.1	dB	
	–55 to –30 dBm, 2-Wire	–0.1		+0.1	dB	4.
Gain tracking, On Hook, relative to 0 dBm	0 to –30 dBm, 2-wire	–0.15		+0.15	dB	4., 7.
	+3 to 0 dBm, 2-wire	–0.35		+0.35	dB	4., 7.
THD (Total Harmonic Distortion)	0 dBm, 2-wire, 1 kHz		–64	–50	dB	
	+7 dBm, 2-wire, 1 kHz		–55	–40	dB	
THD, On Hook	0 dBm, 2-wire, 1kHz			–36	dB	7.
Overload Level, 2-Wire	Active or Reverse Polarity, 1kHz	2.5			Vpk	2.
Idle Channel Noise	C-message		12	15	dBrnC	4.
Idle Channel Noise	Psophometric		-78	-75	dBmP	
$CFILT_i$	Output impedance		8000		Ω	3., 5.
	Drive capability, Active State	–150		+150	µA	3., 5.
VHP_i	Input impedance		5		Ω	3., 5.
	Offset voltage with respect to V_{REF}	–20		+20	mV	3., 5.
$VOUT_i$	Offset voltage with respect to V_{REF}	–40		+40	mV	
	Output impedance		1		Ω	3.
	Drive capability, R_L = 20 kΩ to V_{REF}	–50		+50	µA	3.
VIN_i	Input impedance	200			kΩ	3.
	Offset voltage voice	–20		+20	mV	3.
	Ringing and Line Test	–20		+20	mV	3.
VREF	Bias current	0		+200	µA	
Metering gain	R_L = 300 Ω, 12.0 kHz	4.45	4.70	4.95	dB	4.
	R_L = 300 Ω, 16.0 kHz					
Metering distortion, R_L = 300 Ω, V_{AB} = 1.5 Vpk	Frequency = 12 kHz		–55	–40	dB	4.
	Frequency = 16 kHz					
Crosstalk Between Channels						
Crosstalk coupling loss	F = 200 Hz to 3.4 kHz		–80	–75	dB	
Logic Interface						
Inputs (C1, C2, C3, CHCLK)						8.
V_{IL}				0.8	V	
V_{IH}		2.0			V	
I_{IL}	V_{IN} = 0.4 V	–150		+150	µA	
I_{IH}	V_{IN} = 2.4 V	–100		+100	µA	
Outputs (F)						
V_{OH}	I_{OUT} = –25 µA	2.4	2.8		V	
V_{OL}	I_{OUT} = 25 µA		0.2	0.4	V	

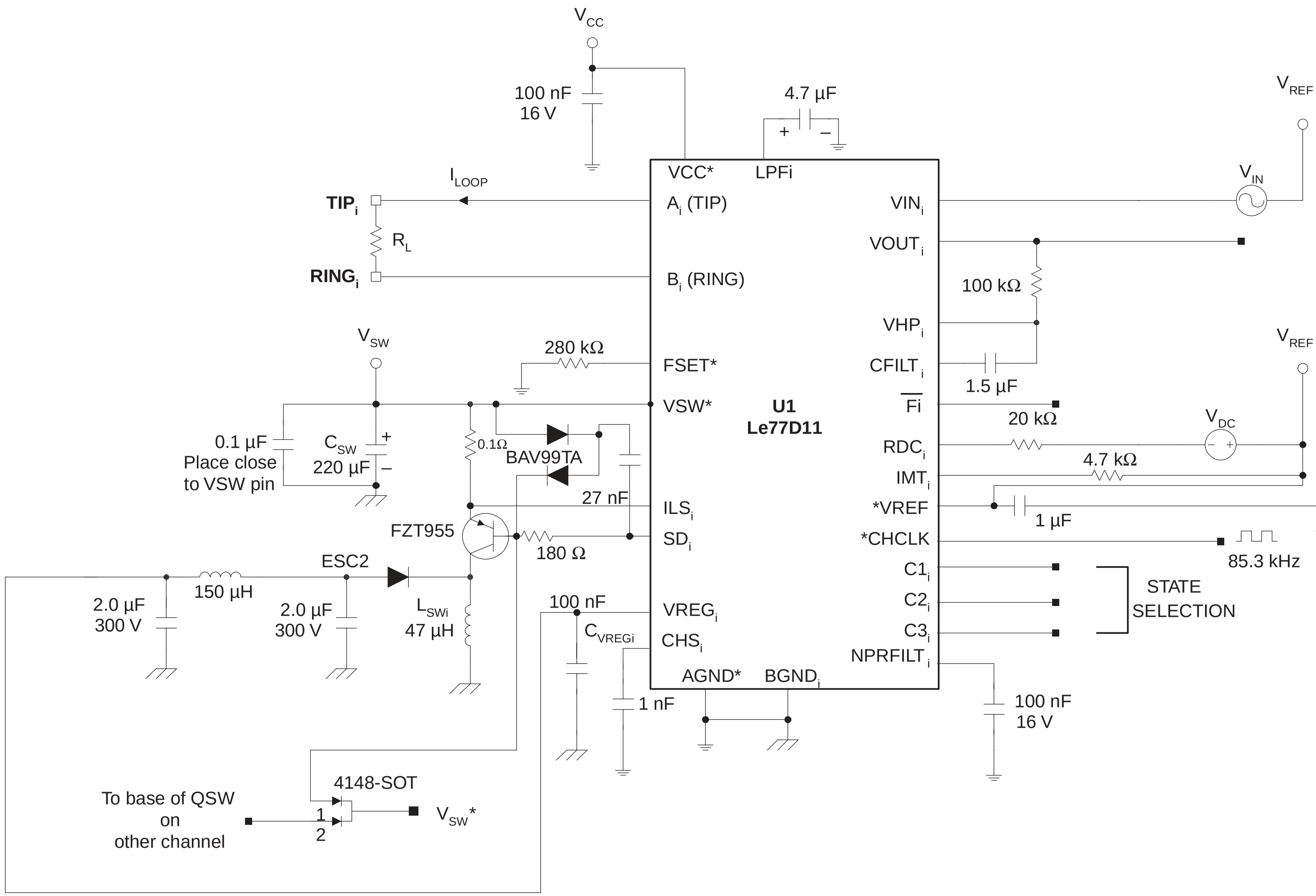
Specification	Condition	Min	Typ	Max	Unit	Note
IMT Pin Characteristics						
IMT_i	Output impedance		1		MΩ	3.
	Offset current, R_L = open, $V_{IMT} = V_{REF}$	–5		+5	μA	
	Output Range				μA	3.
	Ringing	–180		+180		
	Active and Reverse Polarity	–110		+110		
	Standby and Line Test	–80		+80		
Line Test |IMT| current limit	V_{IN} = 0.7V, R_L = 100 Ω with respect to V_{REF}	80		120	μA	
V_{IMT} Thermal Shutdown	I_{IMT} = 1mA	2.8			V	4.

Notes:

1. *V_{AB} = Voltage between the A_i (Tip) and B_i (Ring) pins.*
2. *Overload level is defined when THD = 1%.*
3. *Guaranteed by design.*
4. *Not tested in production. Parameter is guaranteed by characterization or correlation to other tests.*
5. *Layout should have less than 10 pF from pin to ground.*
6. *I_{IMT} = current coming out from IMT pin.*
7. *When On Hook, R_{LDC} is open circuit, R_{LAC} = 600 Ω.*
8. *C3 and C2 have pull-downs and C1 has pull-up to set the device state to Disconnect when the pins are floating.*

TEST CIRCUIT

Per Channel

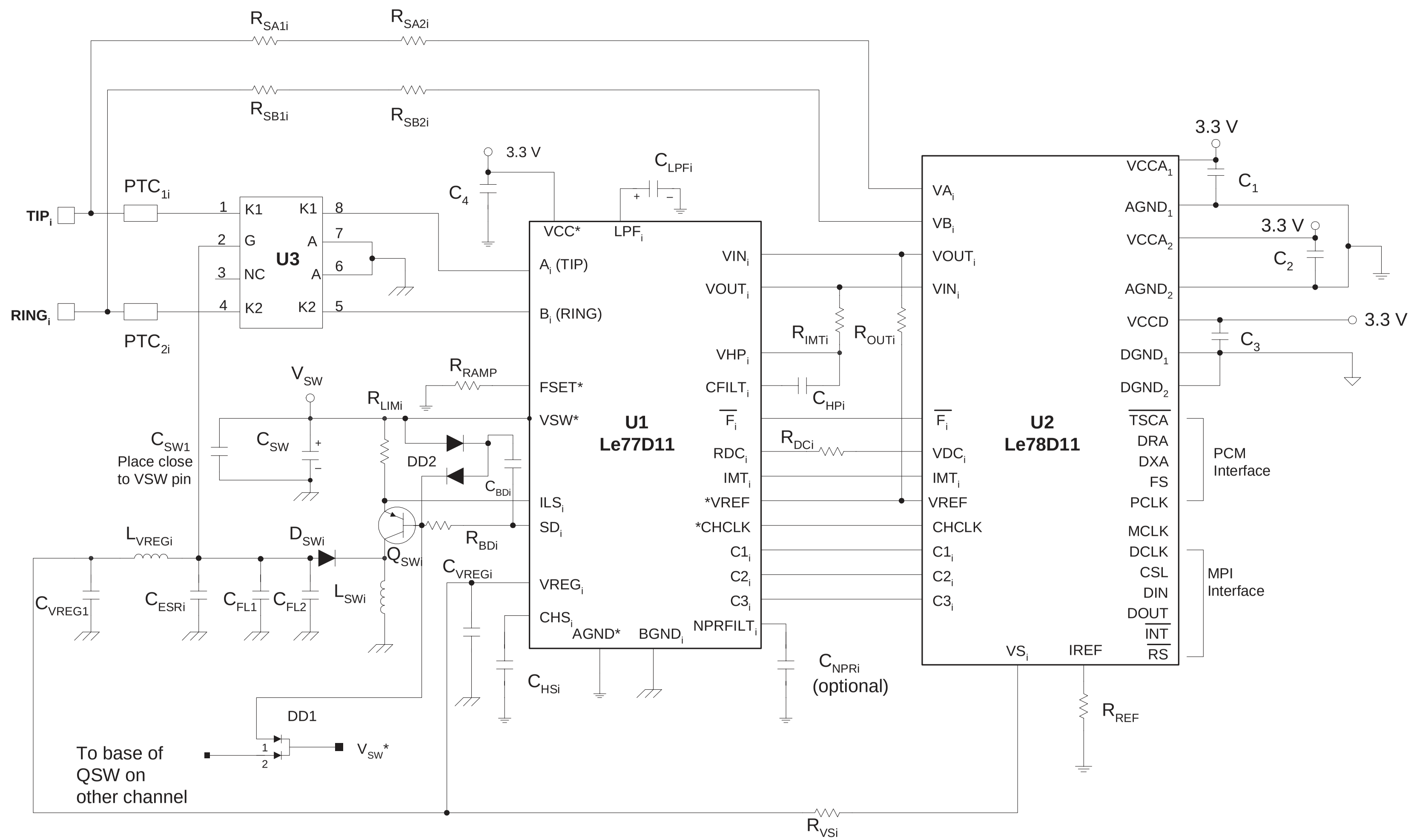


Note:

** denotes pins that are common to both channels.*

i = per channel component.

SINGLE CHANNEL APPLICATION CIRCUIT



Note:

** Denotes pins that are common to both channels.*

i = per channel component.

Protection is voltage tracking device.

C_{ESRi} is located close to gate on U3.

APPLICATION CIRCUIT PARTS LIST

The following list defines the parts and part values required to meet target specification limits for 90 Vpk ringing with V_{SW} = 12 V and CHCLK = 85.3 kHz for channel i of the line card (i = 1, 2). The protection circuit is not included.

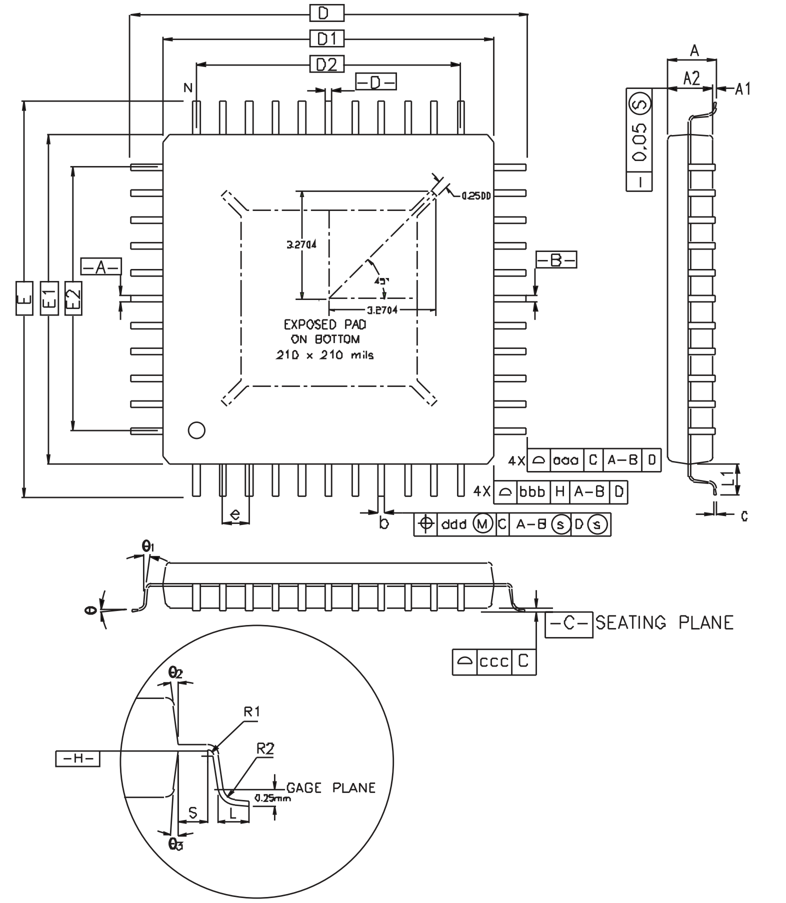
Item	Quantity (see note 1)	Type	Value	Tol.	Rating	Comments	Note
C_{HSi}	2	Capacitor	1 nF	10%	50 V	Panasonic / ECJ-1VB1H102K, 0603	
C_{BDi}	2	Capacitor	27 nF	10%	16 V	Kemet C0603C273K5RAC	
C_1, C_2, C_3, C_4	4	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VF1C104Z, 0603	
C_{ESRi}	2	Capacitor	0.1uF	10%	200 V	CalChip GMC31X7R104K200NT	
C_{NPRi}	2	Capacitor	100 nF	10%	16 V	Panasonic / ECJ-1VB1C104K (optional)	
C_{VREGi}	2	Capacitor	100 nF	10%	200 V	CalChip GMC31X7R104K200NT	
C_{HPi}	2	Capacitor	1.5 µF	10%	6.3 V	Panasonic / ECJ-2YB0J155K,0805	
C_{LPFi}	2	Capacitor	4.7 µF Tantalum	20%	6.3 V	Panasonic ECS-TOJY475R	
C_{FL1}, C_{FL2} C_{VREG1}	6	Capacitor	1.0 µF, ESR < 40 mΩ	10%	200 V	Tecate CMC-300/105KX1825T060	
C_{SW}	1	Capacitor	220 µF Alum. Elect.	20%	25 V	Nichicon / UPW1E221MPH	
C_{SW1}	1	Capacitor	100 nF	10%	50 V	DIGI-KEY / PCC1840CT-ND,0805	
D_{SWi}	2	Diode	ES2C		2 A	General Semi. / ES2C	
DD1	1	Diode	4148-SOT		600 mA	Fairchild / MMBD4148CC	
DD2, DD3	2	Diode	BAV99TA		250 mA	Zetex / BAV99TA (DIGI-KEY # BAV99ZXTR-ND)	
L_{SWi}	2	Inductor	47 µH		2.95 A	Cooper Coiltronics / DR127-470	
L_{VREGi}	2	Inductor	150 µH		205 mA	Coilcraft 1812LS154X_B	
PTC_{1i}, PTC_{2i}	4	PTC	50 Ω		250 V	AsiaCom / MZ2L-50R	
Q_{SWi}	2	PNP Transistor	FZT955		140 V	Zetex / FZT955	
R_{LIMi}	2	Resistor	0.1 Ω,	5%	1/4 W	Panasonic ERJ-14RSJR10U / DIGI-KEY P10SCT-ND	
R_{BDi}	2	Resistor	180 Ω	1%	1/4 W	Panasonic ERJ-6ENF1820V	
R_{DCi}	2	Resistor	20 K	1%	1/16 W	Panasonic / ERJ-3EKF2002V	
R_{REF}	1	Resistor	69.8 K	1%	1/16 W	Panasonic / ERJ-3EKF6982V	
R_{IMTi}	2	Resistor	100 K	1%	1/16 W	Panasonic / ERJ-3EKF1003V	
R_{RAMP}	1	Resistor	280 K	1%	1/16 W	Panasonic / ERJ-3EKF2803V	
R_{VSi}	2	Resistor	475 K	1%	1/16 W	Panasonic / ERJ-3EKF4753V	
R_{SA1i}, R_{SB1i}, R_{SA2i}, R_{SB2i}	8	Resistor	237 k	1%	1/8 W	Panasonic / ERJ-8ENF2373V	
R_{OUTi}	2	Resistor	10 k	1%	1/16 W	Panasonic / ERJ-3KF1002V	
$U3_i$	2	Protector				Bourns / TISP61089BDR	

Note:

1. Quantities required for a complete two-channel solution.

PHYSICAL DIMENSIONS

44-Pin eTQFP



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D	12 BSC		
D1	10 BSC		
E	12 BSC		
E1	10 BSC		
R2	0.08	-	0.20
R1	0.08	-	-
Θ	0 deg	3.5 deg	7 deg
Θ 1	0 deg	-	-
Θ 2	11 deg	12 deg	13 deg
Θ 3	11 deg	12 deg	13 deg

Symbol	Min	Nom	Max
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	-	-
b	0.17	0.20	0.27
e	0.80 BSC		
D2	8.00		
E2	8.00		
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
N	44		

Notes:
1. Controlling dimension in millimeter unless otherwise specified.
2. Dimensions “D1” and “E1” do not include mold protrusion. Allowable protrusion is 0.25mm per side.
   “D1” and “E1” are maximum plastic body size dimensions including mold mismatch.
3. Dimension “b” does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08mm.
4. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
5. Square dotted line is E-Pad outline.
6. “N” is the total number of terminals.

44-Pin eTQFP

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision B1 to C1

- In *Pin Descriptions*, FSET pin, removed reference to 256 kHz operation
- In *Absolute Maximum Ratings*, the following changes were made:
  - Changed T_A from 22.7° to 32°C/W
  - Changed maximum power dissipation from 2.6 to 1.8 W
  - Added another note describing eTQFP package
- In *Supply Currents and Power Dissipation*, Ringing operation state, removed condition V_{IN} = 0.7 V_{DC}
- In *System Specifications*, first paragraph, removed T_A = 0 to 70°C
- Updated Physical Dimensions drawing

Revision C1 to D1

- Made updates pertaining to 90 Vpk throughout document

Revision D1 to E1

- In *Device Specifications*, I_{LSi} Offset, changed min. from .27 to .25 and max from .29 to .31
- Made updates to *Application Circuit Parts List*, including:
  - Increased voltage ratings on capacitors C_{ESRi}, C_{VREGi}, C_{FLi} and C_{VREG1}
  - Changed value of C_{FLi} and C_{VREG1} to 1 μF

Revision E1 to F1

- Modified application circuit and BOM to reflect addition of the TISP61089BDR protector

Revision F1 to G1

- Added green package OPN to *Ordering Information*, on page 1
- Added *Package Assembly*, on page 12
- Updated DC specifications to Vreg, Isc, IMTi and Metering Gain based on Errata notice April 29 2004 revision A1 for device version JCBB.
- Included operational issues 3.0 from errata notice April 29, 2004.

Revision G1 to G2

- Enhanced format of package drawing in *Physical Dimensions*, on page 21
- Added new headers/footers due to Zarlink purchase of Legerity on August 3, 2007

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