

UG511: Si5348-D Evaluation Board User's Guide

The Si5348-D-EVB is used for evaluating the Si5348 Network Synchronizer Clock for SyncE/1588 and Stratum 3/3E applications. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5348-D-EB" in the lower left-hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. In this document, the terms are synonymous in context.) The Si5348 contains three independent DSPLLs in a single IC with programmable jitter attenuation bandwidth on a per DSPLL basis. The Si5348-D-EVB supports three independent differential input clocks, two independent CMOS input clocks, and seven independent output clocks via onboard SMA connectors. The Si5348-D-EVB can be controlled and configured via a USB connection to a host PC running Skyworks' next generation ClockBuilder® Pro (CBPro) software tool. Test points are provided on-board for external monitoring of supply voltages.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5348-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.

EVB FEATURES

- Powered from USB port or external +5 V power supply via screw terminals
- Included SiOCXO1-EB reference OCXO board allows for evaluation in standalone and holdover mode.
- CBPro GUI programmable VDD supply allows device supply voltages from 3.3, 2.5, or 1.8 V
- CBPro GUI programmable V_{DDO} supplies allow each of the seven outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI allows control and measurement of voltage, current, and power of VDD and all 8 VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5348
- SMA connectors for input clocks, output clocks and optional external timing reference clock



UG511: Si5348-D Evaluation Board User's Guide • Si5348-D-EVB Functional Block Diagram, Support Documentation, and ClockBuilderPro Software

1. Si5348-D-EVB Functional Block Diagram, Support Documentation, and ClockBuilderPro Software

Below is a functional block diagram of the Si5348-D-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults for more information.

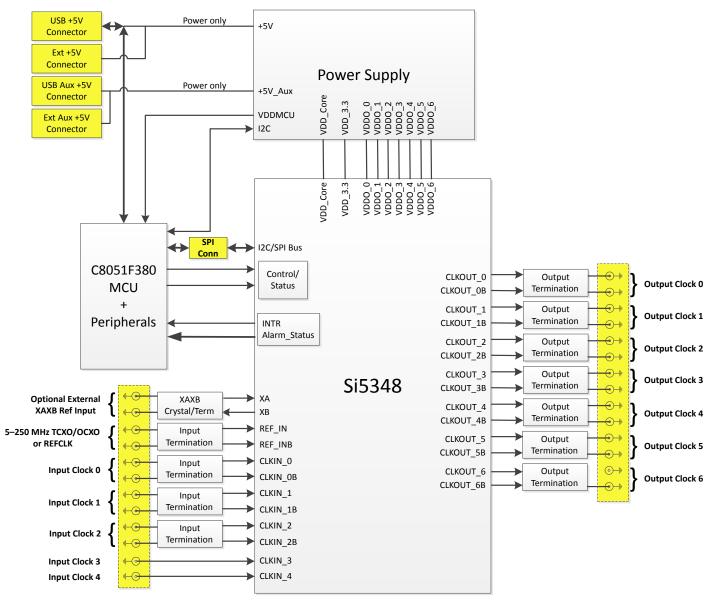


Figure 1.1. Si5348-D-EVB Functional Block Diagram

All Si5348 schematics, BOMs, User's Guides, and software can be found online at the following link: https://www.skywork-sinc.com/search?q=Si5348#documents

The SiOCXO1-EB User's Guide is located at: https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/user-guides/UG123.pdf

UG511: Si5348-D Evaluation Board User's Guide • Quick Start and Jumper Defaults

2. Quick Start and Jumper Defaults

- 1. Install ClockBuilder Pro desktop software from EVB support web page given in Section 2.
- 2. Connect USB cable from Si5348-D-EVB to PC with ClockBuilder Pro software installed.
- 3. Connect the SIOCXO1-EB to the reference input using the included SMA cable.
- 4. Confirm jumpers are installed as shown in the table below.
- 5. Launch the ClockBuilder Pro Software.

6. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5348-D-EVB.

Table 2.1. Si5348-D EVB Jumper Defaults*

Location	Туре	I = Installed O = Open	Location	Туре	I = Installed O = Open
JP1	2 pin	I	JP23	2 pin	0
JP2	2 pin	I	JP24	2 pin	0
JP3	2 pin	I	JP25	2 pin	0
JP4	2 pin	I	JP26	2 pin	0
JP5	2 pin	0	JP27	2 pin	0
JP6	2 pin	0	JP28	2 pin	0
JP7	2 pin	I	JP29	2 pin	0
JP8	2 pin	0	JP30	2 pin	0
JP9	2 pin	0	JP31	2 pin	0
JP10	2 pin	I	JP32	2 pin	0
JP13	2 pin	0	JP33	2 pin	0
JP14	2 pin	I	JP34	2 pin	0
JP15	3 pin	1 to 2	JP35	2 pin	0
JP16	3 pin	1 to 2	JP36	2 pin	0
JP17	2 pin	0	JP38	3 pin	All open
JP18	2 pin	0	JP39	2 pin	0
JP19	2 pin	0	JP40	2 pin	0
JP20	2 pin	0	JP41	2 pin	0
JP21	2 pin	0			
JP22	2 pin	0	J36	5x2 Hdr	All 5 installed

3. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD Core voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy
D5	LOL_T0B	Blue	Loss of Lock - DSPLL C
D6	LOL_T4B	Blue	Loss of Lock - DSPLL D
D8	LOS2B	Blue	Loss of Signal at IN2
D11	INTRB	Blue	Si5348 Interrupt Active
D12	LOS1B	Blue	Loss of Signal at IN1
D13	LOL_AB	Blue	Loss of Lock DSPLL A
D14	LOS0B	Blue	Loss of Signal at IN0

Table 3.1. Si5348-D EVB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5348-D-EVB +3.3 V, and Si5348 VDD or supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. LEDs D14, D12, and D8 indicate loss of signal at clock inputs IN0, IN1, and IN2, respectively. LEDs D13, D5, and D6 indicate loss of lock for one of three internal DSPLLs (A, C, and D) respectively. D11 indicates Si5348 interrupt output is active (as configured by Si5348 register programming). LED locations are highlighted below with LED function name indicated on board silkscreen.

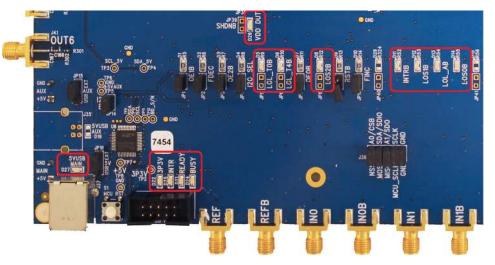


Figure 3.1. Si5348-D-EVB LED Locations

UG511: Si5348-D Evaluation Board User's Guide • External Reference Input (XA/XB)

4. External Reference Input (XA/XB)

An external timing reference (48 MHz XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5348-D-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with an external REFCLK, C111 and C113 must be populated and XTAL Y1 removed (see figure below). The REFCLK can then be applied to SMA connectors J39 and J40.

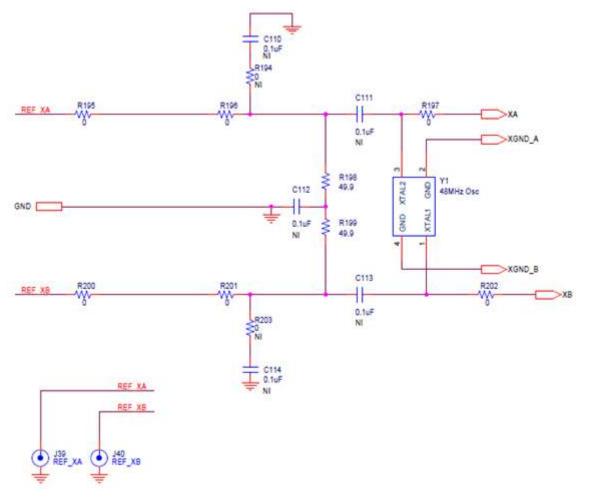


Figure 4.1. External Reference Input Circuit

UG511: Si5348-D Evaluation Board User's Guide • Clock Input and Output Circuits

5. Clock Input and Output Circuits

5.1 Clock Input Circuits (REF/REFB, IN0/IN0B-IN2/IN2B, IN3, IN4)

The Si5348-D-EVB has eight SMA connectors (REF/REFB, IN0/IN0B–IN2/IN2B) for receiving external differential clock signals. The REF/REFB differential input clock is intended to support a TCXO or OCXO, such as the included SiOCXO1-EB, which determines the Si5348's wander performance. (Please note that this input clock is different from the optional reference clock that may be applied at XA/XB.) All differential input clocks are terminated as shown in the figure below. The only exception is that the terminating 49.9 Ω resistor for REF is not installed. This is R84 corresponding to IN0's R76 in the figure below. The reason for this exception is that single-ended TCXOs and OCXOs typically cannot drive a 50 Ω load. Note that input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5348 data sheet.

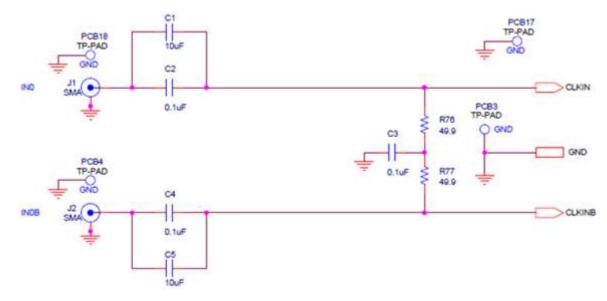


Figure 5.1. Differential Input Clock Termination Circuit

In addition, the Si5348-D-EVB supports two SMA connectors (IN3, IN4) for receiving external single-ended LVCMOS clocks. Each of these clocks connects to its respective Si5348 pins via a single installed 0 Ω resistor. There are no other termination components on the EVB.

UG511: Si5348-D Evaluation Board User's Guide • Clock Input and Output Circuits

5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the 14 output drivers (seven differential pairs, OUT0/OUT0B—OUT6/OUT6B) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. In particular, if differential pair OUT6/OUT6B is configured for 1 Hz output, then the AC coupling output capacitors, C166 and C168, each need to be replaced by a 0 Ω resistor. (These capacitors are the respective counterparts of the OUT0/OUT0B output capacitors, C25 and C27, in the figure below.) The Si5348-D-EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5348-D-EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

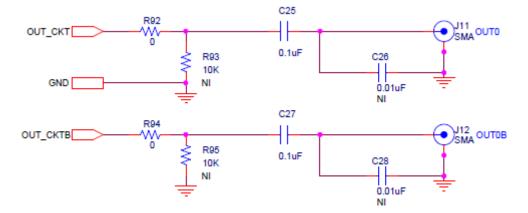


Figure 5.2. Output Clock Termination Circuit

6. Using the Si5348-D-EVB and Installing ClockBuilder Pro Desktop Software

6.1 Installing ClockBuilderPro Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder can be found at the download link shown above. Please follow the instructions as indicated.

6.2 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown below.

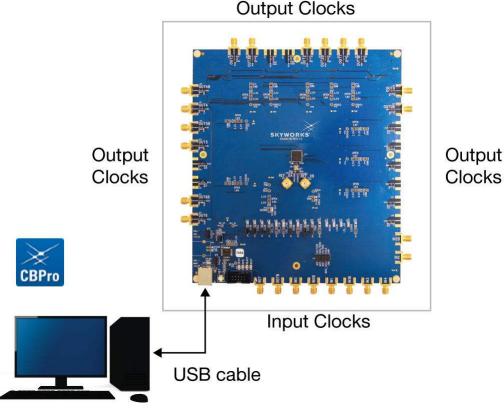


Figure 6.1. EVB Connection Diagram

6.3 Additional Power Supplies

The Si5348-EB comes pre-configured with jumpers installed at JP15 and JP16 (pins 1–2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
 - · Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
 - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

Errata Note: The Si5348-EB REV 1.0 silkscreen at jumpers JP15-16 is reversed, i.e. the "USB" and "EXT" text are incorrectly swapped. Normal operation from USB only is still with jumpers installed between pins 1–2. This is on the right-hand side as viewed, reading the silkscreen choices.

6.4 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilder Pro installer will install two main applications:

CB ClockBuilder Pro Wizard - Skyworks	- 🗆 X
 ClockBuilder Pro Wizard We Make Timing Simple 	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
🖶 <u>Open Project</u>	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation <u>10/40/100G Line Card Whitepaper</u>
ex Open Sample Project	<u>Clock Generators for Cloud Data Centers</u> Optimizing Si534x Jitter Performance
Evaluation Board Detected Si5348A Rev D EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements ClockBuilder Pro Documentation
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes
۵.	Version 4.1 Built on 9/22/2021

Figure 6.2. Application #1: Clockbuilder Pro Wizard

Use the CBPro Wizard to:

- · Create a new design
- · Review or edit an existing design
- · Export: create in-system programming files

Info DUT SPI	DUT Settings I	Editor DUT Register Editor	Regulators All	Voltages GPIO	Status Registers	*	Control Registers
		27	Current	Power	na 19 19		Soft Reset and Calibratio
VD	5 1.001	Voltage					SOFT_RST_ALL
VDE		On V	A	W	Read		SOFT_RST_PLLA
VDD/		On V	A	W	Read		SOFT_RST_PLLB
VDDS	S 3.30V	On V	A	W	Read		
VDDO	0 1.80V	On 1.789 V	0 mA	0 mW	Read		SOFT_RST_PLLC
VDDO	1.80V	0n 1.791 V	0 mA	0 mW	Read		SOFT_RST_PLLD
VDDO		On 1.788 V	0 mA	0 mW	Read		Hard Reset, Sync, & Power I
VDDO		On 1.799 V	0 mA	0 mW	Read		HARD_RST
	197						SYNC
VDDO4	10 is	On 1.798 V	0 mA	0 mW	Read		PDN: 0
VDDO5	1.80V	On 1.790 V	0 mA	0 mW	Read		PDN.
VDDO	6 1.80V	On 1.794 V	0 mA	0 mW	Read		Frequency Adjust
	P	Total	0 mA	0 W	Read All		FINC
All Output Supplies	Select Volt	tage	\$ may				FDEC
og Filtered	Auto Scroll: Or	n 💽 Insert Marker	Clear Copy	y to Clipboard	Pause		
Filtered		n 💽 Insert Marker	Clear Copy	y to Clipboard	Pause		
Filtered	ource Me			y to Clipboard	Pause		
Filtered Timestamp Sc 12:38:51.060 EV	ource Mes VB Pau	ssage	JX hold	y to Clipboard	Pause		
Filtered Filter	ource Mes VB Pau VB Star	ssage using 70 msec for voltage ML	JX hold 25=10)	y to Clipboard	Pause		
Filtered Timestamp Sc 12:38:51.060 EV 12:38:51.140 EV 12:38:51.151 EV	ource Mes VB Pau VB Star VB Fini	ssage using 70 msec for voltage ML rting Read_ADC(num_sample	JX hold es=10) es=10) => 381.3		Pause		
Filtered Filter	Ource Mes VB Pau VB Star VB Fini VB Fini	ssage ising 70 msec for voltage ML rting Read_ADC(num_sample ished Read_ADC(num_sample	JX hold 25=10) es=10) => 381.3 nel=VDD_4_PIN) :		Pause		
Filtered Image: Comparison of the system Second of the system 12:38:51.060 EV 12:38:51.140 EV 12:38:51.151 EV 12:38:51.151 EV 12:38:51.152 EV	ource Mes VB Pau VB Star VB Finit VB Finit VB Star	ssage using 70 msec for voltage ML rting Read_ADC(num_sample ished Read_ADC(num_sample ished Measure_Voltage(chan	JX hold es=10) es=10) => 381.3 nel=VDD_4_PIN) : s=0x090E)	=> 1.804	Pause		

Figure 6.3. Application #2: EVB GUI

Use the EVB GUI to:

- · Download configuration to EVB's DUT (Si5348)
- · Control the EVB's regulators
- · Monitor voltage, current, and power on the EVB

6.5 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5348-D EVB. These workflow scenarios are:

- · Workflow Scenario #1: Testing a Skyworks-Created Default Configuration
- · Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

6.6 Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 6.4. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

CB Clock	Builder Pro Wizard - Skyworks
0 ()	ClockBuilder Pro Wizard We Make Timing Simple
Work	c With a Design
Cò	Create New Project
	Open Project
3	Convert Existing Project/NVM File
ex	<u>Open Sample Project</u>
SHILL SE	Evaluation Board Detected Si5348A Rev D EVB Open Default Plan EVB GUI

Figure 6.5. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

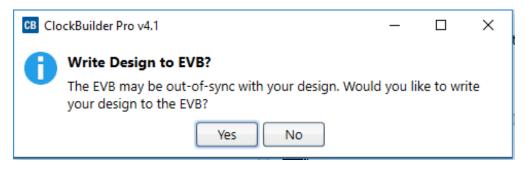


Figure 6.6. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5348 device mounted on your EVB. This ensures the device is completely reconfigured per the Skyworks default plan for the DUT type mounted on the EVB.

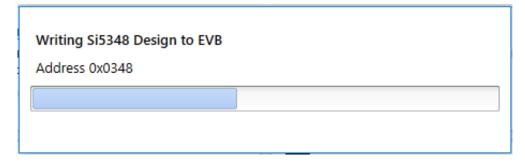


Figure 6.7. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.

CB Si5348 EVB Default Configuration - ClockBuilder Pro		1	200 00		×
ClockBuilder Pro v4.1 🌣 (standard frequency planner)	(no setting overrides)	SKY	wo	R	<s'< th=""></s'<>
Design Dashboard 🔻		Configuring S	i5348	AB F	Rev D
EVB sample plan for Si5348 has been loaded. You can make edits Edit Configuration with Wizard Design ID & Notes · Revision · Host Interface · XAXB & REF · Free Run · Inputs · Input Clock Select · Outputs · DCO · DSPLL · LOS · OOF · LOL · INTR	to the EVB's configuration using the Evaluation Board E Si5348A Rev D EVB Write Design to EVB	Detected	iui		

Figure 6.8. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the nominal values defined in the device's default CBPro project file created by Skyworks, as shown in the example session window below.

DUT SPI	DUT Settings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Register
		Voltage	Curren	t Powe	er	
VDD	1.80V	Dn 1.779 V	153 r	nA 272	mW [Read
VDDA	3.30V	Dn 3.305 V	121 r	nA 400	mW [Read
VDDS	3.30V 📱 🚺	Dn 3.283 V	14 r	nA <mark>4</mark> 6	mW [Read
VDD00	1.80V 📘 🚺	Dn 1.790 V	0 r	nA 0	mW [Read
VDDO1	1.80V 🔽 🔽	Dn 1.789 V	0 r	nA 0	mW [Read
VDDO2	1.80V 📘 🚺	Dn 1.791 V	0 r	mA 0	mW [Read
VDDO3	1.80V 🔽 🕻	Dn 1.798 V	0 r	nA 0	mW [Read
VDDO4	1.80V 📳 🔽	Dn 1.798 V	0 r	nA 0	mW [Read
VDDO5	1.80V 🔽 🔽	Dn 1.787 V	0 r	nA 0	mW [Read
VDDO6	1.80V 🔽 🔽	Dn 1.793 V	0 r	mA 0	mW [Read
All Output	- Select Voltage	Total	288 r	mA 0.718	w [Read All

Figure 6.9. EVB GUI Window

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6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Skyworks-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":

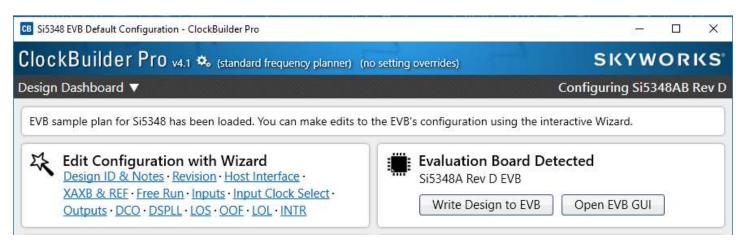


Figure 6.10. Write Design to EVB

Failure to do the step above will cause the device to read in a preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

sign Dashboard 🔻	Configuring Si5348AB Re
EVB sample plan for Si5348 has been loaded. You can make edits to th	e EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Design ID & Notes · Revision · Host Interface · XAXB & REF · Free Run · Inputs · Input Clock Select · Outputs · DCO · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5348A Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time. In engineering mode, you can <u>save this project</u> <u>unencrypted</u> .	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Si5348 Rev D Reference Manual Si5348 Rev D Datasheet Si5348 Rev D EVB User's Guide
Skyworks Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance

Figure 6.11. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

B Si5348 Desig	п кероп		_		×
Design Report	2				
Device Grade	Output Clock Frequency Range	Typical Jitter			A
Si5348A Si5348B*	100 Hz to 718.5 MHz 100 Hz to 350 MHz	< 150 fs			
sufficient (higher fre selecting of	for your design. For m equencies and/or to ena device grade Si5348A wh	ncy plan, a Si5348B grade device is ore in-system configuration flexibility ple fractional synthesis), consider en specifying an ordering part number (OPN) asheet Ordering Guide for more information.			
Design					
SPI Mode	er Supply: VDD (Core) 2: 4-Wire	d / 0x6C to 0x6F (selected via A0/A1 pins)			
XA/XB:	C33 Nange, 1000 to 111	, one to one (serected via Rover prins)			
	XTAL - Crystal)				
REF: 12.8 MH: DSPLL B	5				
D9 IN1: 10 S1 D9 IN2: 15 S1	andard SPLL A,C,D MHz andard SPLL A,C,D 66.25 MHz andard SPLL A,C,D ussed				
Outputs:					
OUTØ: 10 Er) MHz mabled, LVDS 2.5 V GPLL C				
OUT1: 15 Er	6.25 MHz mabled, LVDS 2.5 V GPLL D				
OUT2: 19 Er	66.25 MHz mabled, LVDS 2.5 V GPLL A				
	25 MHz mabled, LVDS 2.5 V GPLL D				
OUT4: 25					
OUT5: 25 Er	6 MHz mabled, <mark>LV</mark> DS 2.5 V				
OUT6: 1	Hz Hz				v
	board Save Report	Ask for Help		Clo	1

Figure 6.12. Design Report Window

6.6.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

6.7 Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on any of the underlined fields below the header "Edit Configuration with Wizard". You can also pull down on the "Design Dashboard" menu and select a design step.

CB Si5348 EVB Default Configuration - ClockBuilder Pro	– 🗆 X
ClockBuilder Pro v4.1 🎭 (standard frequency planner) (no	setting overrides) SKYWORKS
Design Dashboard 🔻	Configuring Si5348AB Rev D
EVB sample plan for Si5348 has been loaded. You can make edits to the	he EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Design ID & Notes · Revision · Host Interface · XAXB & REF · Free Run · Inputs · Input Clock Select · Outputs · DCO · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5348A Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time. In engineering mode, you can <u>save this project</u> <u>unencrypted</u> .	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation <u>Si5348 Rev D Reference Manual</u> <u>Si5348 Rev D Datasheet</u> <u>Si5348 Rev D EVB User's Guide</u>
Skyworks Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click <u>here</u> to get assistance.
Frequency Plan Valid O Design OK Typical Pd 1.16 W, Tj 45	C Home Close

Figure 6.13. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

itep 1 of 14 - Design ID & Notes Configuring Si5348AE Design ID The device has 8 registers, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/revision identifier. Design ID: 5348EVB4 (optional; max 8 characters) The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_ID7. Padding Mode: Image: NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x00 bytes (aka NUI character). Omage: Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x20 bytes (space character). Design Notes Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet addent. While the text is word wrapped in reports, you can use newlines to start a new paragraph. Image: Start and Start		er Pro v4.1 🍫 (standard frequency planner) (no setting overrides)	SKYW	OR	KS
The device has 8 registers, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/revision identifier. Design ID: 5348EVB4 (optional; max 8 characters) The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_ID7. Padding Mode: NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x00 bytes (aka NUI character). Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x20 bytes (space character). Design Notes Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet addence			onfiguring Si534	18AB	Rev
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If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded with 0x20 bytes (space character). Design Notes Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet adden	Padding Mode:	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded	with 0x00 bytes (aka	a NULL	
Enter anything you want here. The text is stored in your project file and included in design reports and custom part number datasheet adden		If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padded	with 0x20 bytes (spa	ace	
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Figure 6.14. Design ID and Notes

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on "Write to EVB" to update the DUT to reconfigure your device in real time. The Design Write status window will appear each time you make a change.

CB Si5348 Design	Write	
Writing Si534 Address 0x00	18 Design to EVB B6	

Figure 6.15. Writing Design Status

6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting "Open Design Project File".

CB ClockBuilder Pro Wizard - Skyworks	- D X
 ClockBuilder Pro Wizard We Make Timing Simple 	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
Dpen Project	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation <u>10/40/100G Line Card Whitepaper</u>
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance
Si5348 EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements
	ClockBuilder Pro Documentation
	<u>CBPro Overview</u> <u>CBPro Tools & Support for In-System Programming</u> <u>CLI User's Guide</u> <u>Release Notes</u>
۰.	Version 4.1 Built on 9/22/2021

Figure 6.16. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file) in the Windows file browser.

→ ∵ ↑ <mark>.</mark> «	Jui_Tharwal > User_Guide_Images_Rebranding	> Si5348 ∨ Č	Search Si5348		Q
rganize 🔻 🛛 New f			8	= • 🔳	(
 Documents Downloads Pictures 	Name Si5348-RevD-5348EVB4-Project	Date modified 11/12/2021 12:44	Type Skyworks Timing	Size 13 KB	
Fil	le name:		 Skyworks Timing 	a Proiect	3

Figure 6.17. Browse to Project File

Select "Yes" when the WRITE DESIGN to EVB popup appears:

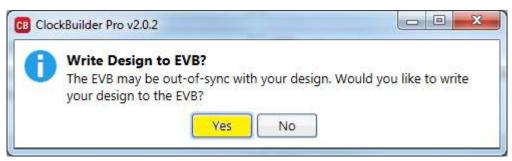


Figure 6.18. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

CB Si5348 EVB Default Configuration - ClockBuilder Pro	- 🗆 X
ClockBuilder Pro v4.1 🎭 (standard frequency planner) (no	setting overrides) SKYWORKS
Design Dashboard 🔻	Configuring Si5348AB Rev D
EVB sample plan for Si5348 has been loaded. You can make edits to t	he EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Design ID & Notes · Revision · Host Interface · XAXB & REF · Free Run · Inputs · Input Clock Select · Outputs · DCO · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5348A Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Please contact your Silicon Labs representive for documentation regarding this pre-release device.
Create Custom Part Number With just a few clicks, you can order factory pre- programmed devices based on your configuration.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid O Design OK O Pd: 1.162 W, Tj: 95 °C	Home Close
	· Devictor Mar File

Figure 6.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

ntroduction	Register File	Settings File	Multi-Project Register/Settings	Regmap	
configuratio A command	will contain the	f this tool is av	need to be written to the Si5	20	
Options					
Export Type					
Each	Contraction of the second s	/alues (CSV) Fil s an address,d	le ata pair in hexadecimal forma	t. A comma sepa	arates the address
used Include If check	directly in firm summary head ed, an informa by the # chara	ware code. ler tional header v	ressed in C code via an array c will be included at the top of t der will contain some basic inf	he <mark>file.</mark> Each line	in the header will be
Certain This ens the dow	control registe ures the devic	e is stable durii	egister writes tten before and after writing t ng configuration download ar urn inclusion of this sequence	id resumes norn	nal operation after
🗌 I am tar	geting pre-pro	oduction sampl	les 🔞		

Figure 6.20. Export Settings

UG511: Si5348-D Evaluation Board User's Guide • Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

7. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP is **NOT** the same as writing a configuration into the Si5348 using ClockBuilder Pro on the Si5348-D EVB). Writing a configuration into the EVB from ClockBuilderPro is done using Si5348 RAM space and can be done a virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP

UG511: Si5348-D Evaluation Board User's Guide • Serial Device Communications (Si53848 <-> MCU)

8. Serial Device Communications (Si53848 <-> MCU)

8.1 On-Board SPI Support

The MCU onboard the Si5348-D-EVB communicates with the Si5348 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5348 device is the SPI slave. The Si5348 device can also support a 2-wire I²C serial interface, although the Si5348-D-EVB does NOT support the I²C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I²C.

8.2 External I²C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5348 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5348 device. The shunt at J4 (I2C_SEL) must also be removed to select I²C as Si5348 interface type. An external I²C controller connected to the Si5348 side of J36 can then communicate to the Si5348 device. (For more information on I²C signal protocol, please refer to the Si5348 data sheet.)

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5348 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I²C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I²C SDA and J36 pin 8 (DUT_SCLK) as the I²C SCLK. Please note the external I²C controller will need to supply its own I²C signal pull-up resistors.

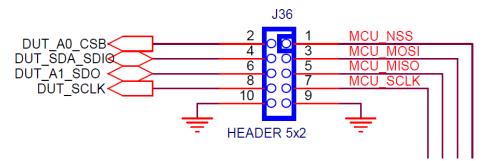


Figure 8.1. Serial Communications Header J36

UG511: Si5348-D Evaluation Board User's Guide • Si5348-D-EVB Schematic and Bill of Materials (BOM)

9. Si5348-D-EVB Schematic and Bill of Materials (BOM)

The Si5348-D-EVB Schematic and Bill of Materials (BOM) can be found online at:

https://www.skyworksinc.com/search?q=Si5348#documents

Note: Please be aware that the Si5348-D-EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

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