CDx4HC(T)541 High-Speed CMOS Logic Octal Buffer and Line Drivers Three-State

1 Features

- 'HC540, CD74HCT540: inverting
- 'HC541, 'HCT541: non-inverting
- Buffered inputs
- Three-state outputs
- Bus line driving capability
- Typical propagation delay = 9 ns at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: –55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility, V_{IL} = 0.8 V (max), V_{IH} = 2 V (min)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

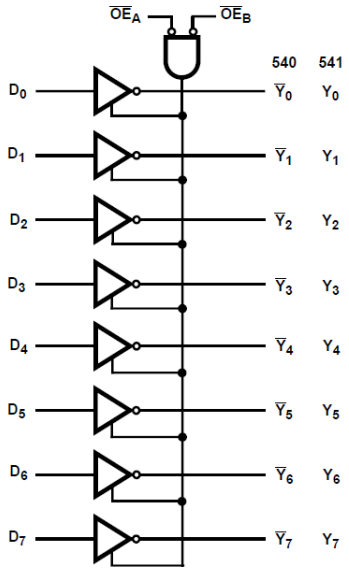
2 Description

The 'HC540 and CD74HCT540 are Inverting Octal Buffers and Line Drivers with Three-State Outputs and the capability to drive 15 LSTTL loads. The 'HC541 and 'HCT541 are Noninverting Octal Buffers and Line Drivers with Three-State Outputs that can drive 15 LSTTL loads. The Output Enables ($\overline{OE1}$) and ($\overline{OE2}$) control the Three-State Outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is HIGH the outputs will be in the high impedance state. For data output $\overline{OE1}$ and $\overline{OE2}$ both must be LOW.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD74HC540M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC540E	PDIP (20)	25.40 mm × 6.35 mm
CD54HC540F3A	CDIP (20)	26.92 mm × 6.92 mm
CD74HC541M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC541E	PDIP (20)	25.40 mm × 6.35 mm
CD54HC541F	CDIP (20)	26.92 mm × 6.92 mm
CD74HCT540M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT540E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT541M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT541E	PDIP (20)	25.40 mm × 6.35 mm
CD54HCT541F	CDIP (20)	26.92 mm × 6.92 mm
CD74HCT541PW	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram

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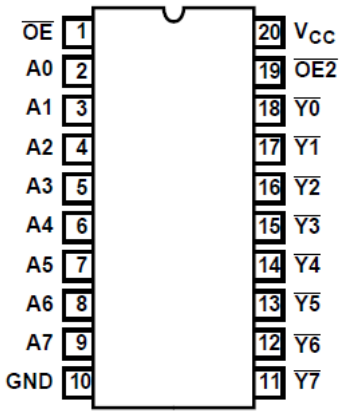
3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

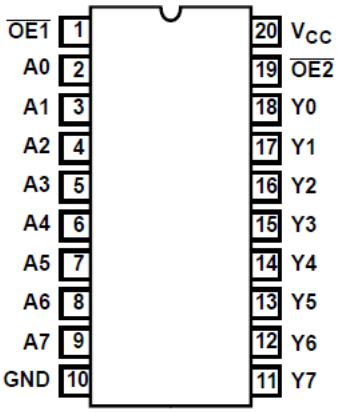
Changes from Revision D (January 2022) to Revision E (October 2022)	Page
• Increased RθJA for packages: DW (58 to 109.1); N (69 to 84.6); PW (83 to 131.8)	4

Changes from Revision C (July 2004) to Revision D (January 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-refrences throughout the document to reflect modern data sheet standards	1

4 Pin Configuration and Functions



HC540
J, N, or DW package
20- Pin CDIP, PDIP, or SOIC
Top View



HC541
J, N, DW, or PW
20-Pin CDIP, PDIP, SOIC, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output diode current	For $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Drain current, per output	For $–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V		±35	mA
I_O	Output source or sink current per output pin	For $V_O > –0.5$ V or $V_O < V_{CC} + 0.5$ V		±25	mA
	Continuous current through V_{CC} or ground current			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
T_A	Temperature range		–55	125	℃
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	N (PDIP) 20 PINS	PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	84.6	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	82.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	21.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	65.2	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[2]	V_{CC}(V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 µA	2			0.1		0.1		0.1	V
		I_{OL} = 20 µA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 µA	6			0.1		0.1		0.1	
	Low level output voltage TTL loads	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	6			8		80		160	µA
I_{OZ}	Three-state leakage current	V_O = V_{CC} or GND	6			±0.5		±5.0		±10	µA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage CMOS loads	V_{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	V_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage CMOS loads	V_{OL} = 20 µA	4.5			0.1		0.1		0.1	V
	Low level output voltage TTL loads	V_{OL} = 6 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} and GND	5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_I = V_{CC} and GND	5.5			8		80		160	µA
I_{OZ}	Three-state leakage current	V_O = V_{CC} or GND	5.5			±0.5		±5.0		±10	µA

5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS[2]	V_{CC}(V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC} [1]	HCT540 Additional quiescent device current per input pin	A0 - A7 inputs held at V_{CC}–2.1	4.5 to 5.5		100	360		450		490	µA
		$\overline{OE2}$ input held at V_{CC}–2.1	4.5 to 5.5		100	270		337.5		367.5	µA
		$\overline{OE1}$ input held at V_{CC}–2.1	4.5 to 5.5		100	414		517.5		563.5	µA
	HCT541 Additional quiescent device current per input pin	A0 - A7 inputs held at V_{CC}–2.1	4.5 to 5.5		100	144		180		196	µA
		$\overline{OE2}$ input held at V_{CC}–2.1	4.5 to 5.5		100	270		337.5		367.5	µA
		$\overline{OE1}$ input held at V_{CC}–2.1	4.5 to 5.5		100	414		517.5		563.5	µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8mA.
(2) $V_I = V_{IH}$ or V_{OL}, unless otherwise noted.

5.5 Switching Characteristics

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay Data to outputs (540)	C_L = 50 pF	2			110		140		165	ns
			4.5			22		28		33	
		C_L = 15 pF	5		9						ns
		C_L = 50 pF	6			19		24		28	
t_{PLZ}, t_{PHZ}	Data to outputs (541)	C_L = 50 pF	2			115		145		175	ns
			4.5			23		29		35	
		C_L = 15 pF	5		9						ns
		C_L = 50 pF	6			20		25		30	
t_{PLZ}, t_{PHZ}	Output enable and disable to outputs (540)	C_L = 50 pF	2			160		200		240	ns
			4.5			32		40		48	
		C_L = 15 pF	5		13						ns
		C_L = 50 pF	6			27		34		41	
t_{PLZ}, t_{PHZ}	Output enable and disable to outputs (541)	C_L = 50 pF	2			160		200		240	ns
			4.5			32		40		48	
		C_L = 15 pF	5		14						ns
		C_L = 50 pF	6			23		29		35	
t_{THL}, t_{TLH}	Output transition time	C_L = 50 pF	2			60		75		90	ns
			4.5			12		15		18	
			6			10		13		15	
C_I	Input capacitance	C_L = 50 pF		10		10		10		10	pF
C_O	Three-state output capacitance			20		20		20		20	pF
C_{PD}	Power dissipation capacitance[1] [2] (540)	C_L = 15 pF	5		50						pF
C_{PD}	Power dissipation capacitance[1] [2] (541)	C_L = 15 pF	5		48						pF
HCT TYPES											
t_{PHL}, t_{PLH}	Propagation delay Data to outputs (540)	C_L = 50 pF	4.5			24		30		36	ns
		C_L = 15 pF	5		9						

5.5 Switching Characteristics (continued)

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PHL}, t_{PLH}	Data to outputs (541)	C_L = 50 pF	4.5			28		35		42	ns
		C_L = 15 pF	5		11						
t_{PLZ}, t_{PHZ}	Output enable and disable to outputs (540, 541)	C_L = 50 pF	4.5			35		44		53	ns
		C_L = 15 pF	5		14						
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5			12		15		18	ns
C_I	Input capacitance	C_L = 50 pF		10		10		10		10	pF
C_O	Three-state output capacitance			20		20		20		20	pF
C_{PD}	Power dissipation capacitance(1) (2) (540, 541)	C_L = 15 pF	5		55						pF

(1) C_{PD} is used to determine the dynamic power consumption, per channel.
(2) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

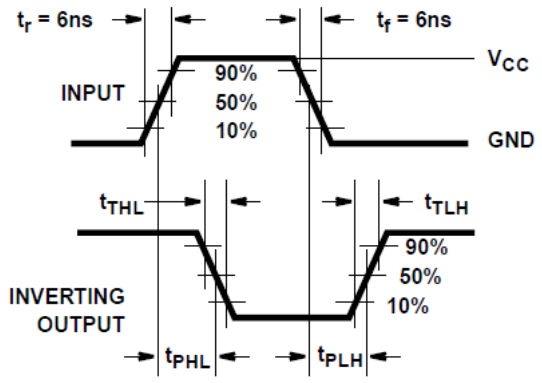


Figure 6-1. HC Transition Times and Propagation Delay Times, Combination Logic

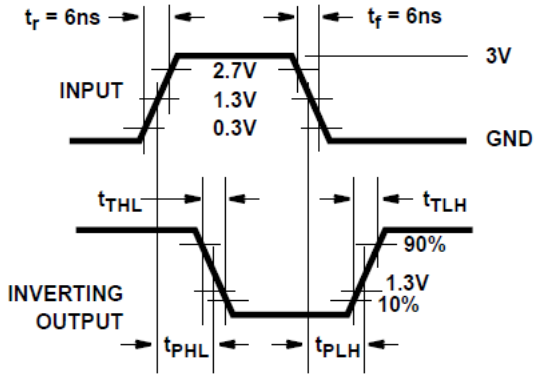


Figure 6-2. HCT Transition Times and Propagation Delay Times, combination Logic

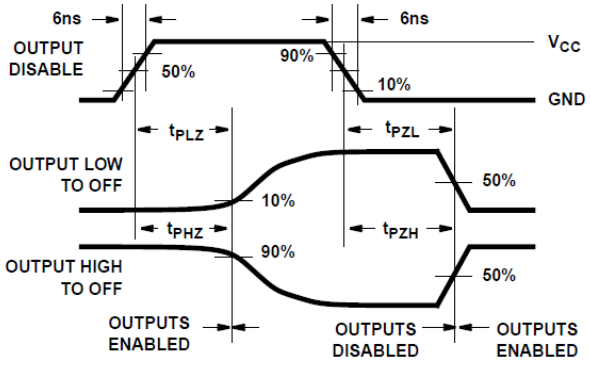


Figure 6-3. HC Three-State Propagation Delay Waveform

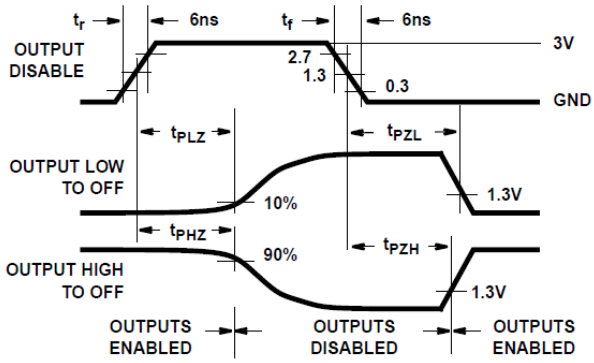
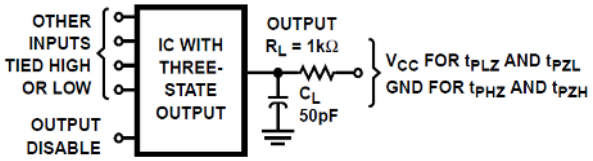


Figure 6-4. HCT Three-State Propagation Delay Waveform



A. Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50 pF.

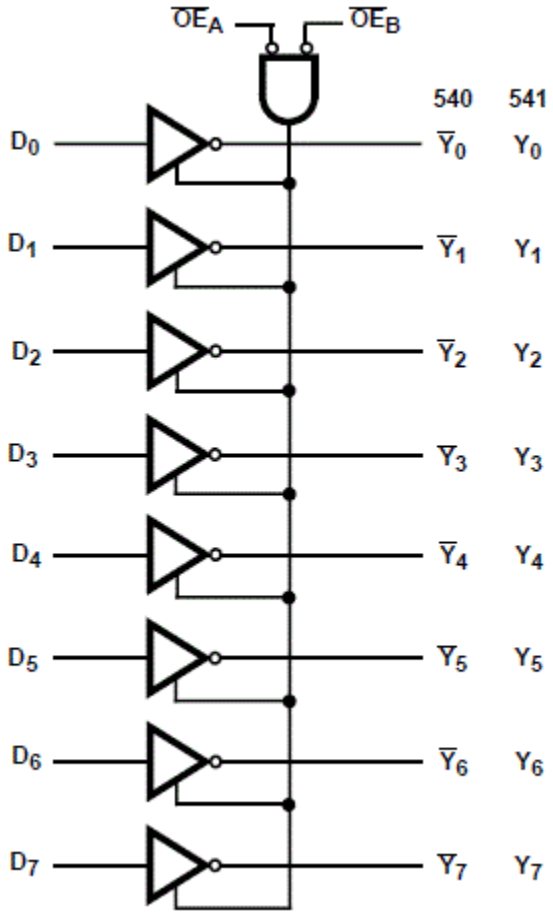
Figure 6-5. HC and HCT Three-State Propagation Delay Test Circuit

7 Detailed Description

7.1 Overview

The ’HC540 and CD74HCT540 are Inverting Octal Buffers and Line Drivers with Three-State Outputs and the capability to drive 15 LSTTL loads. The ’HC541 and ’HCT541 are Noninverting Octal Buffers and Line Drivers with Three-State Outputs that can drive 15 LSTTL loads. The Output Enables ($\overline{OE1}$) and ($\overline{OE2}$) control the Three-State Outputs. If either $\overline{OE1}$ or $\overline{OE2}$ is HIGH the outputs will be in the high impedance state. For data output $\overline{OE1}$ and $\overline{OE2}$ both must be LOW.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table(1)

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	An	540	541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

(1) H = high voltage level, L = low voltage level, X= don’t care, Z = high impedance

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC540F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC540F3A	Samples
CD54HC541F	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC541F	Samples
CD54HC541F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC541F3A	Samples
CD54HCT541F	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT541F	Samples
CD54HCT541F3A	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT541F3A	Samples
CD74HC540E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC540E	Samples
CD74HC540M	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC540M	
CD74HC540M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC540M	Samples
CD74HC541E	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC541E	Samples
CD74HC541EE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC541E	Samples
CD74HC541M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC541M	Samples
CD74HC541M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC541M	Samples
CD74HC541PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ541	Samples
CD74HCT540E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT540E	Samples
CD74HCT540M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT540M	Samples
CD74HCT541E	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT541E	Samples
CD74HCT541M96	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT541M	Samples
CD74HCT541M96E4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT541M	Samples
CD74HCT541M96G4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT541M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC540, CD54HC541, CD54HCT541, CD74HC540, CD74HC541, CD74HCT541 :

- Catalog : CD74HC540, CD74HC541, CD74HCT541

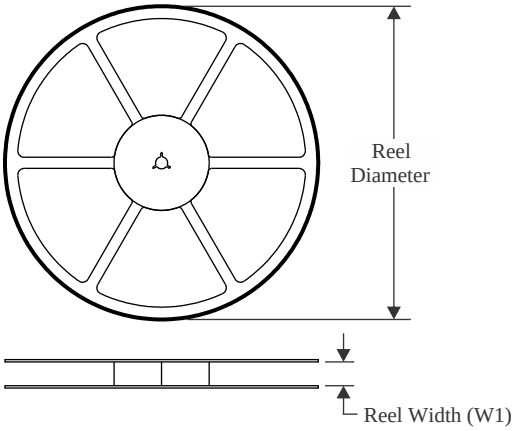
- Military : CD54HC540, CD54HC541, CD54HCT541

NOTE: Qualified Version Definitions:

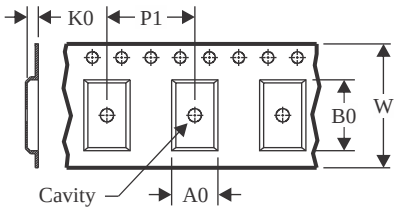
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

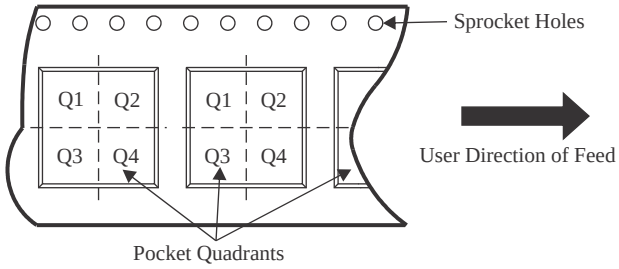


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

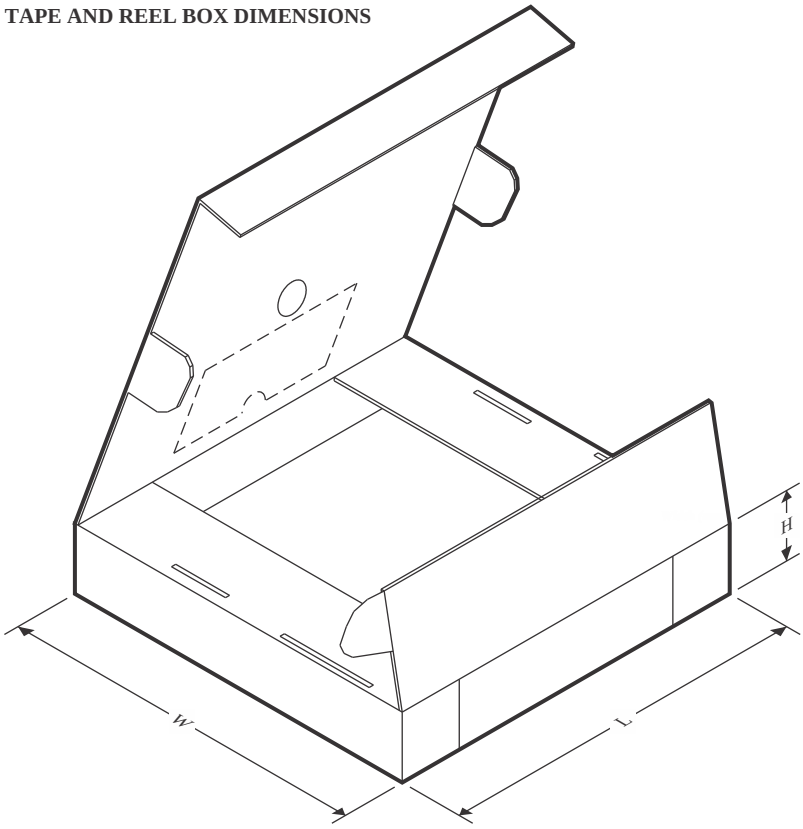
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC540M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC541M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CD74HC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CD74HCT540M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT540M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT541M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

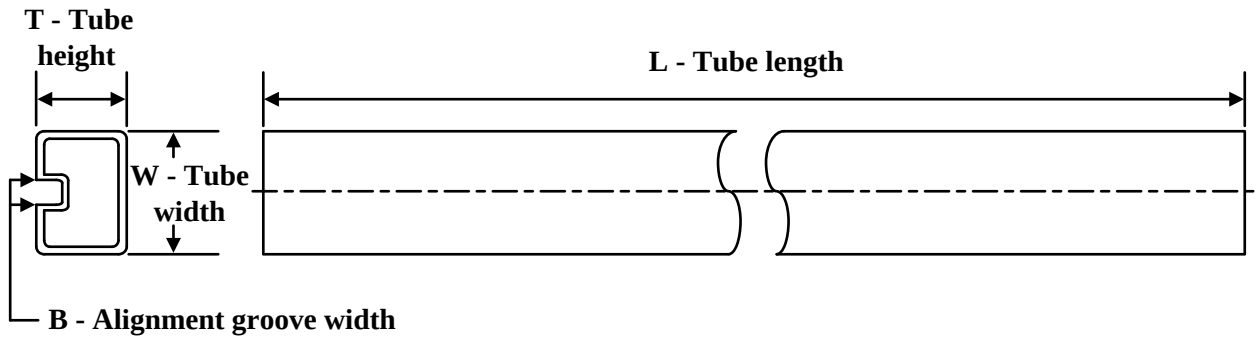
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC540M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC541M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC541M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74HC541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
CD74HCT540M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT540M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HCT541M96	SOIC	DW	20	2000	356.0	356.0	41.0
CD74HCT541M96	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



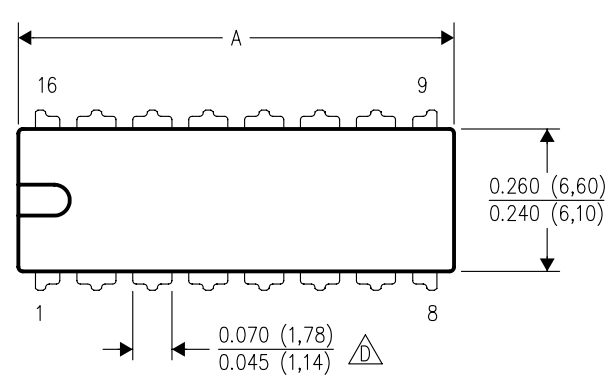
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC540E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC540M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HC541E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC541EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT540E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT541E	N	PDIP	20	20	506	13.97	11230	4.32

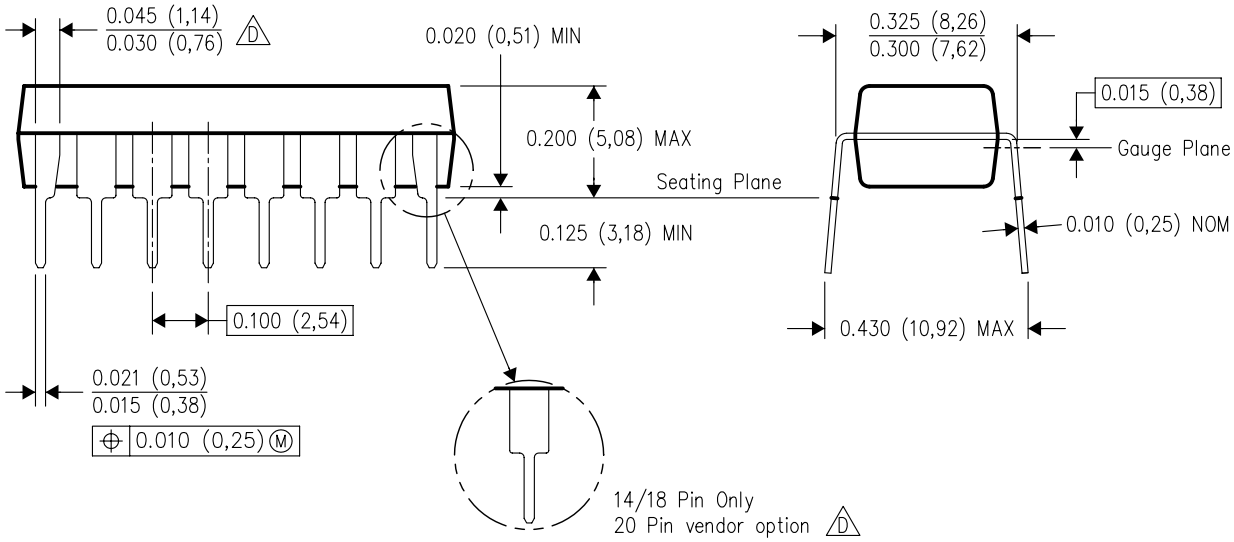
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

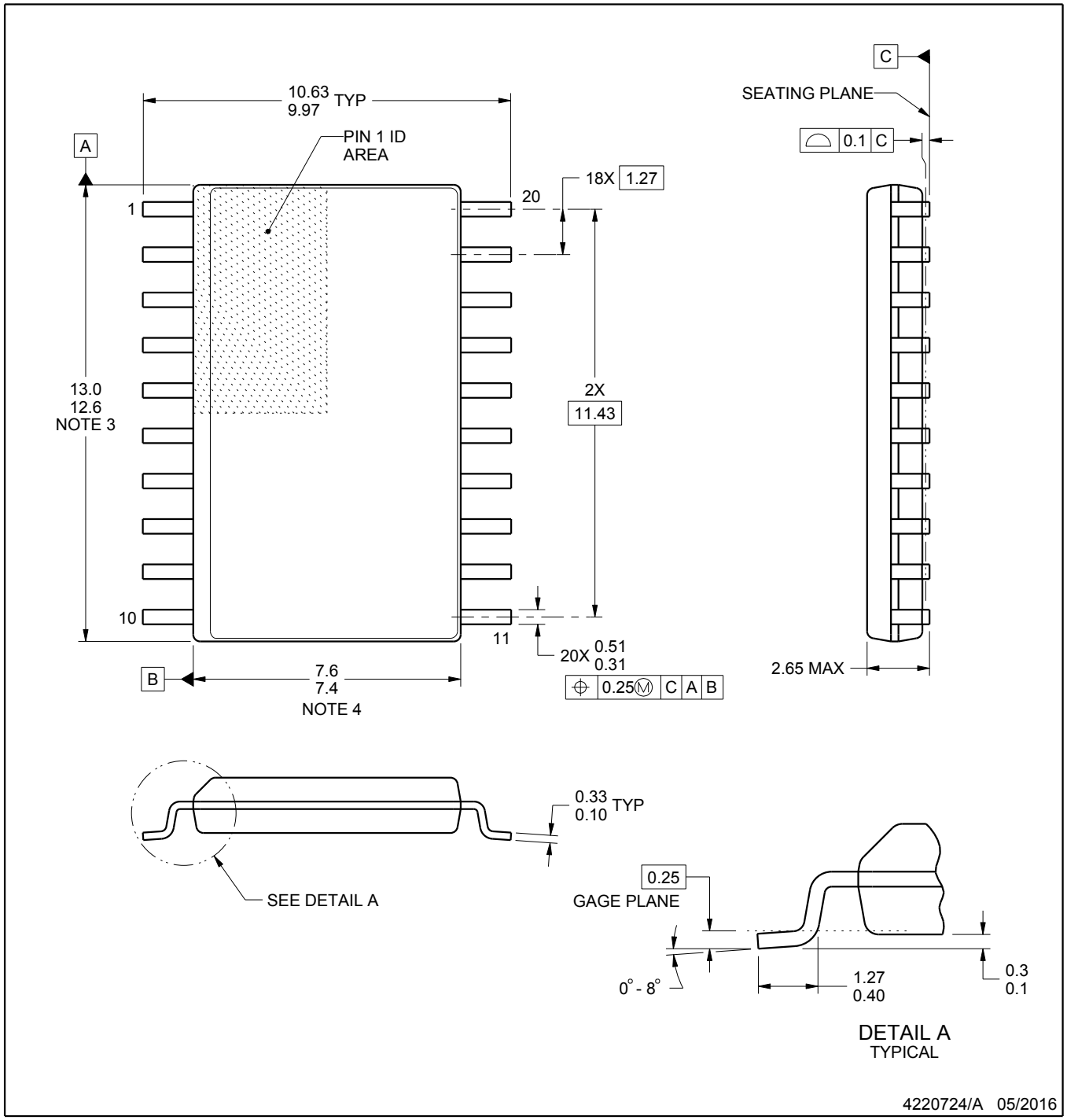
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

DW0020A

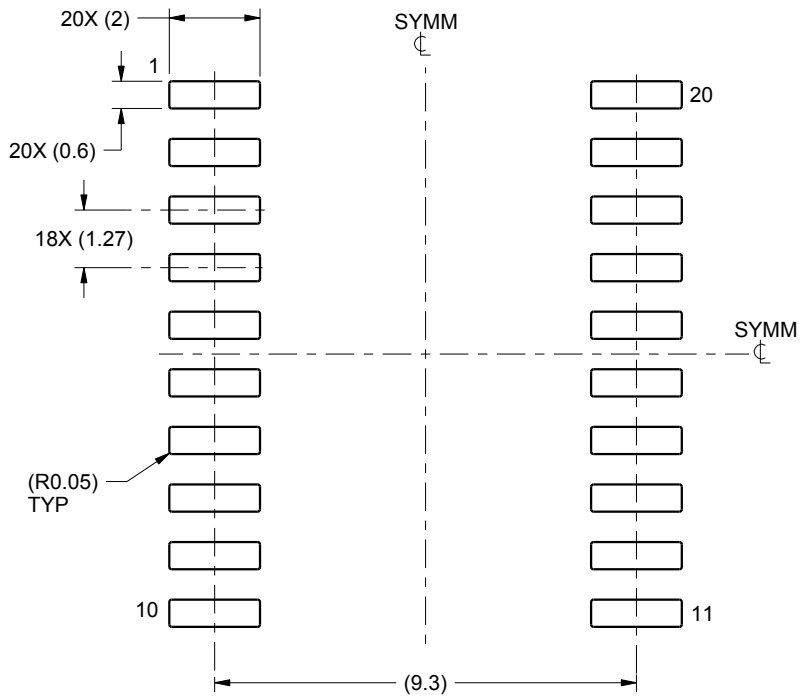
SOIC - 2.65 mm max height

SOIC

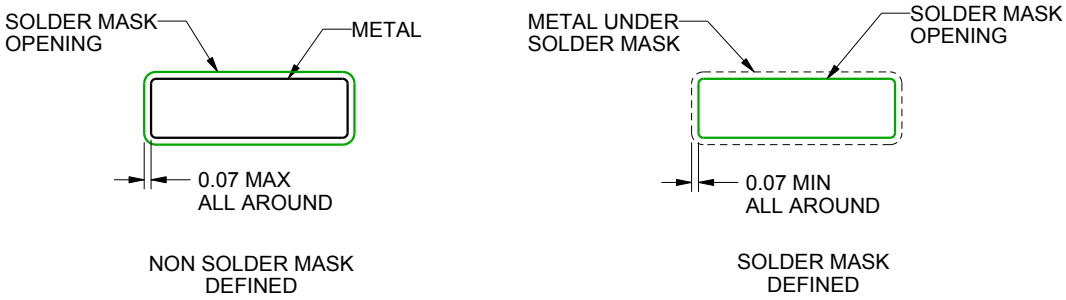


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

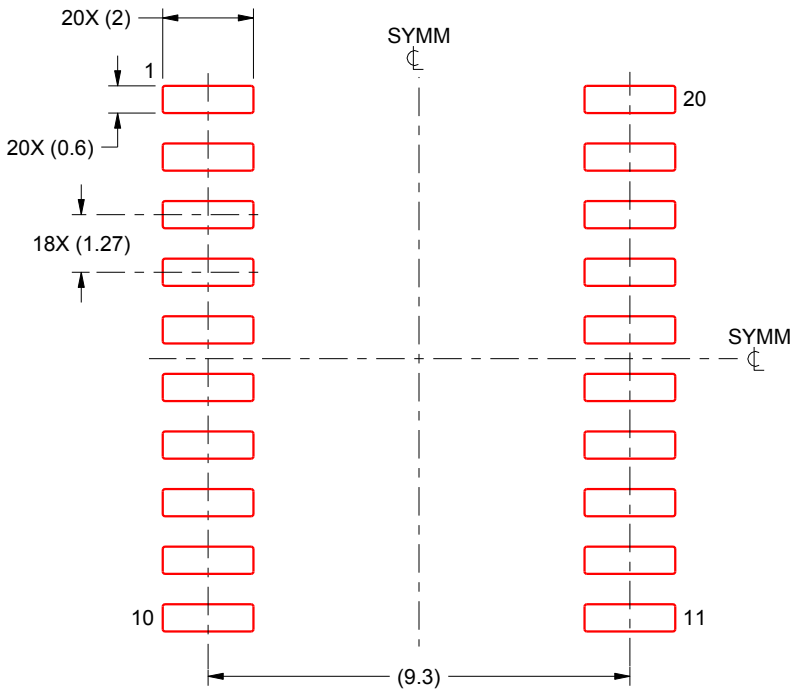


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

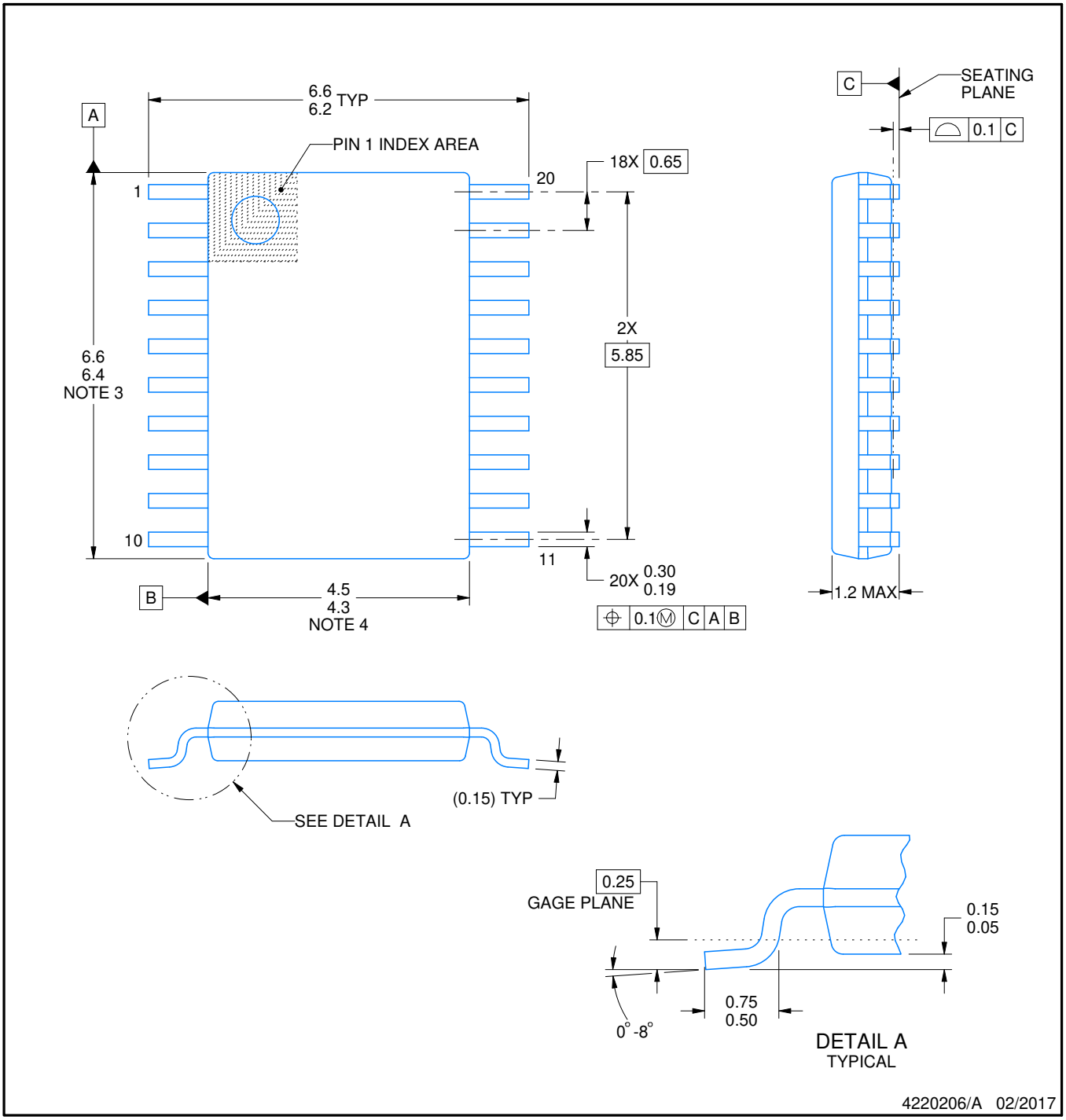
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

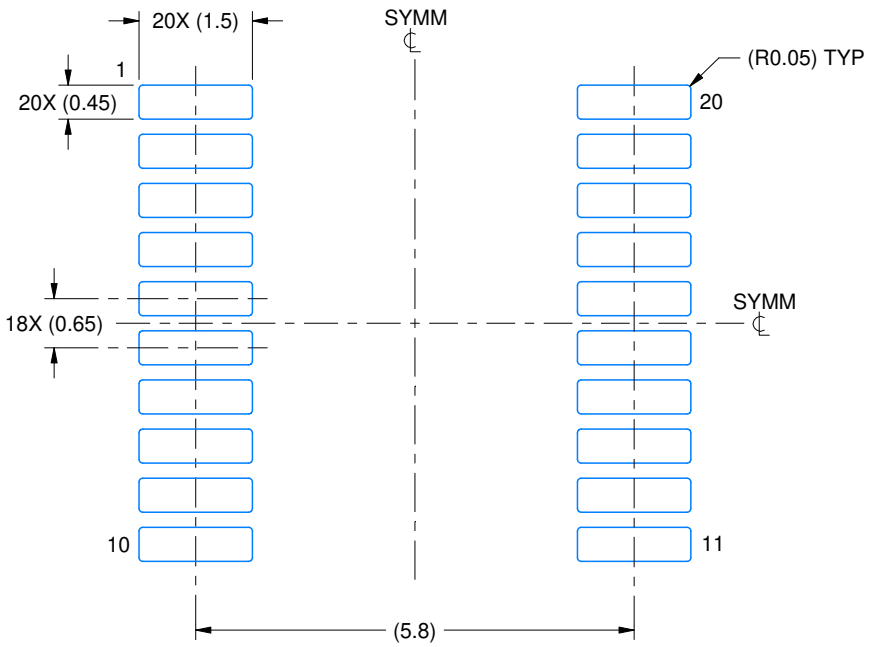
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



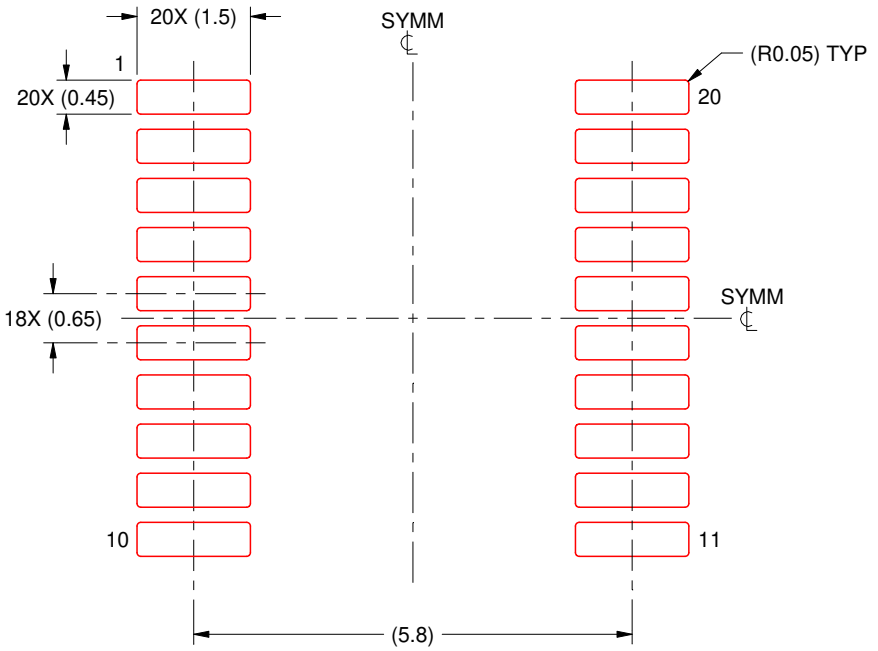
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



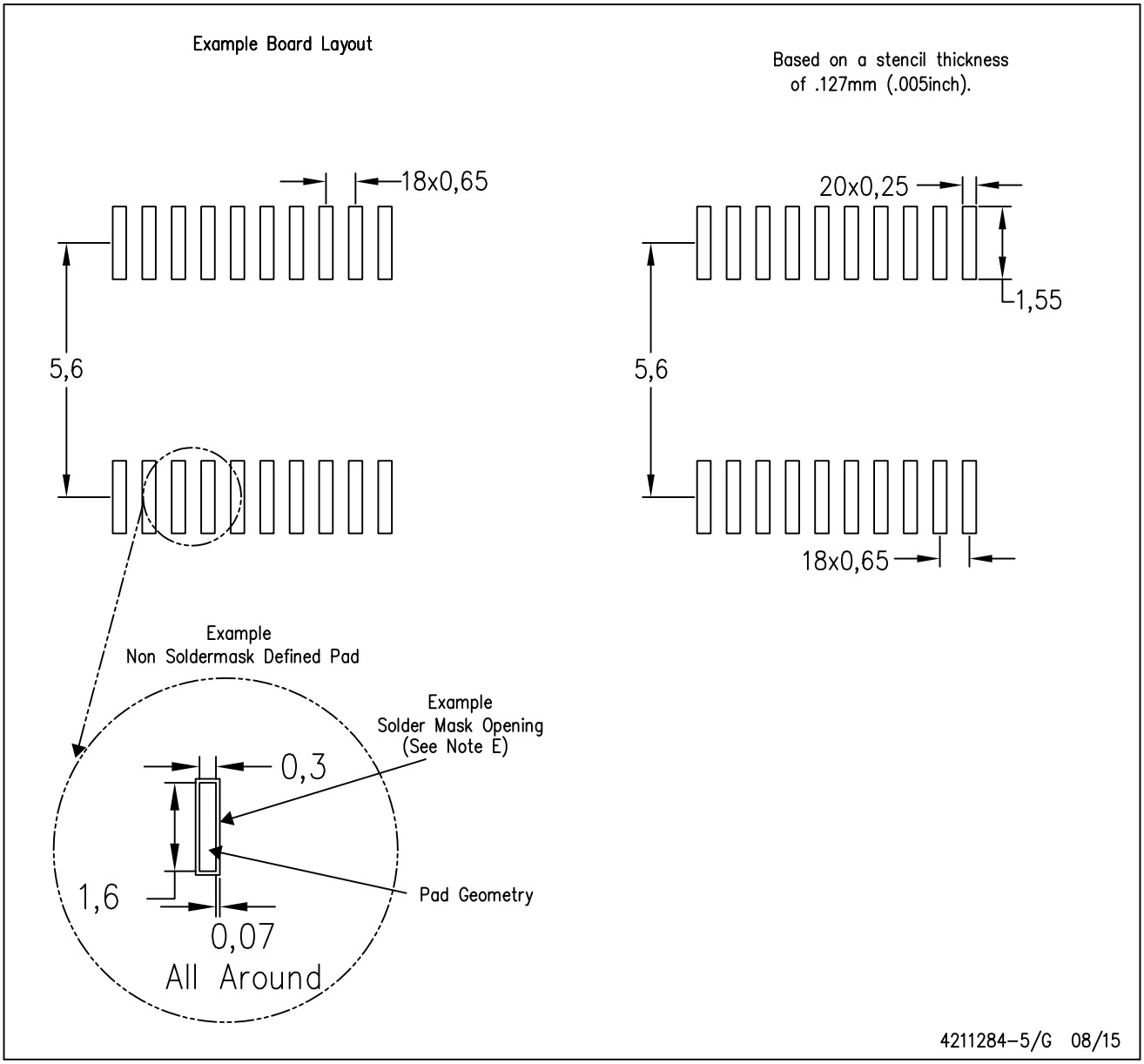
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

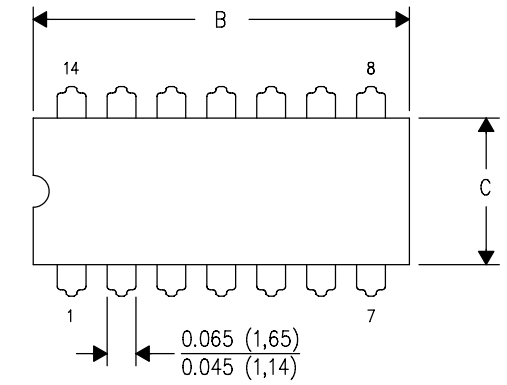


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

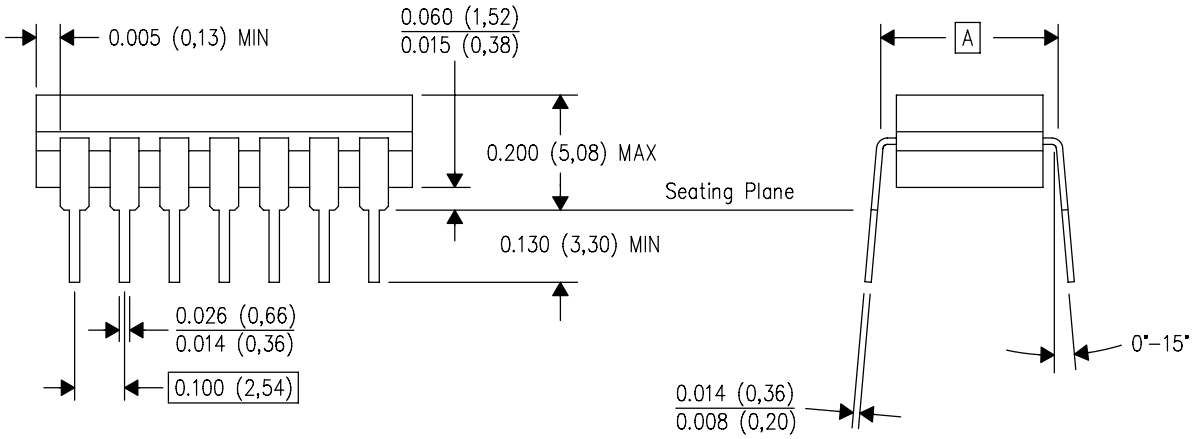
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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