

P-Channel 200 V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---------------------|---------------------------------|--------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) | Q _g (Typ.) |
| - 200 | 5.0 at V _{GS} = - 10 V | - 0.38 | 4.1 |
| | 5.1 at V _{GS} = - 6 V | - 0.37 | |

FEATURES

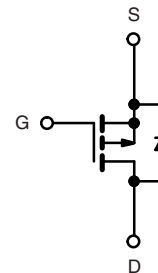
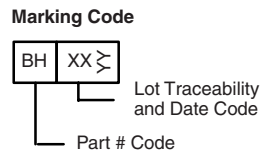
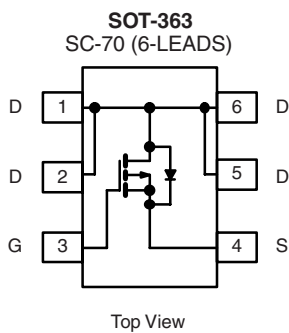
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETS
- Small, Thermally Enhanced SC-70 Package
- Ultra Low On-Resistance
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Active Clamp Circuits in dc-to-dc Power Supplies



P-Channel MOSFET

Ordering Information: Si1419DH-T1-E3 (Lead (Pb)-free)
Si1419DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | | |
|---|-----------------------------------|------------------------|--------------|--------|-----------------|
| Parameter | Symbol | 5 s | Steady State | Unit | |
| Drain-Source Voltage | V _{DS} | - 200 | | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | | |
| Continuous Drain Current (T _J = 150 °C) ^a | I _D | T _A = 25 °C | - 0.38 | - 0.3 | A |
| | | T _A = 85 °C | - 0.27 | - 0.22 | |
| Pulsed Drain Current | I _{DM} | - 0.5 | | | |
| Continuous Diode Current (Diode Conduction) ^a | I _S | - 1.3 | - 0.83 | | |
| Single Pulse Avalanche Current | I _{AS} | - 1.9 | | mJ | |
| Single Pulse Avalanche Energy | | | | | E _{AS} |
| Maximum Power Dissipation ^a | P _D | T _A = 25 °C | 1.56 | 1.0 | W |
| | | T _A = 85 °C | 0.81 | 0.52 | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | | °C | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|--------------|---------|------|------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^a | R _{thJA} | t ≤ 5 s | 60 | 80 | °C/W |
| | | Steady State | 100 | 125 | |
| Maximum Junction-to-Foot (Drain) | R _{thJF} | 34 | 45 | | |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

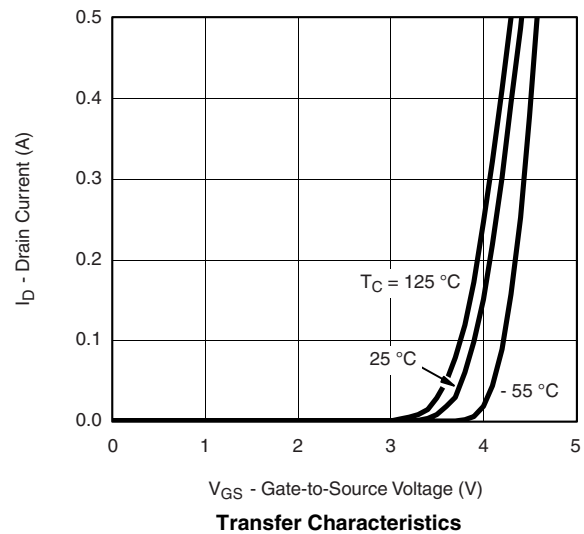
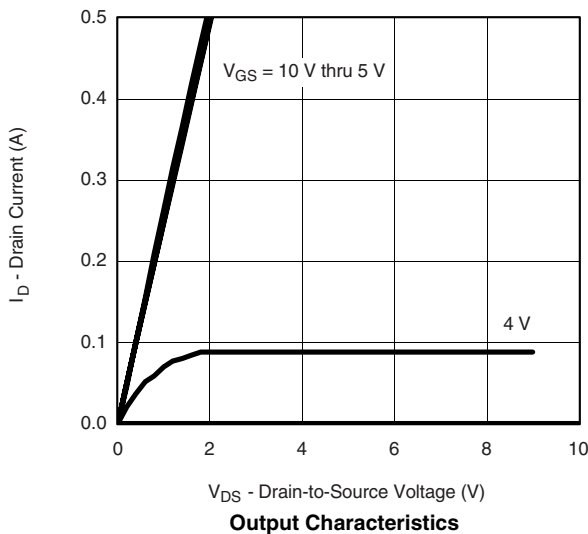
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|---|--------------|--|------|-------|-----------|---------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -100\text{ }\mu\text{A}$ | -2.5 | | -4.5 | V |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| | | $V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$ | | | -5 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}$ | -0.5 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = -10\text{ V}, I_D = -0.4\text{ A}$ | | 3.98 | 5.0 | Ω |
| | | $V_{GS} = -6\text{ V}, I_D = -0.4\text{ A}$ | | 4.06 | 5.1 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -10\text{ V}, I_D = -0.4\text{ A}$ | | 1.0 | | S |
| Diode Forward Voltage ^a | V_{SD} | $I_S = -0.4\text{ A}, V_{GS} = 0\text{ V}$ | | -0.80 | -1.1 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q_g | $V_{DS} = -100\text{ V}, V_{GS} = -10\text{ V}, I_D = -0.4\text{ A}$ | | 4.1 | 6.2 | nC |
| Gate-Source Charge | Q_{gs} | | | 0.8 | | |
| Gate-Drain Charge | Q_{gd} | | | 1.3 | | |
| Gate Resistance | R_g | $f = 1.0\text{ MHz}$ | | 17 | | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -100\text{ V}, R_L = 100\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$ | | 6 | 9 | ns |
| Rise Time | t_r | | | 12 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 12 | 18 | |
| Fall Time | t_f | | | 12 | 18 | |
| Reverse Recovery Time | t_{rr} | $I_F = -0.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$ | | 55 | 83 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | 130 | 200 | |

Notes:

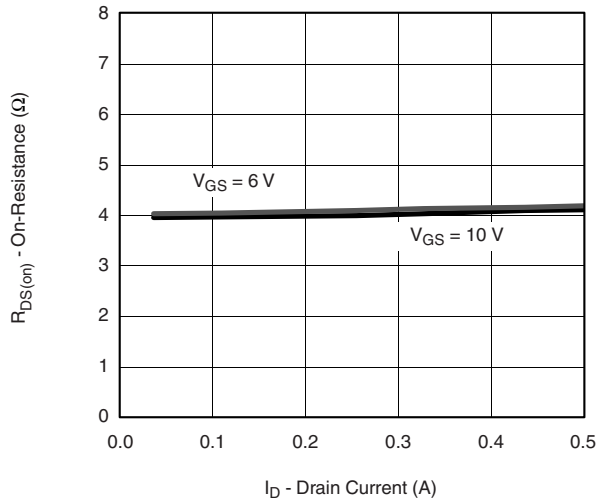
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

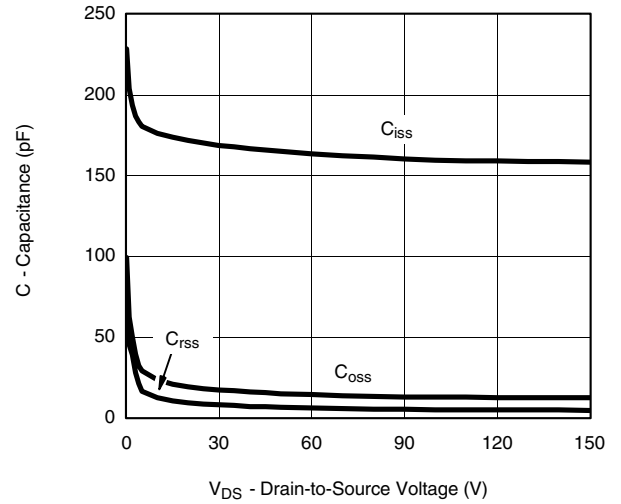
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



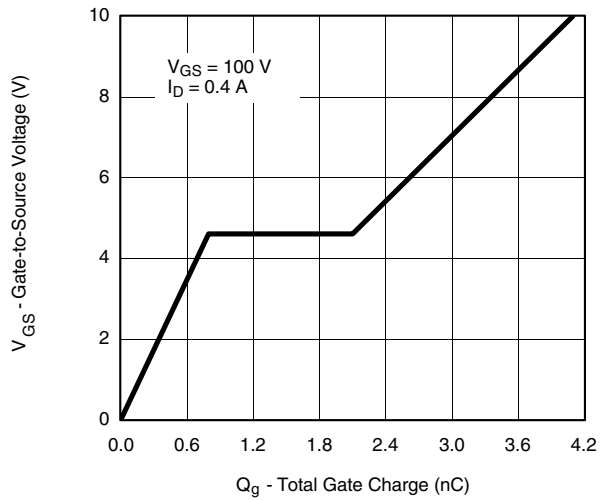
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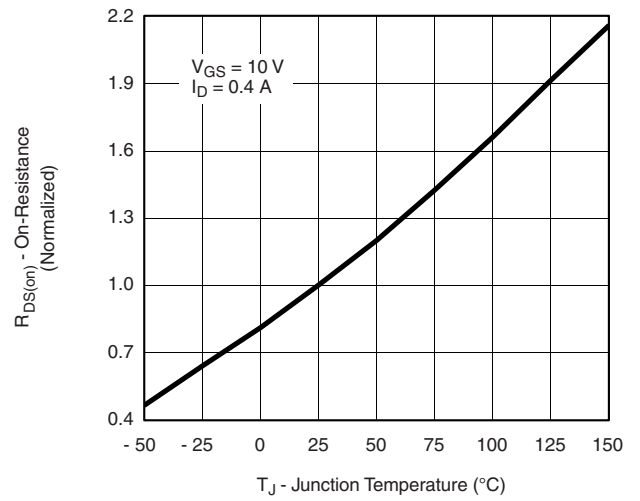
On-Resistance vs. Drain Current



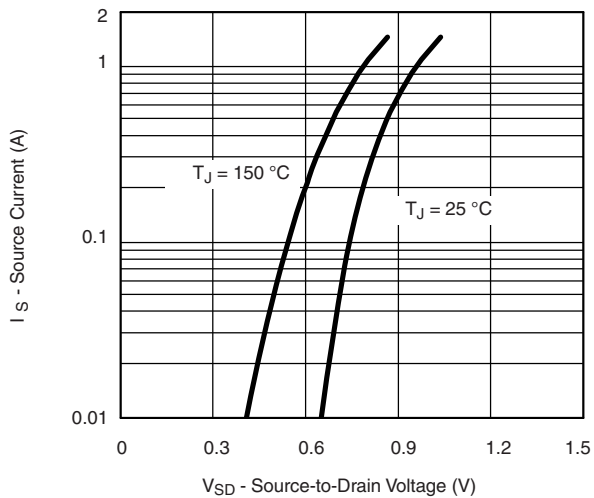
Capacitance



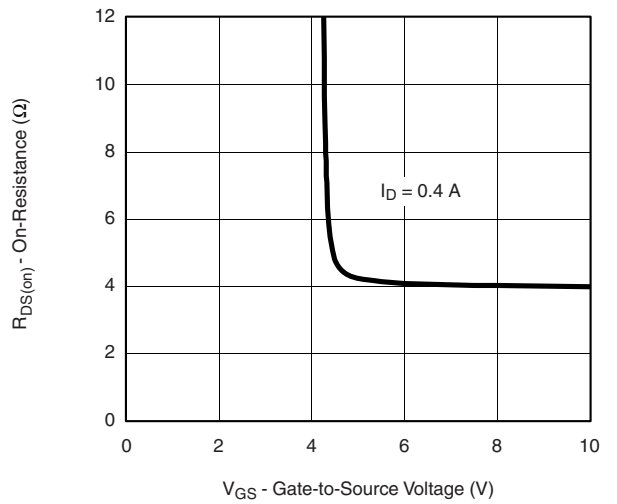
Gate Charge



On-Resistance vs. Junction Temperature

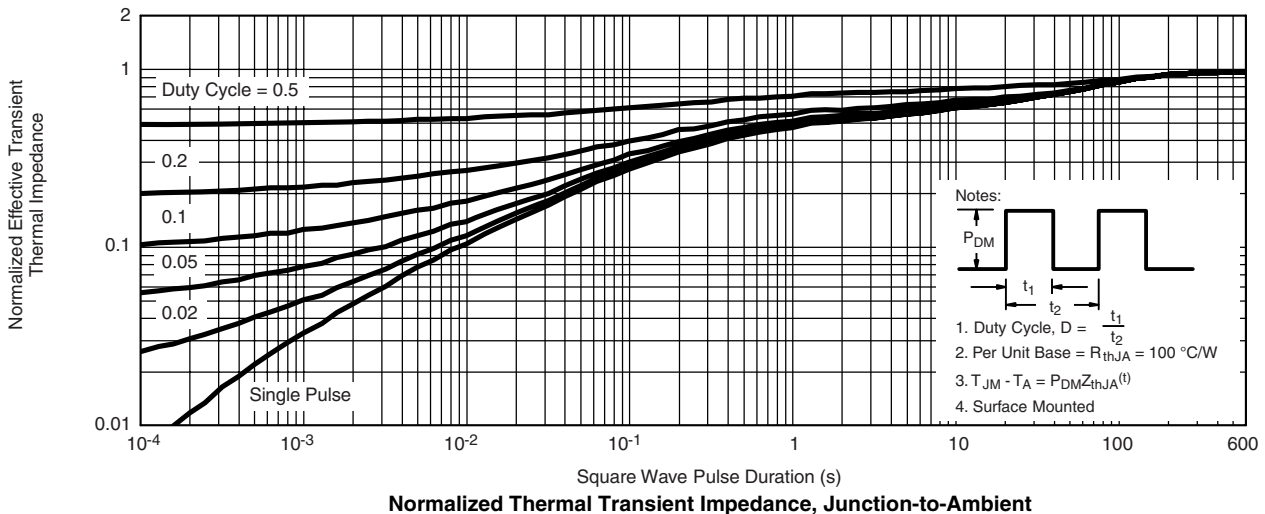
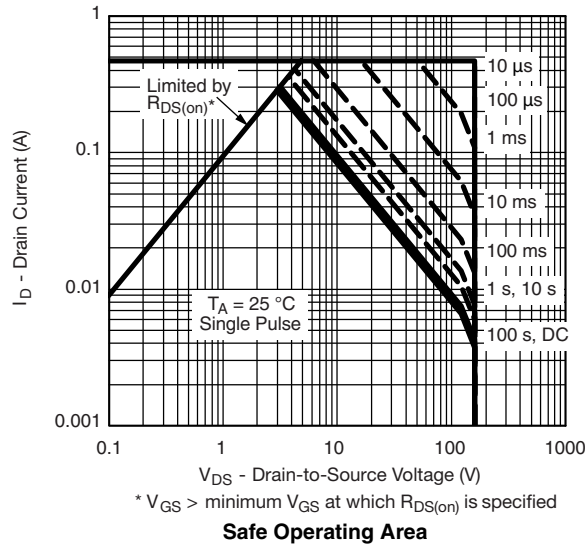
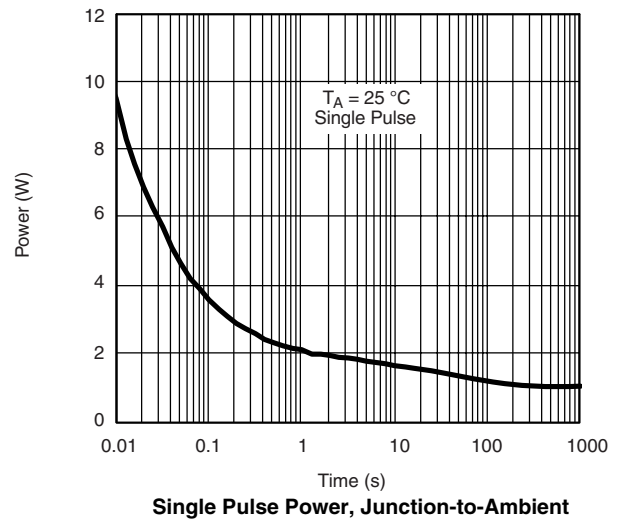
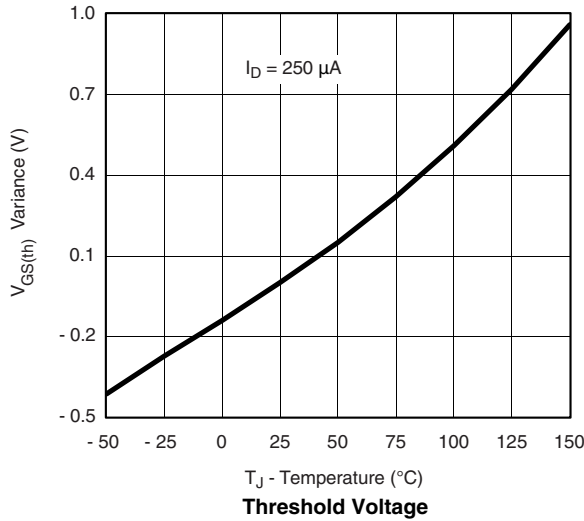


Source-Drain Diode Forward Voltage

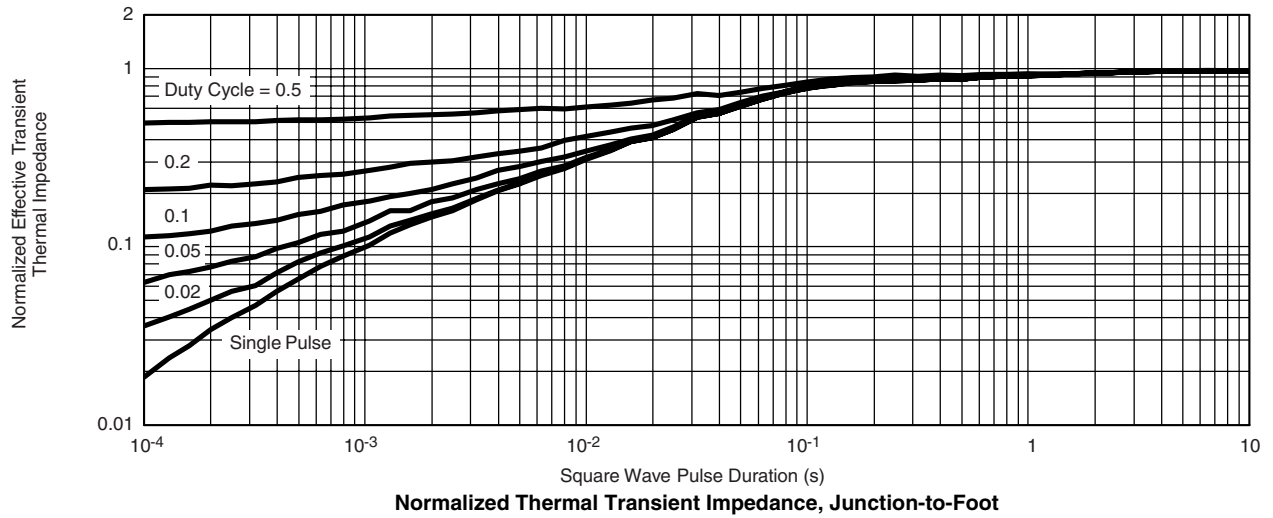


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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