19-3515; Rev 2; 1/07

EVALUATION KIT AVAILABLE

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

MAX5875

General Description

The MAX5875 is an advanced 16-bit, 200Msps, dual digital-to-analog converter (DAC). This DAC meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from 3.3V and 1.8V supplies, this dual DAC offers exceptional dynamic performance such as 78dBc spurious-free dynamic range (SFDR) at f_{OUT} = 16MHz and supports update rates of 200Msps, with a power dissipation of only 260mW.

The MAX5875 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and allows a $0.1V_{P-P}$ to $1V_{P-P}$ differential output voltage swing. The device features an integrated 1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy.

The digital and clock inputs of the MAX5875 accept 3.3V CMOS voltage levels. The device features a flexible input data bus that allows for dual-port input or a single-interleaved data port. The MAX5875 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended temperature range (-40°C to +85°C).

Refer to the MAX5873 and MAX5874 data sheets for pin-compatible 12-bit and 14-bit versions of the MAX5875, respectively. Refer to the MAX5878 data sheet for an LVDS-compatible version of the MAX5875.

Applications

Base Stations: Single/Multicarrier UMTS, CDMA, GSM

Communications: Fixed Broadband Wireless Access, Point-to-Point Microwave

Direct Digital Synthesis (DDS)

Cable Modem Termination Systems (CMTS)

Automated Test Equipment (ATE)

Instrumentation

Selector Guide

PART	RESOLUTION (Bits)	UPDATE RATE (Msps)	LOGIC INPUTS
MAX5873	12	200	CMOS
MAX5874	14	200	CMOS
MAX5875	16	200	CMOS
MAX5876	12	250	LVDS
MAX5877	14	250	LVDS
MAX5878	16	250	LVDS

Features

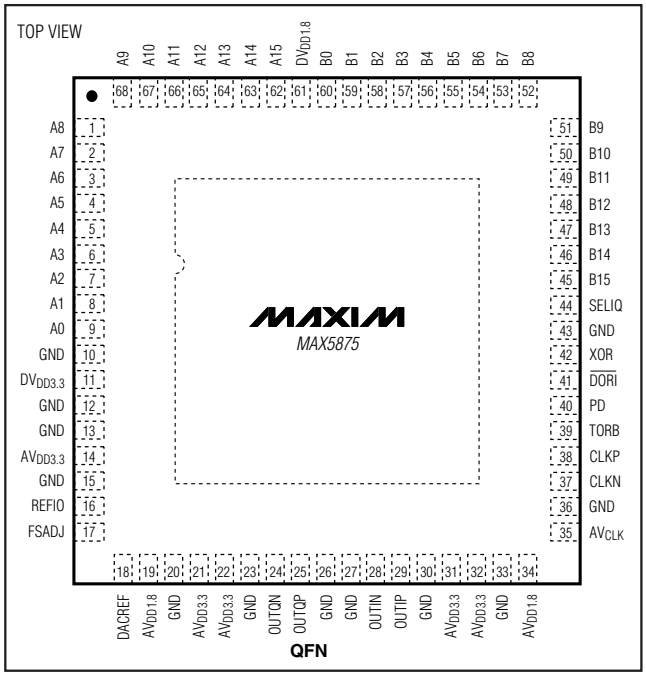
- **200Msps Output Update Rate**
- **Noise Spectral Density = -162dBFS/Hz at f_{OUT} = 16MHz**
- **Excellent SFDR and IMD Performance**
  - **SFDR = 78dBc at f_{OUT} = 16MHz (to Nyquist)**
  - **SFDR = 75dBc at f_{OUT} = 80MHz (to Nyquist)**
  - **IMD = -86dBc at f_{OUT} = 10MHz**
  - **IMD = -76dBc at f_{OUT} = 80MHz**
- **ACLR = 75dB at f_{OUT} = 61MHz**
- **2mA to 20mA Full-Scale Output Current**
- **CMOS-Compatible Digital and Clock Inputs**
- **On-Chip 1.2V Bandgap Reference**
- **Low 260mW Power Dissipation**
- **Compact 68-Pin QFN-EP Package (10mm x 10mm)**
- **Evaluation Kit Available (MAX5875EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5875EGK-D	-40°C to +85°C	68 QFN-EP*	G6800-4
MAX5875EGK+D	-40°C to +85°C	68 QFN-EP*	G6800-4

**EP = Exposed pad.*
+ Denotes lead-free package.
D = Dry pack.

Pin Configuration



16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

ABSOLUTE MAXIMUM RATINGS

$AV_{DD1.8}$, $DV_{DD1.8}$ to GND, DACREF .....-0.3V to +2.16V
$AV_{DD3.3}$, $DV_{DD3.3}$, AV_{CLK} to GND, DACREF.....-0.3V to +3.9V
REFIO, FSADJ to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTIP, OUTIN, OUTQP, OUTQN to GND, DACREF.....-1V to ($AV_{DD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF.....-0.3V to (AV_{CLK} + 0.3V)
A15/B15–A0/B0, XOR, SELIQ to GND, DACREF.....-0.3V to ($DV_{DD3.3}$ + 0.3V)
TORB, $\overline{DORI}$, PD to GND, DACREF ....-0.3V to ($DV_{DD3.3}$ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
68-Pin QFN-EP
(derate 41.7mW/°C above +70°C) (Note 1).....3333.3mW
Thermal Resistance θ_{JA} (Note 1).....+24°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Thermal resistors based on a multilayer board with 4 x 4 via array in exposed paddle area.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, GND = 0, f_{CLK} = f_{DAC}, external reference V_{REFIO} = 1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution					16		Bits
Integral Nonlinearity	INL	Measured differentially			±3		LSB
Differential Nonlinearity	DNL	Measured differentially			±2		LSB
Offset Error	OS			-0.025	±0.001	+0.025	%FS
Offset-Drift Tempco					±10		ppm/°C
Full-Scale Gain Error	GE_{FS}	External reference			±1		%FS
Gain-Drift Tempco		Internal reference			±100		ppm/°C
		External reference			±50		
Full-Scale Output Current	I_{OUTFS}	(Note 3)		2		20	mA
Output Compliance		Single-ended		-0.5		+1.1	V
Output Resistance	R_{OUT}				1		MΩ
Output Capacitance	C_{OUT}				5		pF
DYNAMIC PERFORMANCE							
Clock Frequency	f_{CLK}			1		200	MHz
Output Update Rate	f_{DAC}	f_{DAC} = f_{CLK} / 2, single-port mode		1		100	Msps
		f_{DAC} = f_{CLK}, dual-port mode		1		200	
Noise Spectral Density		f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		-162		dBFS/Hz
		f_{DAC} = 200MHz	f_{OUT} = 80MHz, -12dBFS		-160		

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, GND = 0, f_{CLK} = f_{DAC}, external reference V_{REFIO} = 1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{DAC} = 100MHz	f_{OUT} = 1MHz, 0dBFS		88		dBc
			f_{OUT} = 1MHz, -6dBFS		84		
			f_{OUT} = 1MHz, -12dBFS		82		
			f_{OUT} = 10MHz, -12dBFS		81		
			f_{OUT} = 30MHz, -12dBFS		79		
		f_{DAC} = 200MHz	f_{OUT} = 10MHz, -12dBFS		80		
			f_{OUT} = 16MHz, -12dBFS, $T_A \geq +25°C$	71	78		
			f_{OUT} = 16MHz, 0dBFS		87		
			f_{OUT} = 50MHz, -12dBFS		78		
			f_{OUT} = 80MHz, -12dBFS		75		
Spurious-Free Dynamic Range, 25MHz Bandwidth	SFDR	f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		84		dBc
Two-Tone IMD	TTIMD	f_{DAC} = 100MHz	f_{OUT1} = 9MHz, -7dBFS; f_{OUT2} = 10MHz, -7dBFS		-86		dBc
		f_{DAC} = 200MHz	f_{OUT1} = 79MHz, -7dBFS; f_{OUT2} = 80MHz, -7dBFS		-76		
Four-Tone IMD, 1MHz Frequency Spacing, GSM Model	FTIMD	f_{DAC} = 150MHz	f_{OUT} = 16MHz, -12dBFS		-86		dBc
Adjacent Channel Leakage Power Ratio 3.84MHz Bandwidth, W-CDMA Model	ACLR	f_{DAC} = 184.32MHz	f_{OUT} = 61.44MHz		75		dB
Output Bandwidth	BW_{-1dB}	(Note 4)			240		MHz
INTER-DAC CHARACTERISTICS							
Gain Matching	ΔGain	f_{OUT} = DC - 80MHz			±0.2		dB
		f_{OUT} = DC			+0.01		
Gain-Matching Tempco	ΔGain/°C				±20		ppm/°C
Phase Matching	ΔPhase	f_{OUT} = 60MHz			±0.25		Degrees
Phase-Matching Tempco	ΔPhase/°C	f_{OUT} = 60MHz			±0.002		Degrees/°C
Channel-to-Channel Crosstalk		f_{CLK} = 200MHz, f_{OUT} = 50MHz, 0dBFS			-70		dB
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.14	1.2	1.26	V
Reference Input Compliance Range	$V_{REFIOCR}$			0.125		1.250	V
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Drift	TCO_{REF}				±25		ppm/°C

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, GND = 0, f_{CLK} = f_{DAC}, external reference V_{REFIO} = 1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUT TIMING (See Figure 4)						
Output Fall Time	t_{FALL}	90% to 10% (Note 5)		0.7		ns
Output Rise Time	t_{RISE}	10% to 90% (Note 5)		0.7		ns
Output-Voltage Settling Time	t_{SETTLE}	Output settles to 0.025% FS (Note 5)		14		ns
Output Propagation Delay	t_{PD}	Excluding data latency (Note 5)		1.1		ns
Glitch Impulse		Measured differentially		1		pV•s
Output Noise	n_{OUT}	I_{OUTFS} = 2mA		30		pA/√Hz
		I_{OUTFS} = 20mA		30		
TIMING CHARACTERISTICS						
Data to Clock Setup Time	t_{SETUP}	Referenced to rising edge of clock (Note 6)	-0.6	-1.2		ns
Data to Clock Hold Time	t_{HOLD}	Referenced to rising edge of clock (Note 6)	2.1	1.5		ns
Single-Port (Interleaved Mode) Data Latency		Latency to I output		9		Clock Cycles
		Latency to Q output		8		
Dual-Port (Parallel Mode) Data Latency				5.5		Clock Cycles
Minimum Clock Pulse-Width High	t_{CH}	CLKP, CLKN		2.4		ns
Minimum Clock Pulse-Width Low	t_{CL}	CLKP, CLKN		2.4		ns
CMOS LOGIC INPUTS (A15/B15–A0/B0, XOR, SELIQ, PD, TORB, $\overline{DORI}$)						
Input-Logic High	V_{IH}		0.7 x $DV_{DD3.3}$			V
Input-Logic Low	V_{IL}				0.3 x $DV_{DD3.3}$	V
Input Leakage Current	I_{IN}			1	20	µA
PD, TORB, $\overline{DORI}$ Internal Pulldown Resistance		V_{PD} = V_{TORB} = $V_{\overline{DORI}}$ = 3.3V		1.5		MΩ
Input Capacitance	C_{IN}			2.5		pF
CLOCK INPUTS (CLKP, CLKN)						
Differential Input Voltage Swing		Sine wave		> 1.5		V_{P-P}
		Square wave		> 0.5		
Differential Input Slew Rate	SR_{CLK}	(Note 7)		> 100		V/µs
External Common-Mode Voltage Range	V_{COM}			AV_{CLK} / 2 ±0.3		V
Input Resistance	R_{CLK}			5		kΩ
Input Capacitance	C_{CLK}			2.5		pF
POWER SUPPLIES						
Analog Supply Voltage Range	$AV_{DD3.3}$		3.135	3.3	3.465	V
	$AV_{DD1.8}$		1.710	1.8	1.890	
Digital Supply Voltage Range	$DV_{DD3.3}$		3.135	3.3	3.465	V
	$DV_{DD1.8}$		1.710	1.8	1.890	
Clock Supply Voltage Range	AV_{CLK}		3.135	3.3	3.465	V

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, GND = 0, f_{CLK} = f_{DAC}, external reference V_{REFIO} = 1.25V, output load 50Ω double-terminated, transformer-coupled output, I_{OUTFS} = 20mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

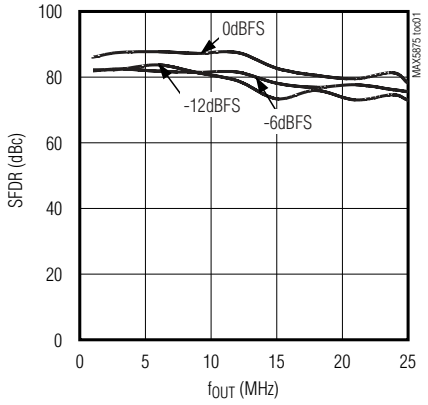
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	$I_{AVDD3.3}$ + I_{AVCLK}	f_{DAC} = 200Msps, f_{OUT} = 1MHz		53	58	mA
		Power-down		0.002		
	$I_{AVDD1.8}$	f_{DAC} = 200Msps, f_{OUT} = 1MHz		25	32	
		Power-down		0.001		
Digital Supply Current	$I_{DVDD3.3}$	f_{DAC} = 200Msps, f_{OUT} = 1MHz		0.5	3	mA
		Power-down		0.001		
	$I_{DVDD1.8}$	f_{DAC} = 200Msps, f_{OUT} = 1MHz		22	25	
		Power-down		0.001		
Power Dissipation	P_{DISS}	f_{DAC} = 200Msps, f_{OUT} = 1MHz		260	300	mW
		Power-down		14		µW
Power-Supply Rejection Ratio	PSRR	$AV_{DD3.3}$ = AV_{CLK} = $DV_{DD3.3}$ = +3.3V ±5% (Notes 7, 8)	-0.1		+0.1	%FS/V

Note 2: Specifications at T_A ≥ +25°C are guaranteed by production testing. Specifications at T_A < +25°C are guaranteed by design and characterization data.
Note 3: Nominal full-scale current I_{OUTFS} = 32 x I_{REF}.
Note 4: This parameter does not include update-rate-dependent effects of sin(x)/x filtering inherent in the MAX5875.
Note 5: Parameter measured single-ended into a 50Ω termination resistor.
Note 6: Not production tested. Guaranteed by design and characterization data.
Note 7: A differential clock input slew rate of > 100V/µs is required to achieve the specified dynamic performance.
Note 8: Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltage.

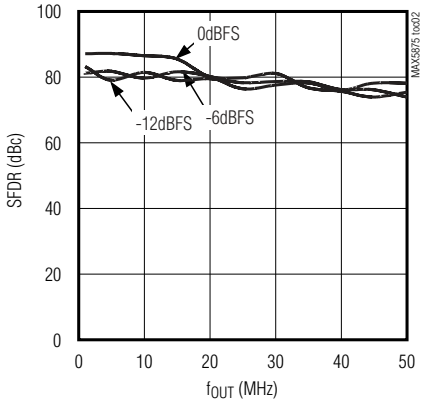
Typical Operating Characteristics

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference, V_{REFIO} = 1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

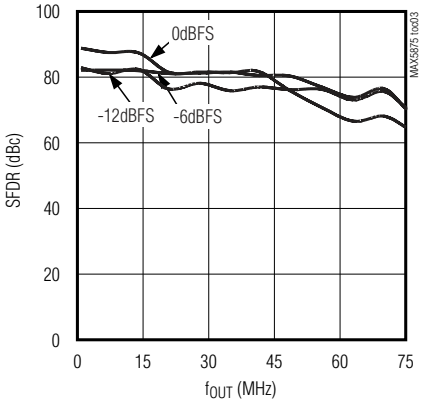
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 50Msps)



SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 100Msps)



SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 150Msps)

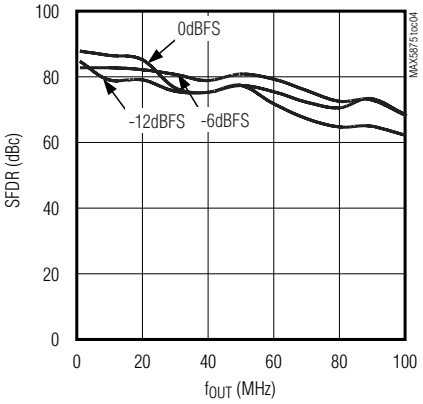


16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

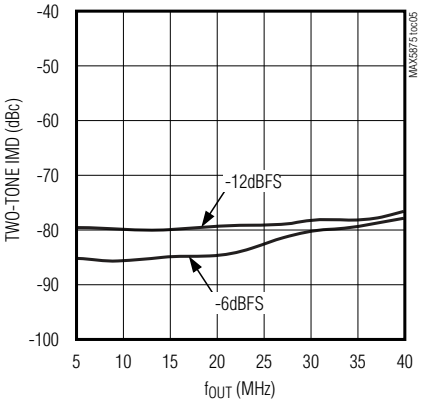
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference, V_{REFIO} = 1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

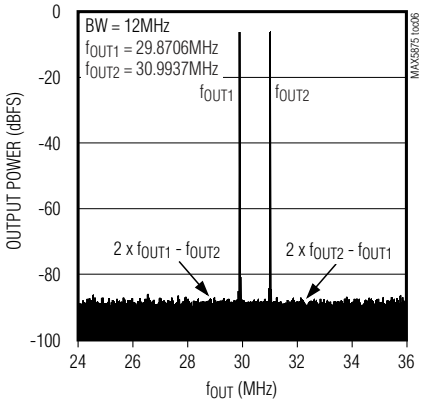
SINGLE-TONE SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 200Msps)



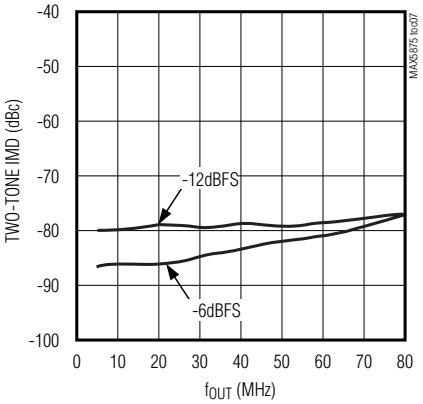
TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, f_{CLK} = 100Msps)



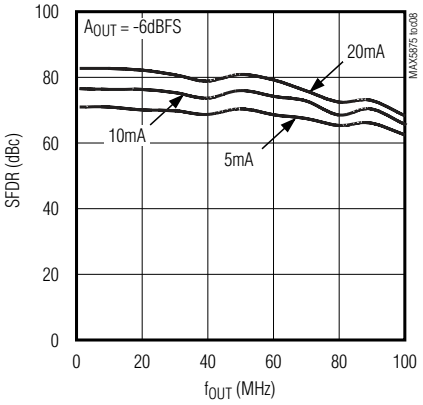
TWO-TONE IMD (f_{CLK} = 100Msps)



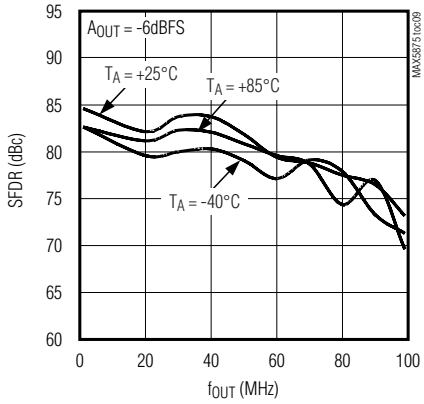
TWO-TONE IMD vs. OUTPUT FREQUENCY (1MHz CARRIER SPACING, f_{CLK} = 200Msps)



SFDR vs. FULL-SCALE OUTPUT CURRENT (f_{CLK} = 200MHz)



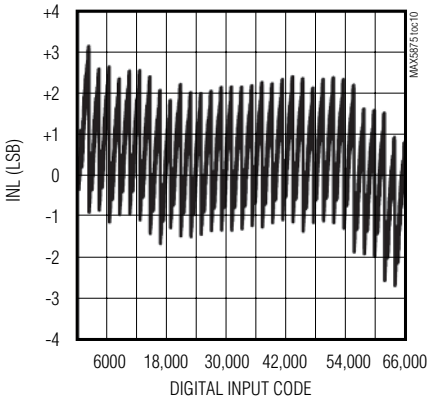
SFDR vs. TEMPERATURE (f_{CLK} = 200MHz)



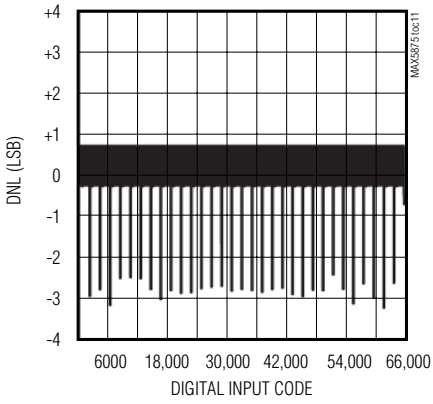
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference, V_{REFIO} = 1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

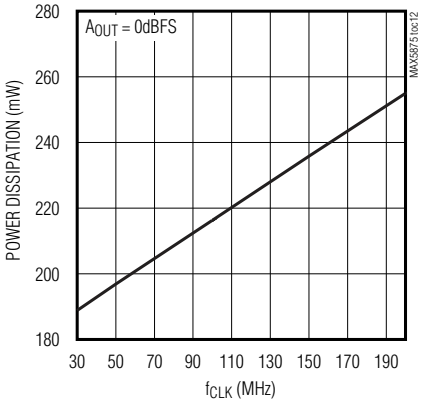
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



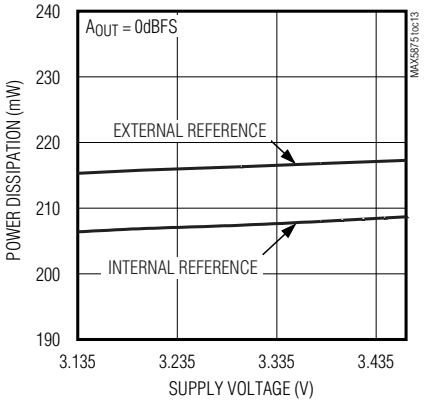
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



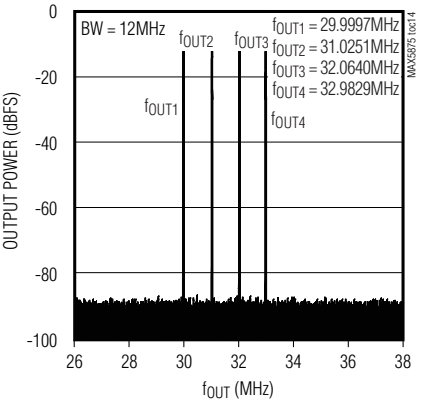
POWER DISSIPATION vs. CLOCK FREQUENCY (f_{OUT} = 10MHz)



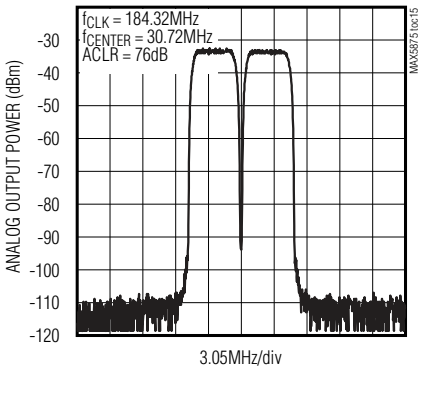
POWER DISSIPATION vs. SUPPLY VOLTAGE (f_{CLK} = 100MHz, f_{OUT} = 10MHz)



FOUR-TONE POWER RATIO PLOT (f_{CLK} = 150MHz, f_{CENTER} = 31.6040MHz)



ACLR FOR WCDMA MODULATION, TWO CARRIERS

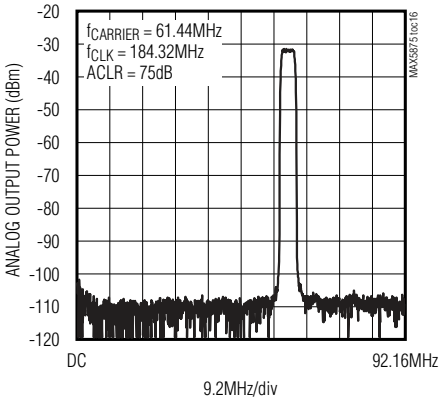


16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

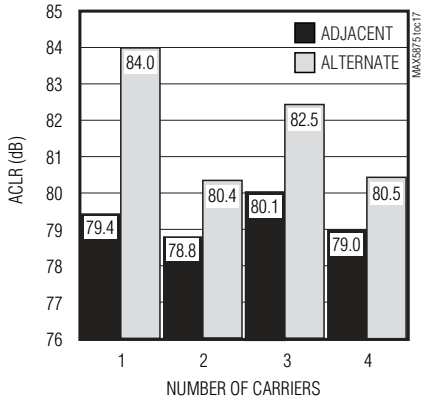
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = $DV_{DD3.3}$ = AV_{CLK} = 3.3V, $AV_{DD1.8}$ = $DV_{DD1.8}$ = 1.8V, external reference, V_{REFIO} = 1.25V, R_L = 50Ω double-terminated, I_{OUTFS} = 20mA, T_A = +25°C, unless otherwise noted.)

ACLR FOR WCDMA MODULATION, SINGLE CARRIER



WCDMA BASEBAND ACLR



Pin Description

PIN	NAME	FUNCTION
1–9	A8, A7, A6, A5, A4, A3, A2, A1, A0	Data Bits A8–A0. In dual-port mode, data is directed to the Q-DAC. In single-port mode, data bits are not used. Connect bits A8–A0 to GND in single-port mode.
10, 12, 13, 15, 20, 23, 26, 27, 30, 33, 36, 43	GND	Converter Ground
11	$DV_{DD3.3}$	Digital Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to GND.
14, 21, 22, 31, 32	$AV_{DD3.3}$	Analog Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass each pin with a 0.1µF capacitor to GND.
16	REFIO	Reference I/O. Output of the internal 1.2V precision bandgap reference. Bypass with a 1µF capacitor to GND. REFIO can be driven with an external reference source. See Table 1.
17	FSADJ	Full-Scale Adjust Input. This input sets the full-scale output current of the DAC. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. See Table 1.
18	DACREF	Current-Set Resistor Return Path. Internally connected to GND. **Do not use an external ground connection.**
19, 34	$AV_{DD1.8}$	Analog Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass each pin with a 0.1µF capacitor to GND.
24	OUTQN	Complementary Q-DAC Output. Negative terminal for current output.
25	OUTQP	Q-DAC Output. Positive terminal for current output.
28	OUTIN	Complementary I-DAC Output. Negative terminal for current output.
29	OUTIP	I-DAC Output. Positive terminal for current output.
35	AV_{CLK}	Clock Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1µF capacitor to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
37	CLKN	Complementary Converter Clock Input. Negative input terminal for differential converter clock. Internally biased to AV_{CLK} / 2.
38	CLKP	Converter Clock Input. Positive input terminal for differential converter clock. Internally biased to AV_{CLK} / 2.
39	TORB	Two's-Complement/Binary Select Input. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate a binary input format. TORB has an internal pulldown resistor.
40	PD	Power-Down Input. Set PD high to force the DAC into power-down mode. Set PD low for normal operation. PD has an internal pulldown resistor.
41	$\overline{DORI}$	Dual-(Parallel)/Single-(Interleaved) Port Select Input. Set $\overline{DORI}$ high to configure as a dual-port DAC. Set $\overline{DORI}$ low to configure as a single-port interleaved DAC. $\overline{DORI}$ has an internal pulldown resistor.
42	XOR	DAC Exclusive-OR Select Input. Set XOR low to allow the data stream to pass unchanged to the DAC input. Set XOR high to invert the input data into the DAC. If unused, connect XOR to GND.
44	SELIQ	DAC Select Input. Set SELIQ low to direct data into the Q-DAC inputs. Set SELIQ high to direct data into the I-DAC inputs. If unused, connect SELIQ to GND. SELIQ's logic state is only valid in single-port (interleaved) mode.
45–60	B15, B14, B13, B12, B11, B10, B9, B8, B7, B6, B5, B4, B3, B2, B1, B0	Data Bits B15–B0. In dual-port mode, data is directed to the I-DAC. In single-port mode, the state of SELIQ determines where the data bits are directed.
61	$DV_{DD1.8}$	Digital Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass with a 0.1µF capacitor to GND.
62–68	A15, A14, A13, A12, A11, A10, A9	Data Bits A15–A9. In dual-port mode, data is directed to the Q-DAC. In single-port mode, data bits are not used. Connect bits A15–A9 to GND in single-port mode.
—	EP	Exposed Pad. Must be connected to GND through a low-impedance path.

Detailed Description

Architecture

The MAX5875 high-performance, 16-bit, dual current-steering DAC (Figure 1) operates with DAC update rates up to 200Msps. The converter consists of input registers and a demultiplexer for single-port (interleaved) mode, followed by a current-steering array. During operation in interleaved mode, the input data registers demultiplex the single-port data bus. The current-steering array generates differential full-scale currents in the 2mA to 20mA range. An internal current-switching network, in combination with external 50Ω termination resistors, converts the differential output currents into dual differential output voltages with a 0.1V to 1V peak-to-peak output voltage range. An integrated 1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale output range.

Reference Architecture and Operation

The MAX5875 supports operation with the internal 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source. REFIO also serves as a reference output when the DAC operates in internal reference mode. For stable operation with the internal reference, decouple REFIO to GND with a 1µF capacitor. Due to its limited output-drive capability, buffer REFIO with an external amplifier when driving large external loads.

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

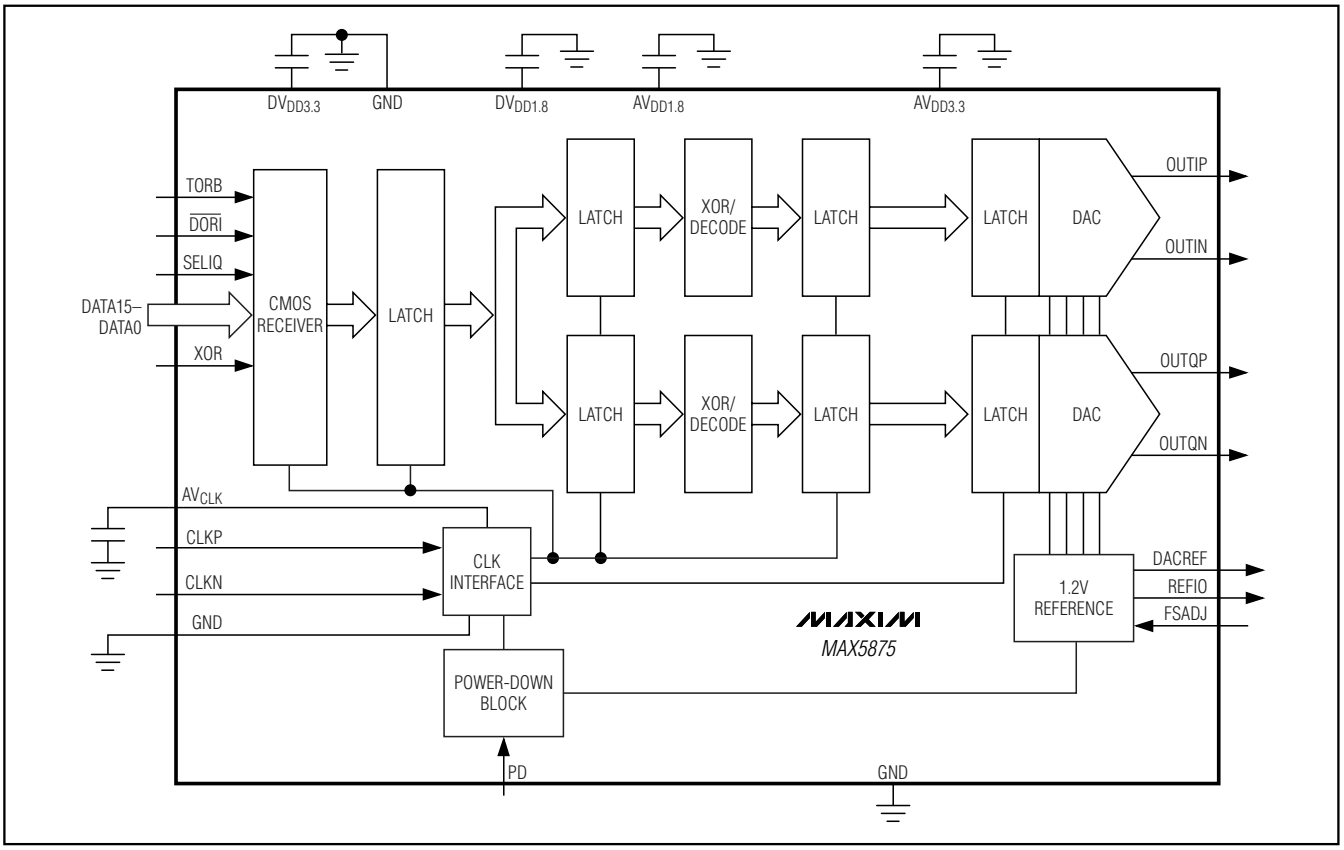


Figure 1. MAX5875 High-Performance, 16-Bit, Dual Current-Steering DAC

The MAX5875's reference circuit (Figure 2) employs a control amplifier to regulate the full-scale current I_{OUTFS} for the differential current outputs of the DAC. Calculate the full-scale output current as follows:

$$I_{OUTFS} = 32 \times \frac{V_{REFIO}}{R_{SET}} \times \left(1 - \frac{1}{2^{16}}\right)$$

where I_{OUTFS} is the full-scale output current of the DAC. R_{SET} (located between FSADJ and DACREF) determines the amplifier's full-scale output current for the DAC. See Table 1 for a matrix of different I_{OUTFS} and R_{SET} selections.

Analog Outputs (OUTIP, OUTIN, OUTQP, OUTQN)

Each MAX5875 DAC outputs two complementary currents (OUTIP/N, OUTQP/N) that operate in a single-ended or differential configuration. A load resistor converts these two output currents into complementary single-ended output voltages. A transformer or a differential amplifier configuration converts the differential voltage existing between OUTIP (OUTQP) and OUTIN (OUTQN) to a single-ended voltage. If not using a transformer, the recommended termination from the output is a 25Ω termination resistor to ground and a 50Ω resistor between the outputs.

Table 1. I_{OUTFS} and R_{SET} Selection Matrix Based on a Typical 1.200V Reference Voltage

FULL-SCALE CURRENT I_{OUTFS} (mA)	R_{SET} (Ω)	
	CALCULATED	1% EIA STD
2	19.2k	19.1k
5	7.68k	7.5k
10	3.84k	3.83k
15	2.56k	2.55k
20	1.92k	1.91k

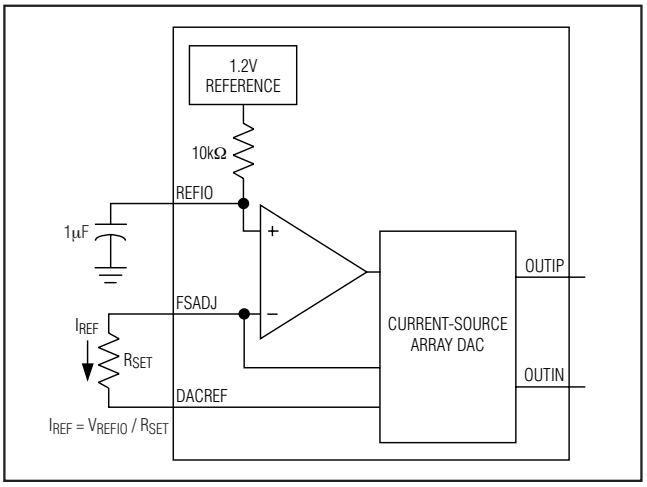


Figure 2. Reference Architecture, Internal Reference Configuration

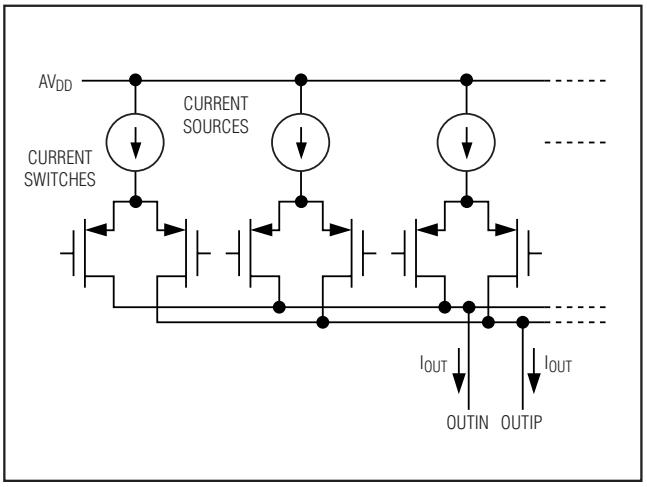


Figure 3. Simplified Analog Output Structure

To generate a single-ended output, select OUTIP (or OUTQP) as the output and connect OUTIN (or OUTQN) to GND. SFDR degrades with single-ended operation. Figure 3 displays a simplified diagram of the internal output structure of the MAX5875.

Clock Inputs (CLKP, CLKN)

The MAX5875 features flexible differential clock inputs (CLKP, CLKN) operating from a separate supply (AV_{CLK}) to achieve the optimum jitter performance. Drive the differential clock inputs from a single-ended or a differential clock source. For single-ended operation, drive CLKP with a logic source and bypass CLKN to GND with a 0.1µF capacitor.

CLKP and CLKN are internally biased to AV_{CLK} / 2. This facilitates the AC-coupling of clock sources directly to the device without external resistors to define the DC level. The dynamic input resistance from CLKP and CLKN to ground is > 5kΩ.

Data Timing Relationship

Figure 4 displays the timing relationship between digital CMOS data, clock, and output signals. The MAX5875 features a 1.5ns hold, a -1.2ns setup, and a 1.1ns propagation delay time. A nine (eight)-clock-cycle latency exists between CLKP/CLKN and OUTIP/OUTIN (OUTQP/OUTQN) when operating in single-port (interleaved) mode. In dual-port (parallel) mode, the clock latency is 5.5 clock cycles for both channels. Table 2 shows the DAC output codes.

Table 2. DAC Output Code Table

DIGITAL INPUT CODE		OUT_P	OUT_N
OFFSET BINARY	TWO'S COMPLEMENT		
0000 0000 0000 0000	1000 0000 0000 0000	0	I_{OUTFS}
0111 1111 1111 1111	0000 0000 0000 0000	I_{OUTFS} / 2	I_{OUTFS} / 2
1111 1111 1111 1111	0111 1111 1111 1111	I_{OUTFS}	0

CMOS-Compatible Digital Inputs

Input Data Format Select (TORB, $\overline{DORI}$)

The TORB input selects between two's-complement or binary digital input data. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate a binary input format.

The $\overline{DORI}$ input selects between a dual-port (parallel) or single-port (interleaved) DAC. Set $\overline{DORI}$ high to configure the MAX5875 as a dual-port DAC. Set $\overline{DORI}$ low to configure the MAX5875 as a single-port DAC. In dual-port mode, connect SELIQ to ground.

CMOS DAC Inputs (A15/B15–A0/B0, XOR, SELIQ)

The MAX5875 latches input data on the rising edge of the clock in a user-selectable two's-complement or binary format. A logic-high voltage on TORB selects two's-complement and a logic-low selects offset binary format.

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

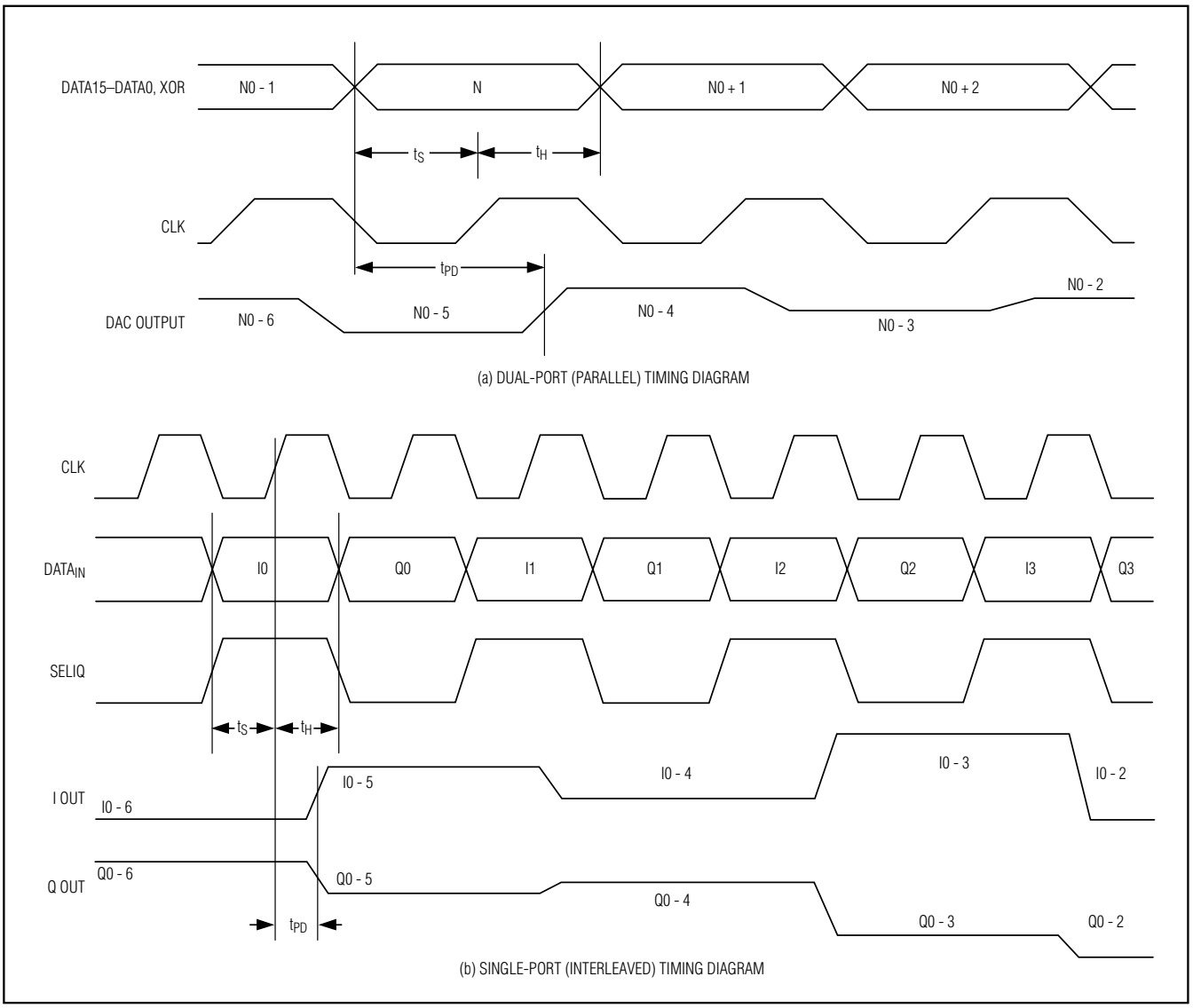


Figure 4. Timing Relationships Between Clock and Input Data for (a) Dual-Port (Parallel) Mode and (b) Single-Port (Interleaved) Mode

The MAX5875 includes a single-ended, CMOS-compatible XOR input. Input data (all bits) are compared with the bit applied to XOR through exclusive-OR gates. Pulling XOR high inverts the input data. Pulling XOR low leaves the input data noninverted. By applying a previously encoded pseudo-random bit stream to the data input and applying decoding to XOR, the digital input data can be decorrelated from the DAC output, allowing for the troubleshooting of possible spurious or harmonic distortion degradation due to digital feedthrough on the printed circuit board (PCB).

A15/B15–A0/B0, XOR, and SELIQ are latched on the rising edge of the clock. In single-port mode ($\overline{DORI}$ pulled low) a logic-high signal on SELIQ directs the B15–B0 data onto the I-DAC inputs. A logic-low signal at SELIQ directs data to the Q-DAC inputs. In dual-port (parallel) mode ($\overline{DORI}$ pulled high), data on pins A15–A0 are directed onto the Q-DAC inputs and B15–B0 are directed onto the I-DAC inputs.

Power-Down Operation (PD)

The MAX5875 also features an active-high power-down mode that reduces the DAC's digital current

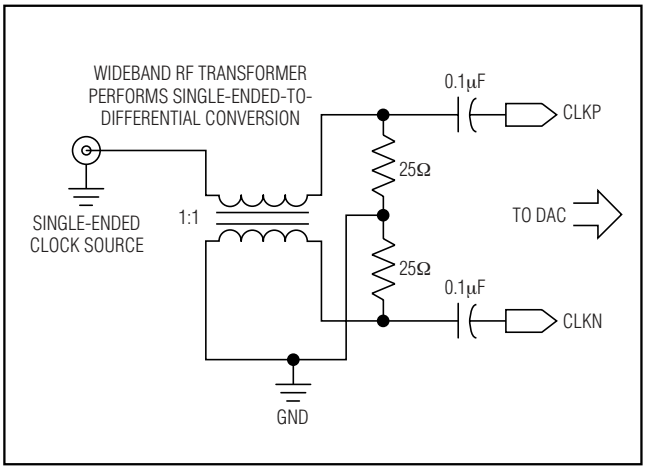


Figure 5. Differential Clock-Signal Generation

consumption from 22.5mA to less than 2µA and the analog current consumption from 78mA to less than 3µA. Set PD high to power down the MAX5875. Set PD low for normal operation.

When powered down, the power consumption of the MAX5875 is reduced to less than 14µW. The MAX5875 requires 10ms to wake up from power-down and enter a fully operational state. The PD integrated pulldown resistor activates the MAX5875 if PD is left floating.

Applications Information

CLK Interface

The MAX5875 features a flexible differential clock input (CLKP, CLKN) with a separate supply (AV_{CLK}) to achieve optimum jitter performance. Use an ultra-low jitter clock to achieve the required noise density. Clock jitter must be less than $0.5ps_{RMS}$ for meeting the specified noise density. For that reason, the CLKP/CLKN input source must be designed carefully. The differential clock (CLKN and CLKP) input can be driven from a single-ended or a differential clock source. Differential clock drive is required to achieve the best dynamic performance from the DAC. For single-ended operation, drive CLKP with a low noise source and bypass CLKN to GND with a 0.1µF capacitor.

Figure 5 shows a convenient and quick way to apply a differential signal created from a single-ended source (e.g., HP/Agilent 8644B signal generator) and a wideband transformer. Alternatively, these inputs may be driven from a CMOS-compatible clock source; however, it is recommended to use sinewave or AC-coupled differential ECL/PECL drive for best dynamic performance.

Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

Use a pair of transformers (Figure 6) or a differential amplifier configuration to convert the differential voltage existing between OUTIP/OUTQP and OUTIN/OUTQN to a single-ended voltage. Optimize the dynamic performance by using a differential transformer-coupled output to limit the output power to < 0dBm full scale. Pay close attention to the transformer core saturation characteristics when selecting a transformer for the MAX5875. Transformer core saturation can introduce strong 2nd-order harmonic distortion, especially at low output frequencies and high signal amplitudes. For best results, center tap the transformer to ground. When not using a transformer, terminate each DAC output to ground with a 25Ω resistor. Additionally, place a 50Ω resistor between the outputs (Figure 7).

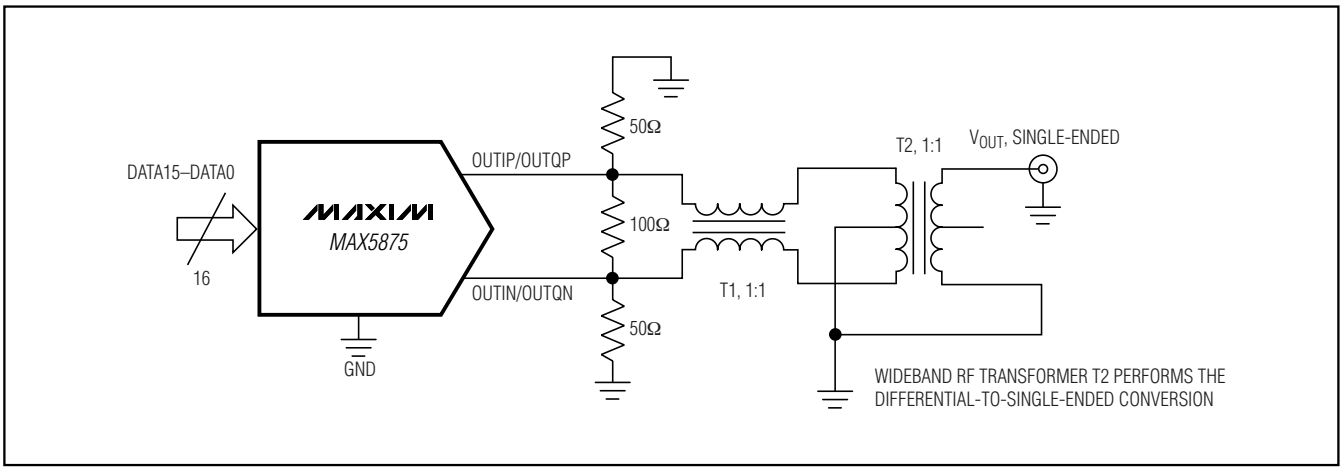


Figure 6. Differential to Single-Ended Conversion Using a Wideband RF Transformer

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

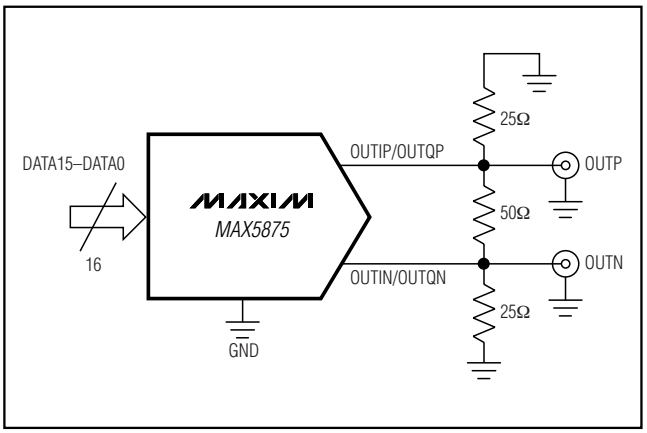


Figure 7. Differential Output Configuration

For a single-ended unipolar output, select OUTIP (OUTQP) as the output and ground OUTIN (OUTQN) to GND. Driving the MAX5875 single-ended is not recommended since additional noise and distortion will be added.

The distortion performance of the DAC depends on the load impedance. The MAX5875 is optimized for 50Ω differential double termination. It can be used with a transformer output as shown in Figure 6 or just one 25Ω resistor from each output to ground and one 50Ω resistor between the outputs (Figure 7). This produces a full-scale output power of up to -2dBm, depending on the output current setting. Higher termination impedance can be used at the cost of degraded distortion performance and increased output noise voltage.

Grounding, Bypassing, and Power-Supply Considerations

Grounding and power-supply decoupling can strongly influence the MAX5875 performance. Unwanted digital crosstalk couples through the input, reference, power supply, and ground connections, and affects dynamic performance. High-speed, high-frequency applications require closely followed proper grounding and power-supply decoupling. These techniques reduce EMI and internal crosstalk that can significantly affect the MAX5875 dynamic performance.

Use a multilayer PCB with separate ground and power-supply planes. Run high-speed signals on lines directly above the ground plane. Keep digital signals as far away from sensitive analog inputs and outputs, reference inputs sense lines, and clock inputs as practical. Use a controlled-impedance symmetric design of clock input and the analog output lines to minimize 2nd-order harmonic-distortion components, thus optimizing the DAC's dynamic performance. Keep digital signal paths short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5875 requires five separate power-supply inputs for analog ($AV_{DD1.8}$ and $AV_{DD3.3}$), digital ($DV_{DD1.8}$ and $DV_{DD3.3}$), and clock (AV_{CLK}) circuitry. Decouple each AV_{DD}, DV_{DD}, and AV_{CLK} input pin with a separate 0.1µF capacitor as close to the device as possible with the shortest possible connection to the ground plane (Figure 8). Minimize the analog and digital load capacitances for optimized operation. Decouple all three power-supply voltages at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

The analog and digital power-supply inputs $AV_{DD3.3}$, AV_{CLK}, and $DV_{DD3.3}$ allow a 3.135V to 3.465V supply voltage range. The analog and digital power-supply inputs $AV_{DD1.8}$ and $DV_{DD1.8}$ allow a 1.71V to 1.89V supply voltage range.

The MAX5875 is packaged in a 68-pin QFN-EP package, providing greater design flexibility and optimized DAC AC performance. The EP enables the use of necessary grounding techniques to ensure highest performance operation. Thermal efficiency is not the key factor, since the MAX5875 features low-power operation. The exposed pad ensures a solid ground connection between the DAC and the PCB's ground layer.

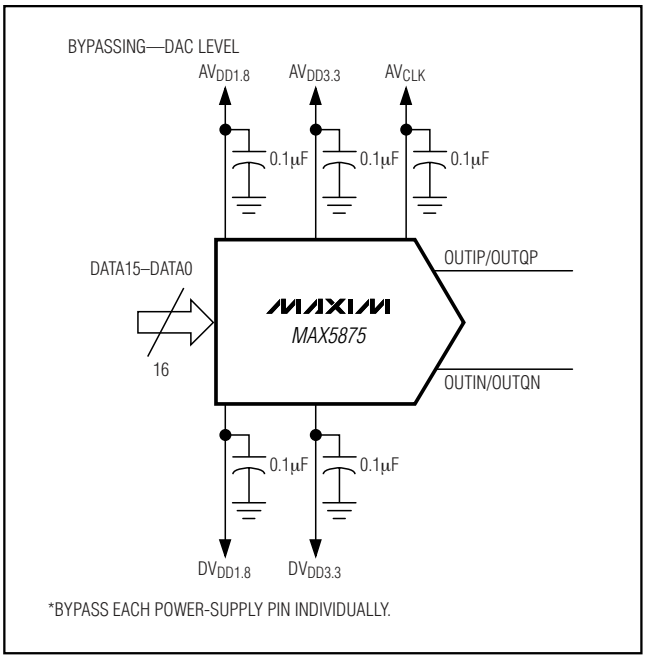


Figure 8. Recommended Power-Supply Decoupling and Bypassing Circuitry

The data converter die attaches to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PCB side of the package. This allows for a solid attachment of the package to the PCB with standard infrared reflow (IR) soldering techniques. A specially created land pattern on the PCB, matching the size of the EP (6mm x 6mm), ensures the proper attachment and grounding of the DAC. Refer to the MAX5875 EV kit data sheet. Designing vias into the land area and implementing large ground planes in the PCB design allow for the highest performance operation of the DAC. Use an array of at least 4 x 4 vias (≤ 0.3mm diameter per via hole and 1.2mm pitch between via holes) for this 68-pin QFN-EP package. **Connect the MAX5875 exposed paddle to GND.** Vias connect the land pattern to internal or external copper planes. Use as many vias as possible to the ground plane to minimize inductance.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum can be derived from the DAC's resolution (N bits):

$$SNR = 6.02 \times N + 1.76$$

However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading; therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next-largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Two-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD product(s) to either output tone.

Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (W-CDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

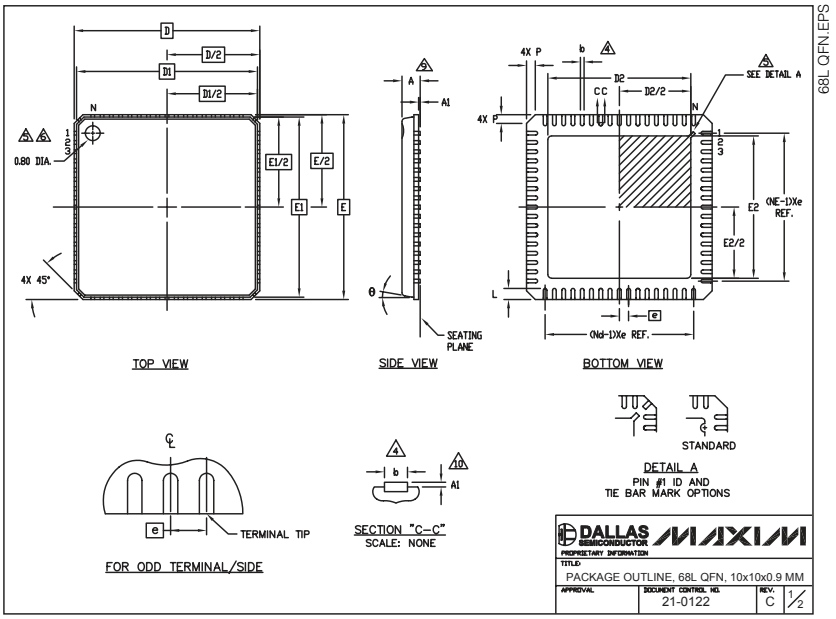
Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV•s.

16-Bit, 200Msps, High-Dynamic-Performance, Dual DAC with CMOS Inputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR
PROPRIETARY INFORMATION
MAXIM
TITLE:
PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0122
REV.
C
1/2

Revision History

Pages changed at Rev 2: 1–16

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