User's Guide

Using the TPSM5601R5H-IBB-EVM

ABSTRACT

The TPSM5601R5H-IBB-EVM features the TPSM5601R5H synchronous-buck power module configured in an inverting-buck-boost (IBB) topology, which results in the output voltage being inverted (negative output). The negative output voltage is set to one of five common values by using a configuration jumper. In an IBB configuration, the input voltage range and maximum output current is reduced due to the shift in topology. Therefore, it is important to note that the maximum output current the EVM can supply changes with respect to operating conditions. Input and output capacitors are included to accommodate the allowable range of input voltage and the selectable output voltages on the EVM. The EVM also provides additional level-shifting circuitry for the enable (EN) and power good (PGOOD) pins to alleviate any problems associated with the offset voltages. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response
- Frequency response

Control test points and jumpers are provided for use of the enable (EN) and power-good (PGOOD) level-shifting features of the device. The recommended PCB layout of the EVM maximizes thermal performance and minimizes output ripple and noise.

Table of Contents

1 EVM Setup 2
2 EVM Connectors and Test Points 3
3 EVM Parameters 4
3.1 Maximum Output Current 4
3.2 Maximum V_{IN} and V_{OUT} Configurations 4
3.3 Switching Node Behavior 4
4 Typical Performance 5
4.1 Typical Characteristics (V_{IN} = 12 V) 5
4.2 Typical Characteristics (V_{IN} = 24 V) 6
4.3 Typical Characteristics (V_{IN} = 36 V) 7
4.4 Typical Characteristics (V_{IN} = 48 V) 8
5 Feature Description 9
5.1 Enable Pin (EN) 9
5.2 Power-Good Pin (PGOOD) 10
5.3 System Loop Stability 11
6 Layout 12
6.1 PCB Layout 12
7 Schematic 15
8 Bill of Materials (BOM) 16
Device Support 17
Related Documentation 17
Support Resources 17

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1 EVM Setup

Figure 1-1 highlights the user interface items associated with the EVM. The VIN Power terminal block (J1) is used for connection to the host input supply and the –VOUT Power terminal block (J4) is used for connection to the load. These terminal blocks accept up to a 16-AWG wire.

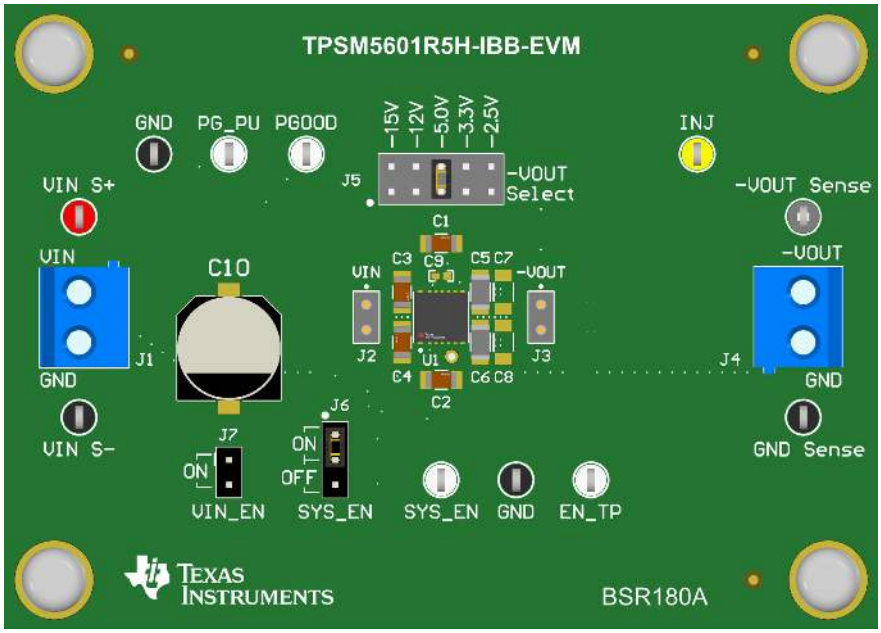


Figure 1-1. EVM User Interface

- Use the VIN S+ and VIN S– test points along with the –VOUT Sense and GND Sense test points located near the power terminal blocks as voltage monitoring points where voltmeters can be connected to measure VIN and –VOUT. *Do not use the monitoring test points as the input supply or output load connection points*. The PCB traces connecting to these test points are not designed to support high currents.
- Use the VIN scope test points (J2) and –VOUT scope test points (J3) to monitor VIN and –VOUT waveforms with an oscilloscope. Use these jumpers with the tip-and-barrel method. The two sockets of each test point are on 0.1-in centers. Connect the scope probe tip to the upper socket pin labeled "•" and connect the scope ground lead to the lower socket pin.
- The control test points located near the bottom and top left of the EVM test the features of the device. Refer to Table 2-1 for more information on the individual control test points.
- The –VOUT Select jumper (J5) is provided to select the desired negative output voltage:
  - –2.5 V
  - –3.3 V
  - –5 V
  - –12 V
  - –15 V

  Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.
- The device can be turned on or off using the system enable (SYS_EN) jumper (J6). Place the jumper in the ON position to enable the device or in the OFF position to disable the device. If the jumper is left open, the EVM will default to the OFF state. The undervoltage lockout (UVLO) can be set by populating resistors R8 and R9 located on the bottom side of the EVM. If the ENABLE/UVLO feature is not needed, remove resistor R9 from the board and place the jumper on the VIN_EN jumper (J7).
- The power good (PGOOD) test point is available to monitor when a valid output voltage is present on the EVM. Additionally, the PG_PU pin is present as a convenient point to connect a pullup voltage for the PGOOD signal.
- The frequency response test point (INJ) along with the –VOUT Sense test point is available to inject a sinusoidal signal into the system and measure the gain/phase response characteristics of the device.

2 EVM Connectors and Test Points

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. Table 2-1 describes each test point.

Table 2-1. Test Point Descriptions

TEST POINT(1)	DESCRIPTION
VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point to measure efficiency.
VIN S–	Input ground monitor. Connect the negative lead of a DVM to this point to measure efficiency.
–VOUT Sense	Negative output voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
GND Sense	Output ground monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
GND	System ground test points
VIN Scope (J2)	Input voltage scope monitor. Connect an oscilloscope probe to this set of points to measure input ripple voltage.
–VOUT Scope (J3)	Negative output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure negative output voltage ripple and transient response.
SYS_EN (J6)	System enable select jumper. Use the control header (J6) to enable or disable the device using a jumper. The SYS_EN test point is connected to the level-shifting circuitry to activate the enable circuit. A minimum supply voltage of 5 V on the SYS_EN test point is required to turn on the enable circuitry. *Do not exceed 20 V on this test point.* Failing to adhere to these constraints can result in damaged components. To monitor the enable signal, monitor the EN_TP testpoint.
VIN_EN (J7)	Enable tied to the VIN jumper. The enable pin is tied directly to VIN, which allows the device to start up when VIN is within its valid operating range. The enable test point (EN_TP) is connected directly to the enable pin of the device to monitor the enable signal. Do not connect this test point to ground or any other signal. If enable/disable feature is desired, then use the system enable select jumper (J6).
PGOOD	Power-good test point. Monitors the power-good signal of the device. A level-shifting circuitry is implemented on the EVM to allow a proper reading state of the pin.
PG_PU	PGOOD pullup test point. Apply 5 V to this pin or any other DC voltage less than 18 V to use as a pullup voltage for the PGOOD signal. A pullup resistor and level-shifting circuitry is implemented on the EVM for proper utilization.
INJ	Frequency response test point. Inject a sinusoidal signal to this test point (system) to measure the gain and phase response characterstocs of the device.

(1) Refer to the product data sheet for absolute maximum ratings associated with the features in this table.

3 EVM Parameters

3.1 Maximum Output Current

In IBB configuration, the inductor current and peak switching currents are larger than in the equivalent buck converter. Consequently, the output current capability in the IBB topology is less than the buck configuration for the same current limit specifications.

Figure 3-1 provides a general idea of the recommended maximum output current from the TPSM5601R5H-IBB-EVM.

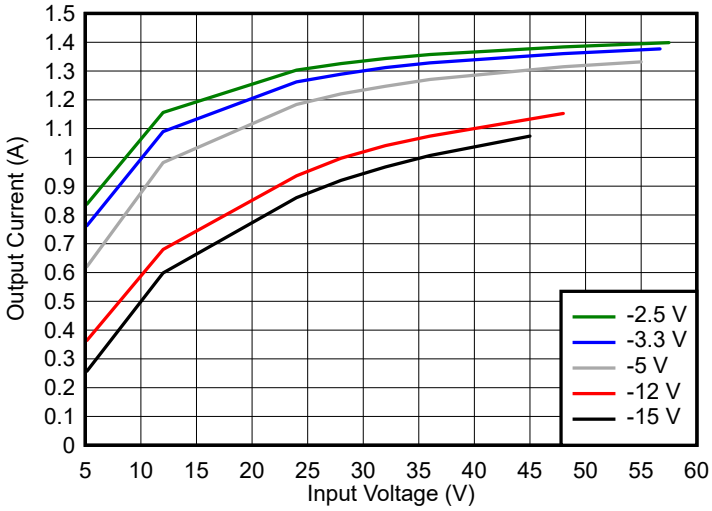


Figure 3-1. Recommended Maximum Output Current

3.2 Maximum V_{IN} and V_{OUT} Configurations

In an IBB topology, the voltage across the device is equal to the input voltage plus the negative output voltage. As a result, the input voltage range is reduced. Make sure to keep this voltage less than the specified maximum input voltage (V_{IN_MAX}) of the device. Refer to the product data sheet for absolute maximum ratings.

3.3 Switching Node Behavior

The voltage on the switch node switches from the input voltage to the negative output voltage in an inverting topology. During start-up, V_{IN} rises to achieve the set input voltage, then the device begins switching, which causes the V_{OUT} to start ramping down after the enable pin voltage exceeds its threshold and V_{IN} exceeds its UVLO threshold. As V_{OUT} continues to ramp down, the switch node low-level follows V_{OUT} downward. Figure 3-2 displays a typical behavior of the switch node at start-up.

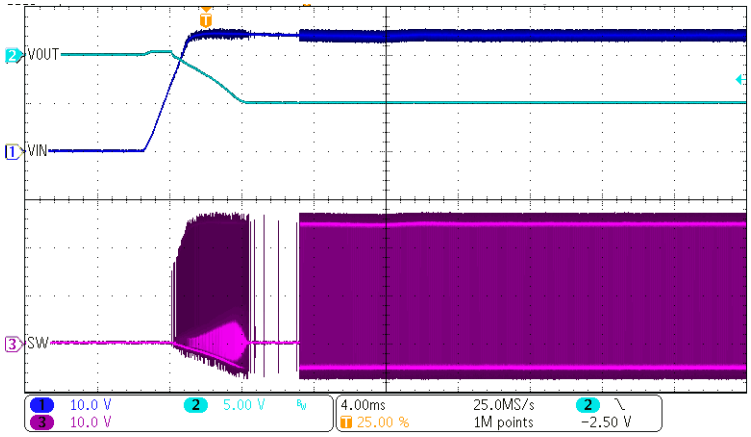


Figure 3-2. Switch Node Voltage During Start-Up

4 Typical Performance

4.1 Typical Characteristics (V_{IN} = 12 V)

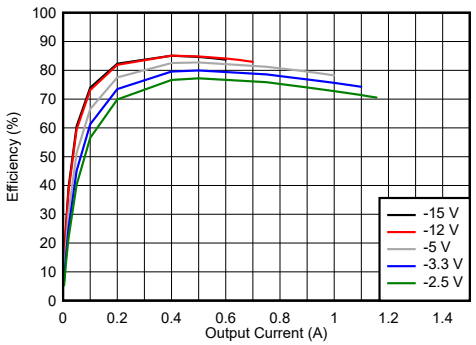


Figure 4-1. Efficiency

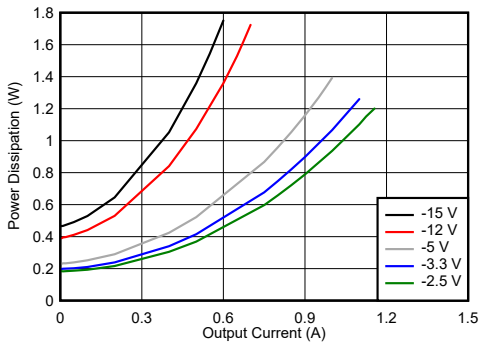


Figure 4-2. Power Dissipation

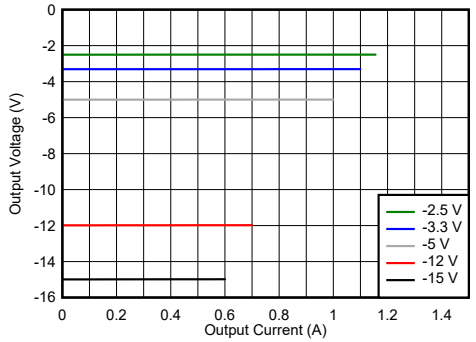


Figure 4-3. Load Regulation

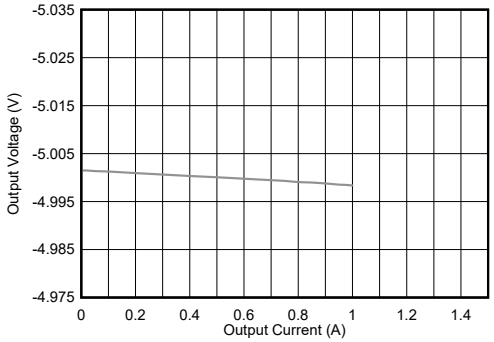
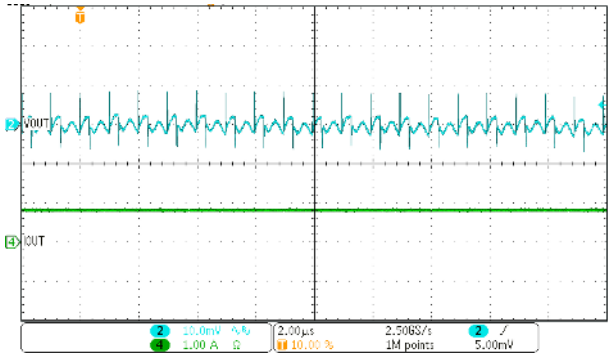
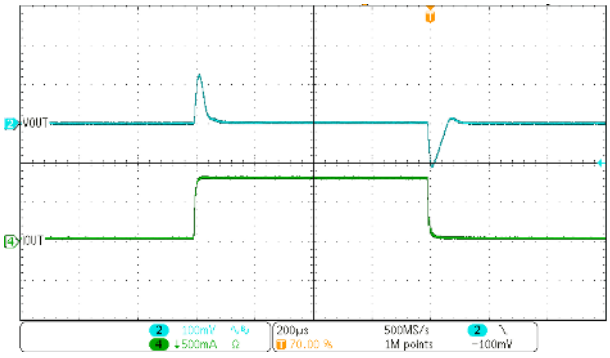


Figure 4-4. Load Regulation (V_{OUT} = –5 V)



V_{OUT} = –5 V I_{OUT} = 750 mA

Figure 4-5. Output Ripple Waveform



V_{OUT} = –5 V 750-mA Load Step

Figure 4-6. Transient Repsonse Waveform

4.2 Typical Characteristics (V_{IN} = 24 V)

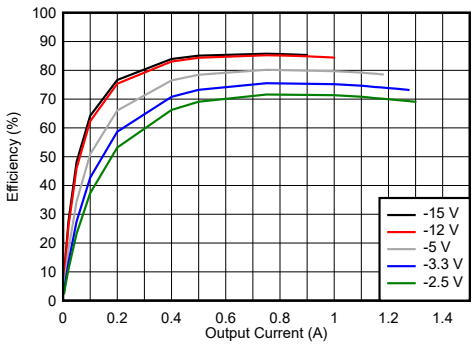


Figure 4-7. Efficiency

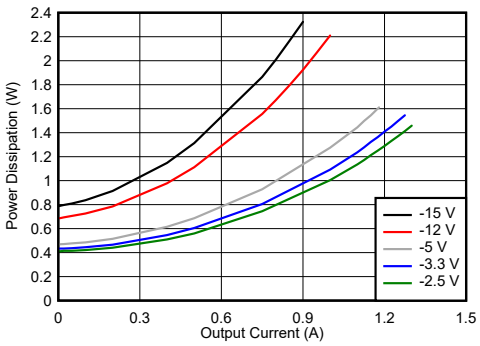


Figure 4-8. Power Dissipation

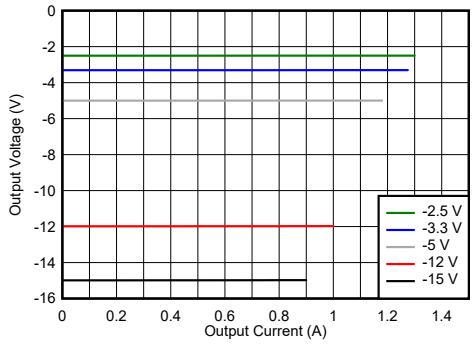


Figure 4-9. Load Regulation

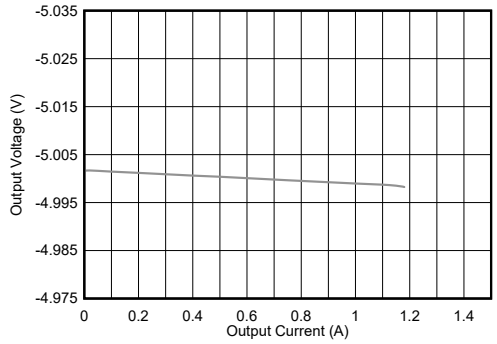
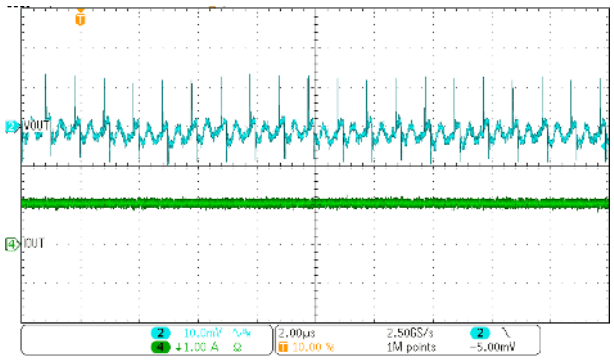
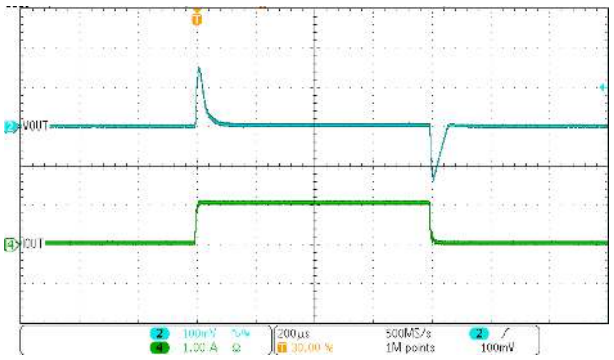


Figure 4-10. Load Regulation (V_{OUT} = –5 V)



V_{OUT} = –5 V I_{OUT} = 1 A

Figure 4-11. Output Ripple Waveform



V_{OUT} = –5 V 1-A Load Step

Figure 4-12. Transient Response Waveform

4.3 Typical Characteristics (V_{IN} = 36 V)

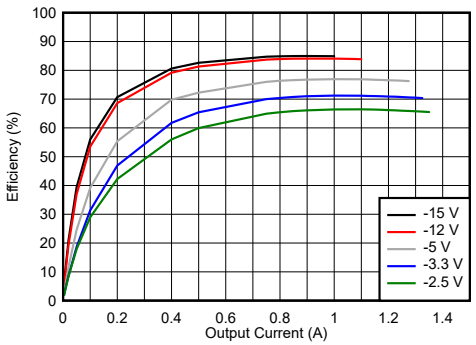


Figure 4-13. Efficiency

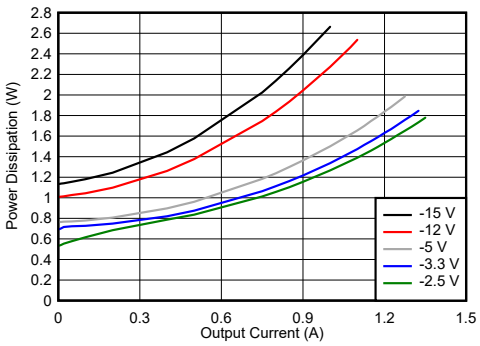


Figure 4-14. Power Dissipation

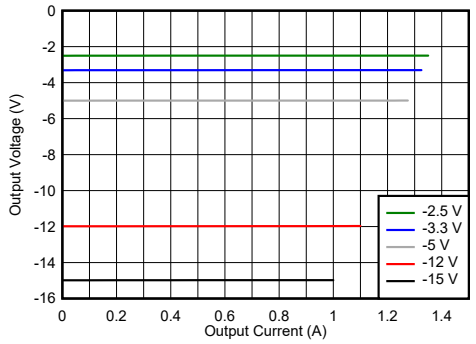


Figure 4-15. Load Regulation

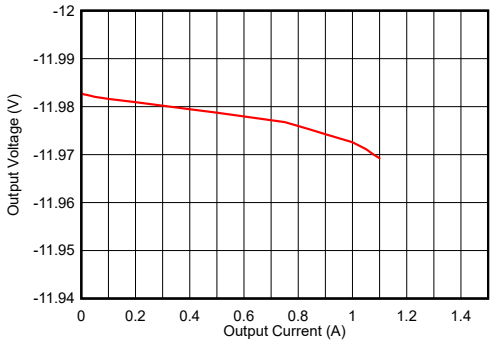
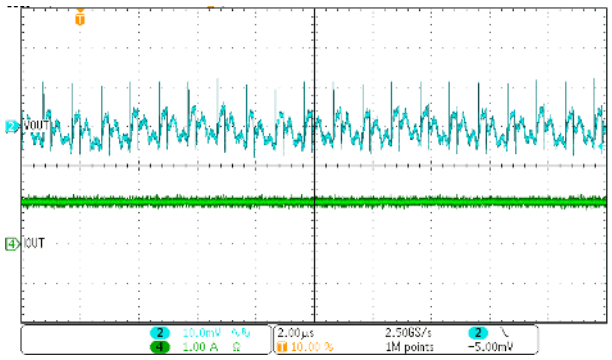
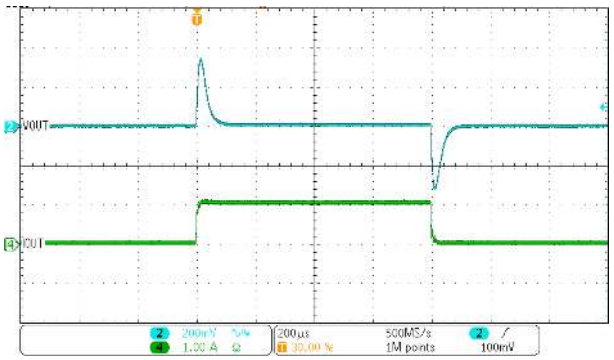


Figure 4-16. Load Regulation (V_{OUT} = –12 V)



V_{OUT} = –12 V I_{OUT} = 1.0 A

Figure 4-17. Output Ripple Waveform



V_{OUT} = –12 V 1-A Load Step

Figure 4-18. Transient Response Waveform

4.4 Typical Characteristics (V_{IN} = 48 V)

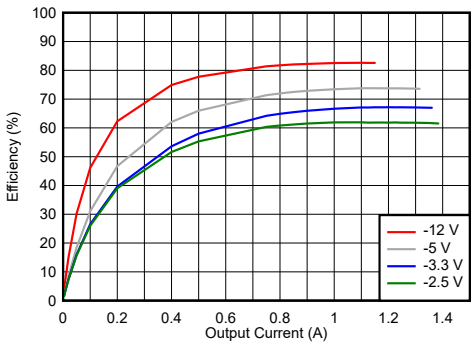


Figure 4-19. Efficiency

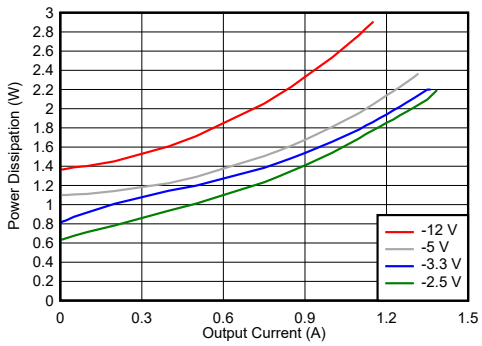


Figure 4-20. Power Dissipation

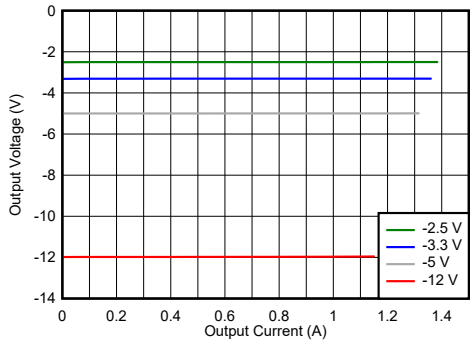


Figure 4-21. Load Regulation

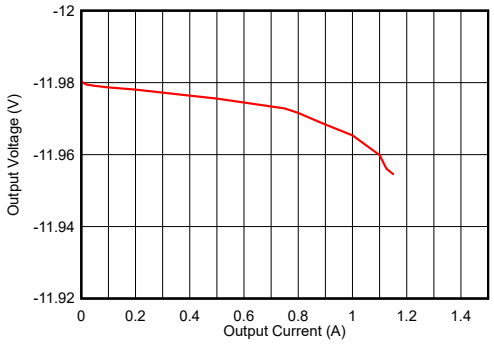
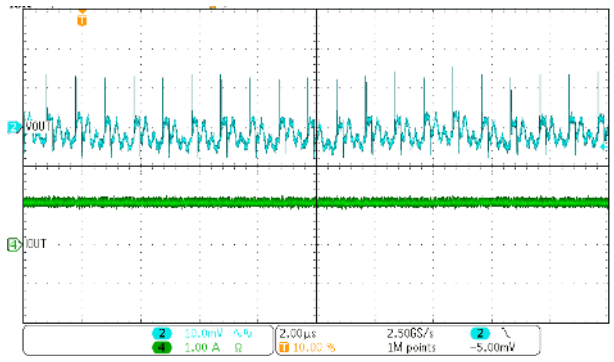
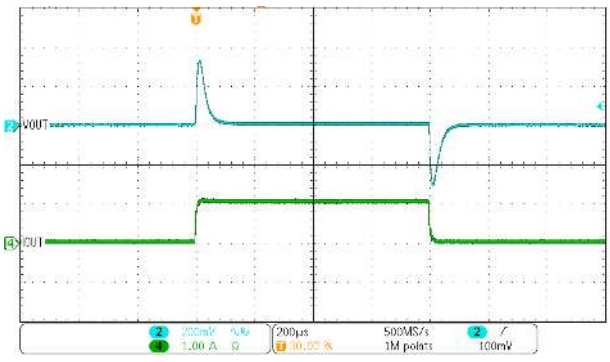


Figure 4-22. Load Regulation (V_{OUT} = –12 V)



V_{OUT} = –12 V I_{OUT} = 1.0 A

Figure 4-23. Output Ripple Waveform



V_{OUT} = –12 V 1-A Load Step

Figure 4-24. Transient Response Waveform

5 Feature Description

5.1 Enable Pin (EN)

In an IBB configuration, the enable voltage thresholds are referenced to –VOUT instead of GND as in a typical non-inverting buck. This behavior can cause difficulties enabling or disabling the device. Therefore, the TPSM5601R5H-IBB-EVM includes a level-shifting circuitry (Figure 5-1) to alleviate any problems associated with the offset EN threshold voltages. This eliminates the need for negative EN signals. If the enable/disable feature is not needed, then remove resistor R9 located on the bottom side of the EVM and place the jumper on VIN_EN jumper (J7). For a deeper understanding of the EN level-shifting circuitry, see the *Inverting Application for the TPSM5601R5H Application Report*.

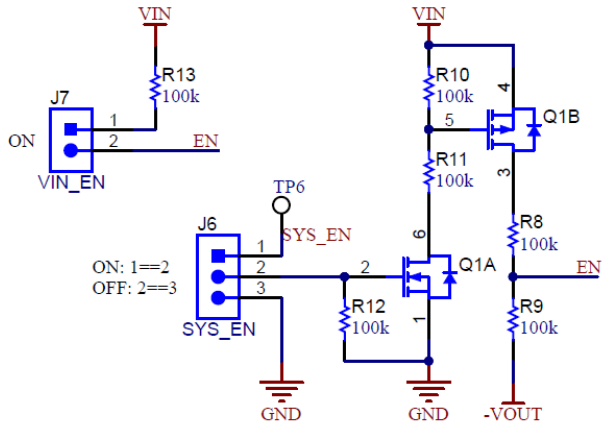


Figure 5-1. Enable Level-Shifter

The following are connection steps required to use enable/disable level-shifting circuitry:

1. Place a jumper on the control header (J6) for desired function ON or OFF.
2. Apply a minimum DC votlage of 5 V on the SYS_EN testpoint. *Do not exceed 20 V on this test point.*

Figure 5-2 and Figure 5-3 demonstrate a typical start-up and shutdown behavior when using the enable level-shifting circuitry.

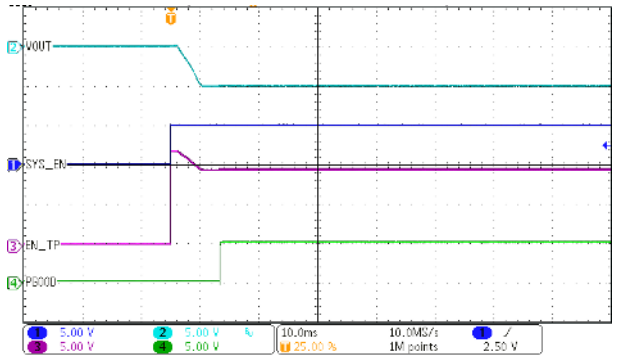


Figure 5-2. Enable Turn-On on V_{IN} = 24 V

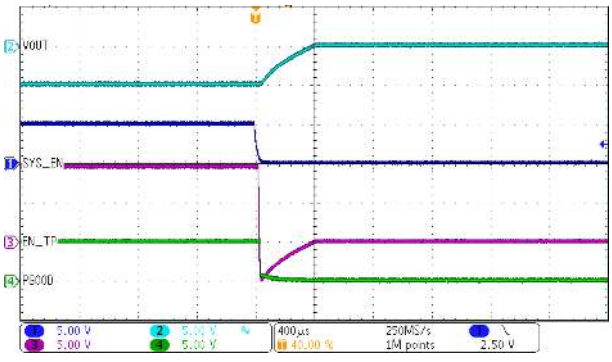


Figure 5-3. Enable Turn-Off on V_{IN} = 24 V

5.2 Power-Good Pin (PGOOD)

The TPSM5601R5H-IBB-EVM has PGOOD level-shifting circuitry (Figure 5-4) integrated to alleviate any problems associated with the offset PGOOD pin voltages by translating the negative output signals of the PGOOD pin. Figure 5-5 demonstrates the typical behavior of the PGOOD signal with the additional level-shifiting circuitry. For a deeper understanding of the PGOOD level-shifting circuitry, see the *Inverting Application for the TPSM5601R5H Application Report*.

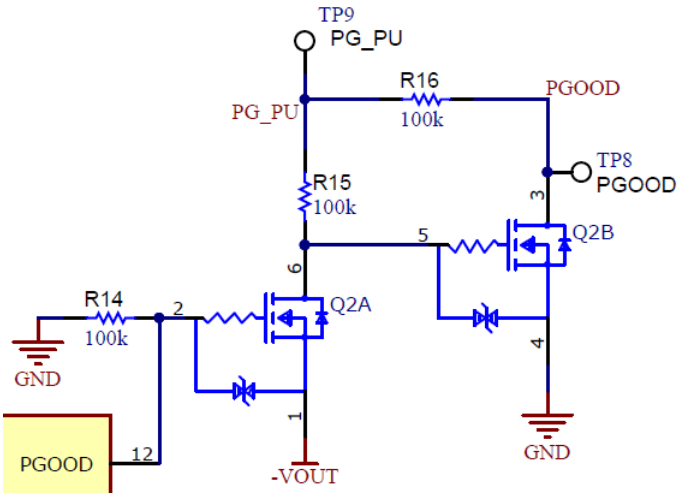


Figure 5-4. PGOOD Level-Shifter

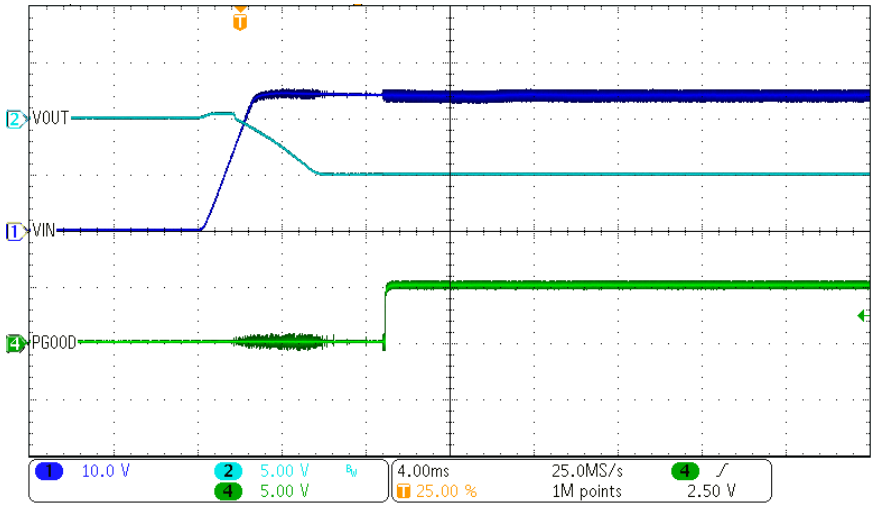


Figure 5-5. PGOOD Signal

5.3 System Loop Stability

Stability is an important factor in power converters. The guideline for a stable design is a phase margin of at least 45°. With that in mind, the TPSM5601R5H-IBB-EVM is designed to accommodate a wide range of operating conditions with a phase margin greater than 45°. Note that the stability of the system (EVM) will be affected by the operating conditions, input voltage, and total output capacitance. Figure 5-6 demonstrates the recommended operating range for a stable design (≥ 45°). If the operating conditions are outside the recommended range, it is important to run a bode plot to ensure stability.

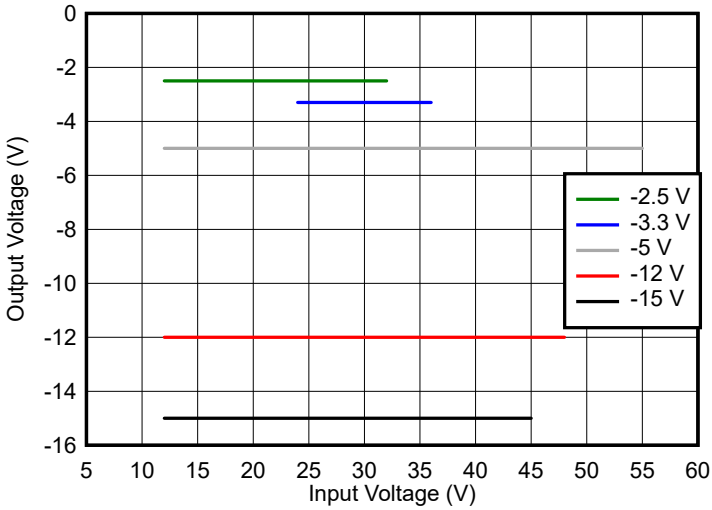


Figure 5-6. Recommended Operating Range for ≥ 45° Phase Margin

Table 5-1 shows the phase margin across various input voltages with a fixed –5-V output. The results measured are from the original BOM (C_{OUT} = 2 × 47 µF) of the TPSM5601R5H-IBB-EVM.

Table 5-1. Stability Analysis of TPSM5601R5H-IBB-EVM

V_{IN} (V)	V_{OUT} (V)	Max I_{OUT} (A)	$F_{crossover}$ (kHz)	PHASE MARGIN (°)
12	–5	0.982	18.00	45.0
24	–5	1.184	23.30	50.8
28	–5	1.221	24.32	51.7
36	–5	1.271	26.00	53.2
48	–5	1.315	27.40	54.3

6 Layout

6.1 PCB Layout

Figure 6-1 through Figure 6-6 show the EVM PCB layout images.

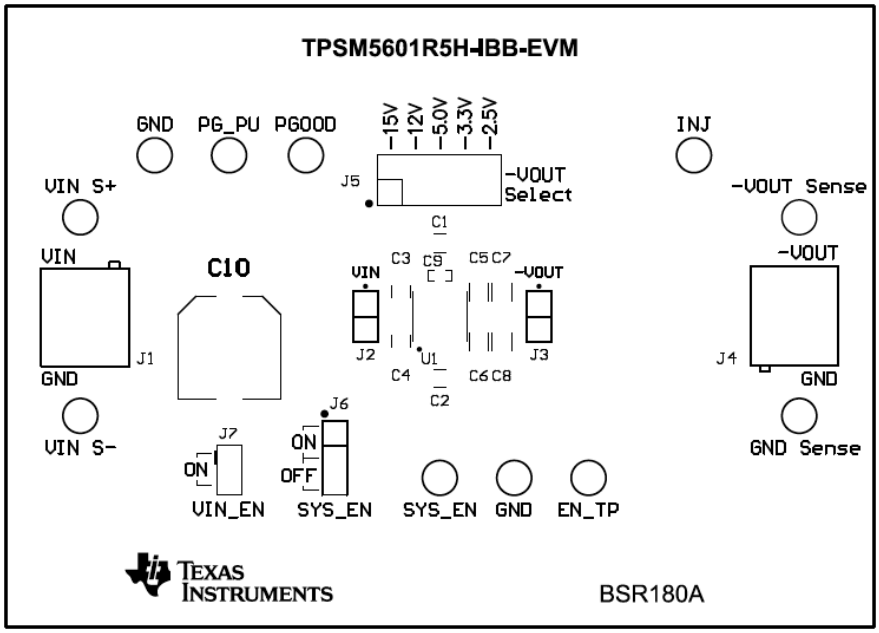


Figure 6-1. Top Silk Screen (Top View)

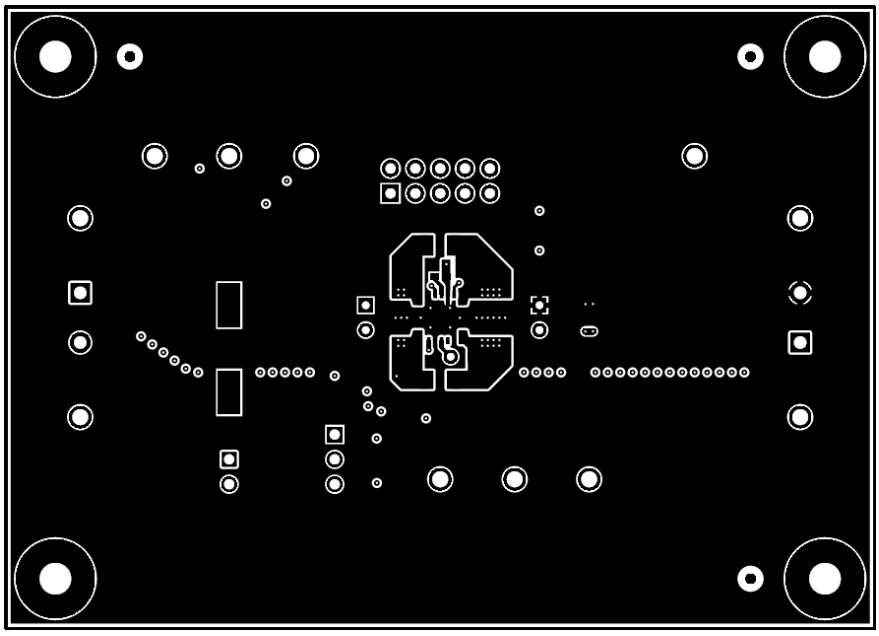


Figure 6-2. Top Copper Layer

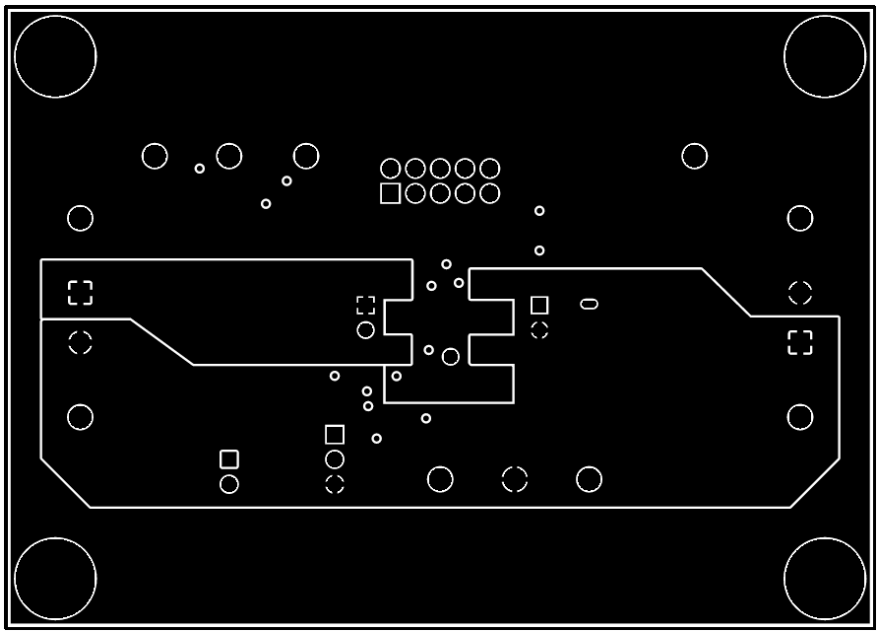


Figure 6-3. Signal Layer 1

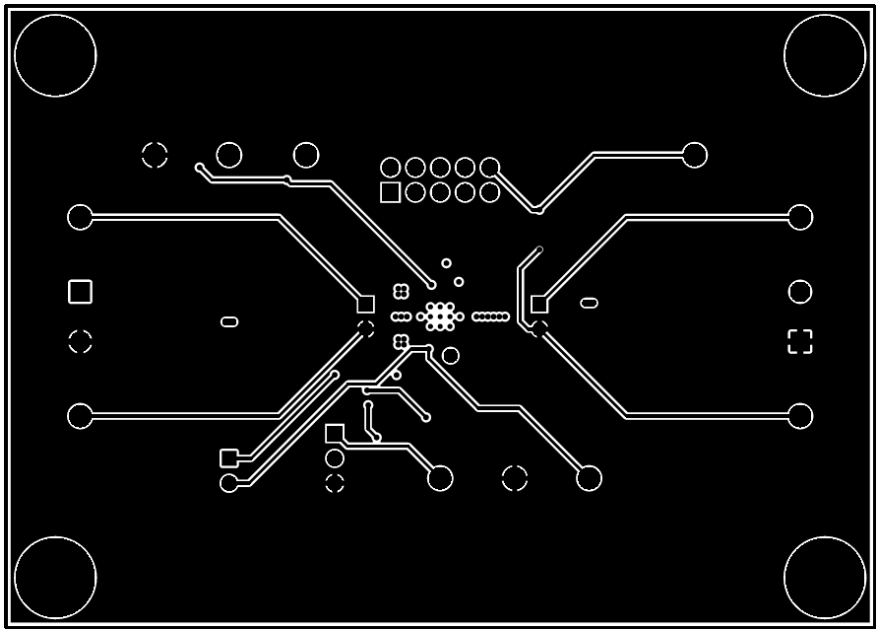


Figure 6-4. Signal Layer 2

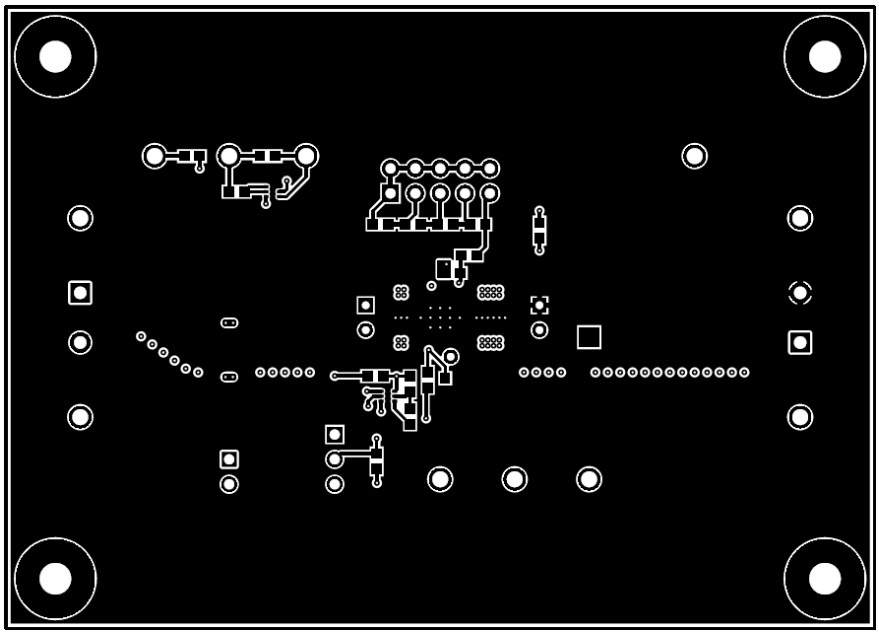


Figure 6-5. Bottom Layer

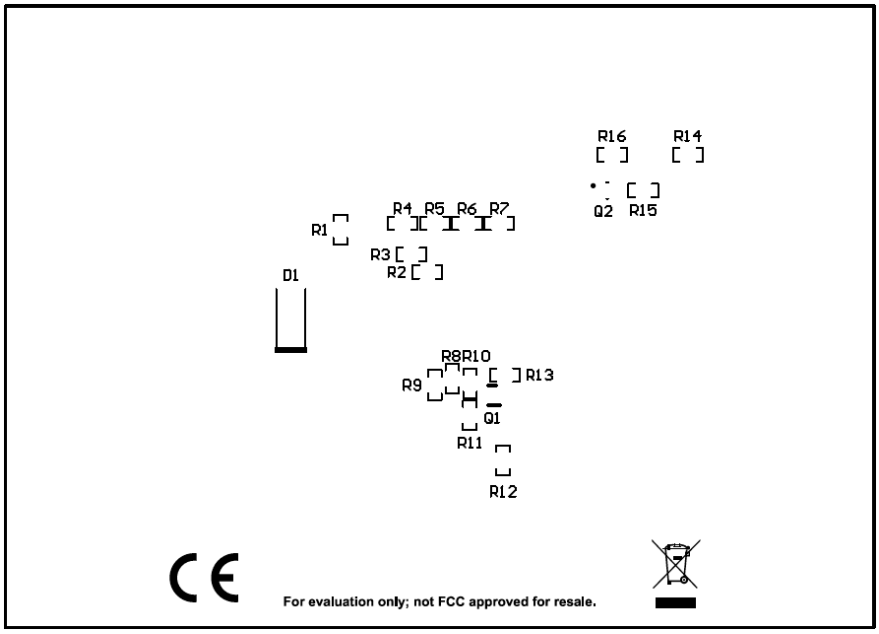


Figure 6-6. Bottom Layer Silk Screen (Bottom View)

7 Schematic

Figure 7-1 illustrates the TPSM5601R5H-IBB-EVM schematic.

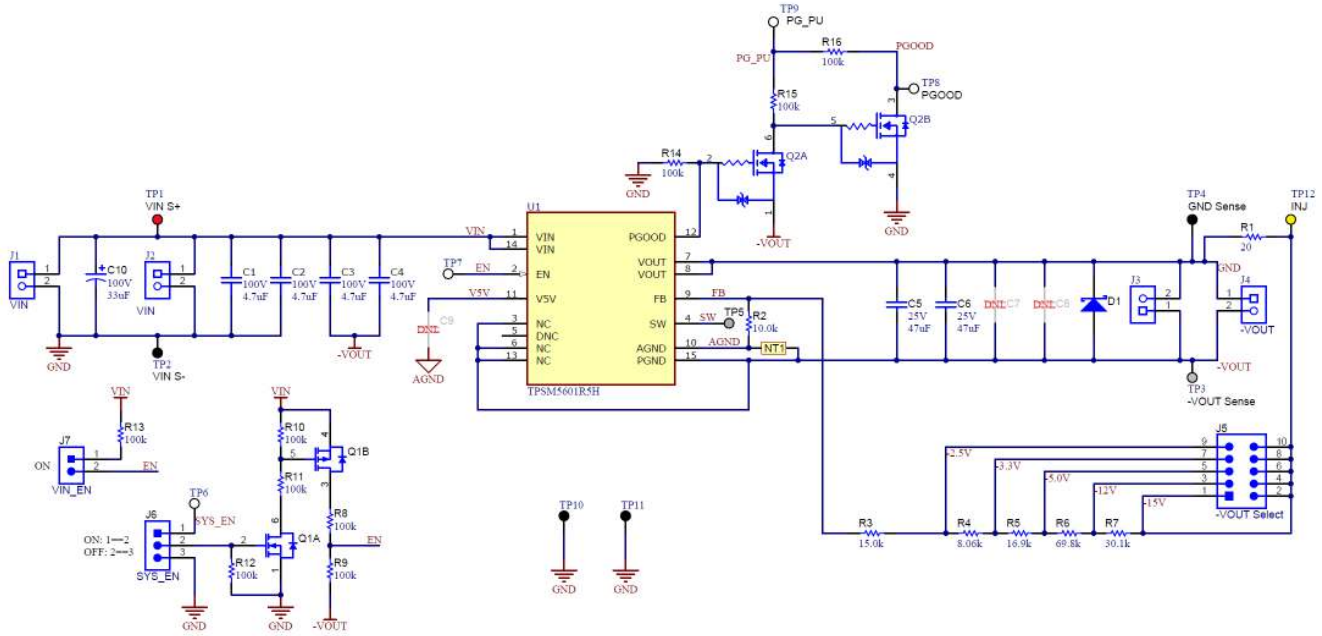


Figure 7-1. TPSM5601R5H-IBB-EVM Schematic

8 Bill of Materials (BOM)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER
C1, C2, C3, C4	4	4.7 µF	4.7-µF, ±10%, 100-V Ceramic Capacitor X7S	1206	GRM31CC72A475KE11L
C5, C6	2	47 µF	CAP, CERM, 47 µF, 25 V, ±20%, X5R	1206_190	C3216X5R1E476M160AC
C10	1	33 µF	CAP, AL, 33 µF, 100 V, ±20%, SMD	JA0	EMVE101ADA330MJA0G
D1	1	20 V	Diode, Schottky, 20 V, 3 A	SMA	B320A-13-F
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 × 1/4, Nylon	Screw	NY PMS 440 0025 PH
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C
J1, J4	2		Terminal Block, Brass, TH	2 × 1 5.08 mm	ED120/2DS
J2, J3	2		Socket Strip, Black, Tin, TH	100 mil, 2 pin	310-43-102-41-001000
J5	1		Header, Tin, TH	5 × 2, 100 mil	PEC05DAAN
J6	1		Header, Tin, TH	3 PIN, 100 mil	PEC03SAAN
J7	1		Header, Tin, TH	2 PIN, 100 mil	PEC02SAAN
Q1	1	60 V	MOSFET, 2-CH, N/P-CH, 60 V, 0.305 A	SOT-563	SI1029X-T1-GE3
Q2	1		Mosfet Array 2 N-Channel (Dual) 30-V, 100-mA, 150-mW, Surface Mount ES6	SOT-563	SSM6N44FE,LM
R1	1	20	RES, 20, 5%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060320R0JNEA
R2	1	10.0 k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060310K0FKEA
R3	1	15.0 k	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060315K0FKEA
R4	1	8.06 k	RES, 8.06 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW06038K06FKEA
R5	1	16.9 k	RES, 16.9 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060316K9FKEA
R6	1	69.8 k	RES, 69.8 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060369K8FKEA
R7	1	30.1 k	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0	0603	CRCW060330K1FKEA
R8, R9, R10, R11, R12, R13, R14, R15, R16	9	100 k	RES, 100 k, 0.1%, 0.1 W, AEC-Q200 Grade 1	0603	TNPW0603100KBEEA
SH-J5, SH-J6	2	1 × 2	Shunt, 2 mm, Gold plated, Black	2-mm Shunt	2SN-BK-G
TP1	1		Test Point, Multipurpose, Red, TH	Testpoint	5010
TP2, TP4, TP10, TP11	4		Test Point, Multipurpose, Black, TH	Testpoint	5011
TP3	1		Test Point, Multipurpose, Grey, TH	Testpoint	5128
TP6, TP7, TP8, TP9	4		Test Point, Multipurpose, White, TH	Testpoint	5012
TP12	1		Test Point, Multipurpose, Yellow, TH	Testpoint	5014
U1	1		60-V Input, 1-V to 16-V Output, 1.5-A Power Module	B3QFN	TPSM5601R5H
C7, C8	0			1206	C3216X5R1E476M160AC
C9	0			0402	EMK105BJ105KVHF

Device Support

Related Documentation

- Texas Instruments, *TPSM5601R5H Product Data Sheet*
- Texas Instruments, *Inverting Application for the TPSM5601R5H Application Report*

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265