Micro Linear

ML4815

Zero Voltage Switching Resonant Controller

GENERAL DESCRIPTION

The ML4815 is designed to facilitate zero-voltage switched (ZVS) resonant converters requiring constant off-time and variable on-time control. Since the power MOSFET is turned on at zero voltage in ZVS resonant converters, power dissipation due to charge-dumping of the MOSFET drain-source capacitance is eliminated, allowing high frequency operation and power density to be maximized. MOSFET parasitic drain-source capacitance can also be used as part of the resonant circuit, minimizing component count.

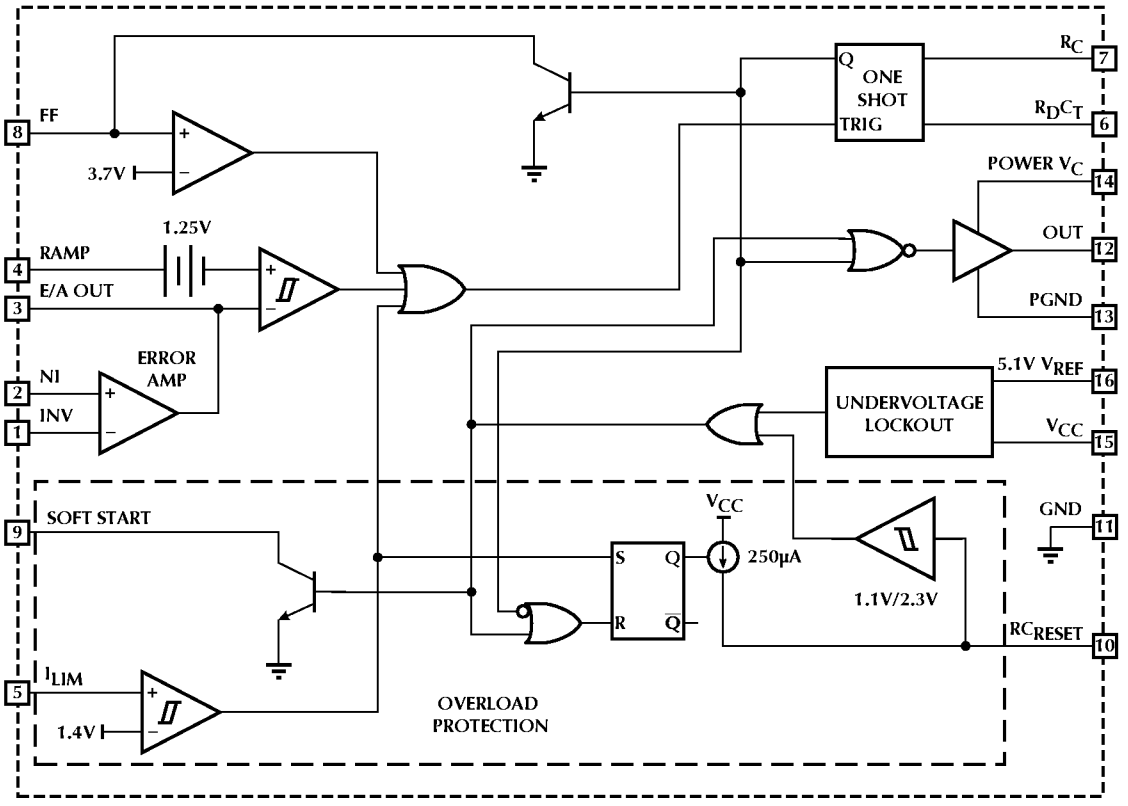
The ML4815 features a monostable multivibrator for precise off-time setting. The on-time is modulated through a ramp comparator in a manner similar to PWM converters. Either current mode control with maximum on-time clamp, or voltage mode control with input feedforward, can be selected.

ML4815 supports pulse-by-pulse (peak) current limiting as well as "hiccup" mode for fault protection. The controller is designed for operation up to 2MHz. The ML4815 also includes a wide band error amplifier, and a high peak current output driver which minimizes cross-conduction current.

FEATURES

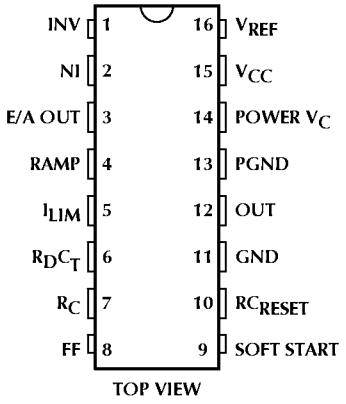
- Supports single-switch ZVS resonant topology with minimal external components ideal for simple, high density DC to DC converters
- Small converter frequency variation from no-load to full-load
- High current (2A peak) totem-pole output drive with low cross conduction
- Precision buffered 5.1V reference (±2%)
- Wideband (5.5MHz), high slew rate (12V/µs) error amp
- Undervoltage lockout with low current start-up
- Integrating fault detection/soft-start reset

BLOCK DIAGRAM (Pin Configuration Shown is for DIP Version)



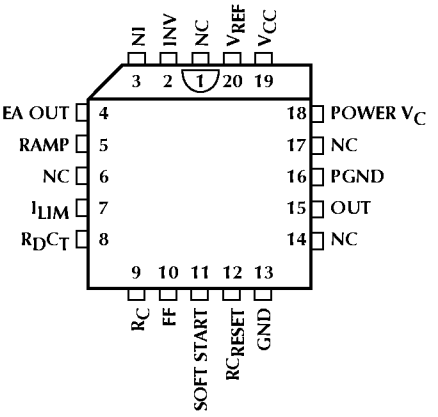
PIN CONFIGURATION

ML4815
16-Pin PDIP (P16)



TOP VIEW

ML4815
20-Pin PLCC (Q20)



TOP VIEW

PIN DESCRIPTION (Pin Number in Parentheses is for PLCC Version)

PIN	NAME	FUNCTION
1 (2)	INV	Inverting input to error amp
2 (3)	NI	Non-inverting input to error amp
3 (4)	E/A OUT	Output of error amplifier and input to main comparator
4 (5)	RAMP	Non-inverting input to main comparator. Connected to FF for feedforward voltage-mode control or to I_{LIM} for current-mode control.
5 (7)	I_{LIM}	Current limit sense pin. Normally connected to current sense resistor.
6 (8)	R_DC_T	External RC network input for setting one-shot off-time
7 (9)	R_C	External resistor input for modifying charge time of R_DC_T
8 (10)	FF	Capacitor to generate feedforward ramp
9 (11)	SOFT START	External RC network input for setting soft start time
10 (12)	RC_{RESET}	External RC network input for overcurrent integration and restart delay time
11 (13)	GND	Analog signal ground
12 (15)	OUT	High current totem-pole output
13 (16)	PGND	Return path for OUT
14 (18)	POWER V_C	Positive Supply for OUT
15 (19)	V_{CC}	Positive supply input
16 (20)	V_{REF}	Buffered output for the 5.1V reference

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} 30V
Output Current, Source or Sink
  DC 0.5A
  Pulsed (0.5µs) 2A
Analog Inputs ..... –0.3V to 6V
Error Amplifier Output Current ..... –5µA
Soft Start Sink Current 100µA
Feedforward Sink Current 800mA
C_T Charging Current ..... –50mA
Junction Temperature 125ºC
Storage Temperature Range ..... –65ºC to 150ºC
Lead Temperature (Soldering, 10 sec) 260ºC
Thermal Resistance (θ_{JA})
  Plastic DIP 65ºC/W
  Plastic Leaded Chip Carrier (PLCC) 60ºC/W

OPERATING CONDITIONS

Temperature Range ..... 0ºC to 70ºC

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, C_T = 330pF, R_C = 100Ω, R_D = 2kΩ, V_{CC} = 15V, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF}	Output Voltage	T_A = 25°C, I_O = 1mA	5.0	5.1	5.2	V
	Line Regulation	T_A = 25°C, 10V < V_{CC} < 30V		2	20	mV/V
	Load Regulation	T_A = 25°C, 1mA < I_O < 10mA		5	20	mV/V
	Temperature Stability	–55°C. < T_J < 125°C.		0.2	0.4	%
	Total Variation	Line, Load, Temp	4.94		5.25	V
	Output Noise Voltage	10Hz to 10kHz		50		µV
	Long Term Stability	1000 Hours		5	25	mV
I_{SC}	Short Circuit Current	V_{REF} = 0V	–15	–50	–100	mA
ERROR AMPLIFIER						
V_{IO}	Input Offset Voltage				20	mV
I_{IB}	Input Bias Current			0.6	3	µA
I_{IO}	Input Offset Current			0.1	1	µA
	Open Loop Gain	1V < V_O < 4V	60	96		dB
	CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
	PSRR 12V < V_{CC} < 25V	12V < V_{CC} < 25V	75	110		dB
I_{SINK}	Output Sink Current	E/A OUT = 1V	1	2.5		mA
I_{SOURCE}	Output Source Current	E/A OUT = 4V	–0.5	–1.3		mA
V_{OH}	Output High Voltage	E/A OUT = 1mA	0	0.5	1.0	V
V_{OL}	Output Low Voltage	E/A OUT = –0.5mA			0.8	V
	Unity Gain Bandwidth		3.0	5.5		MHz
	Slew Rate		6	12		V/µs
RAMP COMPARATOR						
	RAMP Bias Current	R_C = 0		0.7		µA
	E/A OUT Zero DC Threshold	INV = E/A OUT (V), NI = FF = 2V, I_{LIM} = 0V, $R_D C_T$ = 1.5V	1.05	1.20	1.55	V
	Delay to Output	C_L = 0		55		ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT COMPARATOR						
	I_{LIM} Input Bias Current	$0 < V(I_{LIM}) < 4V$		2		µA
	Current Limit Threshold			1.41		V
	Hysteresis			30		mV
	Delay to Output	RC_{RESET} = 0, C_L = 0		50		ns
ONE-SHOT						
	Off-Time Initial Accuracy	T_A = 25ºC, C_L = 0		0.45		µs
	Off-Time Voltage Stability	C_L = 0, 12V < V_{CC} < 25V		5		%
	Off-Time Temperature Stability	C_L = 0		5		%
I_{SC}	Off-Time Total Variation	C_L = 0		6		%
FEEDFORWARD/MAXIMUM ON TIME CLAMP						
	Discharge Current	FF = 2.5V		–250		mA
	Temperature Stability	C_{FF} = 330pF, R_{FF} = 2.7kΩ to V_{REF}, C_L = 0		1.0		µs
SHUTDOWN/RESTART						
	RC_{RESET} Charging Current			–250		µA
	Overload Shutdown Threshold			2.3		V
	Restart Threshold			1.1		V
SOFT START						
	Input Bias Current	FF = 4V		1		µA
	Discharge Current	FF = 1V		25		mA
UNDER VOLTAGE LOCKOUT						
	Start Threshold			13.4		V
	UVLO Hysteresis			3.6		V
OUTPUT						
	Output Low Level	I_{OUT} = 20mA		0.25	0.40	V
		I_{OUT} = 200mA		1.2	2.2	V
	Output High Level	I_{OUT} = –20mA		13.0		V
		I_{OUT} = –200mA		12.7		V
	Rise/Fall Time	C_L = 1nF		30		ns
SUPPLY						
	Short Circuit Current	T_A = 25ºC, V_{OC} = 8V		2	3	mA
	Operating I_{CC}			28	38	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

FUNCTIONAL DESCRIPTION

ML4815 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the ML4815:

1) Use a ground plane

2) Damp or clamp parasitic inductive kick energy from the gate of any driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1A Schottky diode at the output pin will serve this purpose.

3) Bypass V_{CC}, V_C and V_{REF}. Use 1µF monolithic ceramic capacitors with low equivalent series inductance for V_{CC} and V_C. Allow less than 1 cm of total lead length between the bypassed pin and the ground plane for each capacitor.

4) Treat the off-time setting capacitor, C_T, like a bypass capacitor.

CONTROL METHODS

In current-mode control the current transformer output is fed into the RAMP comparator input. The current-sense waveform is used as the on-time modulating ramp. The on-time can be clamped to a maximum by using R_{FF} and C_{FF} as shown.

In feedforward voltage-mode control the on-time modulating ramp is generated with an external capacitor, C_{FF}, from pin FF to ground. C_{FF} is charged through an external resistor, R_{FF}. The maximum on-time is the time taken to charge C_{FF} to 3.7V. Since the charging current depends on V_{IN} the resulting maximum on-time varies with V_{IN}.

OUTPUT SECTION

When driving power MOSFETs with high equivalent gate capacitance (C_G > 3nF) it is advisable to use an external 1N4148 diode between the V_{CC} and V_C pins (Figure 6) to reduce extra power dissipation caused by slow turn-off of Q7. In this case both V_{CC} and V_C pins should have bypass capacitors (C = 1µF) as close as possible to the IC pins.

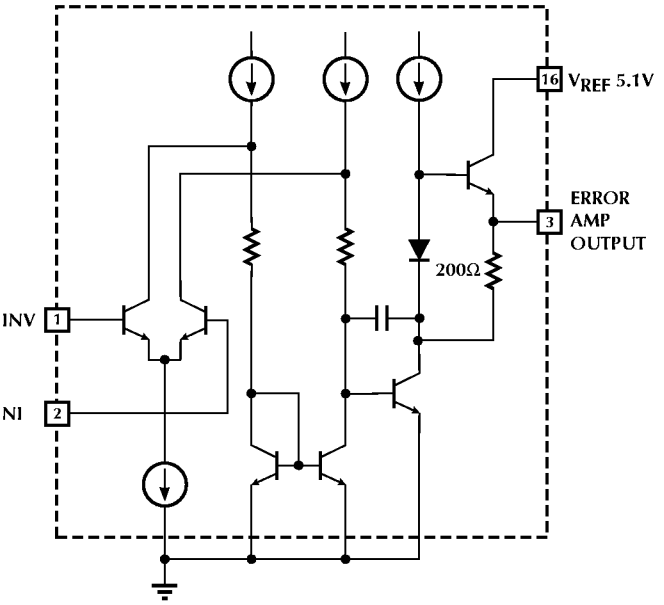


Figure 1. Simplified Schematic of Error Amplifier

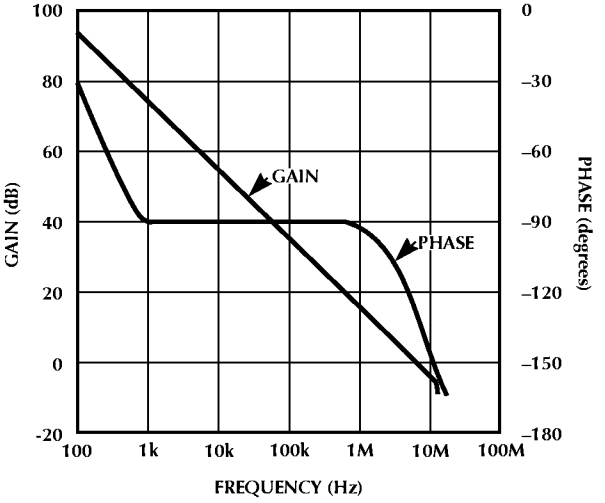


Figure 2. Open Loop Frequency Response

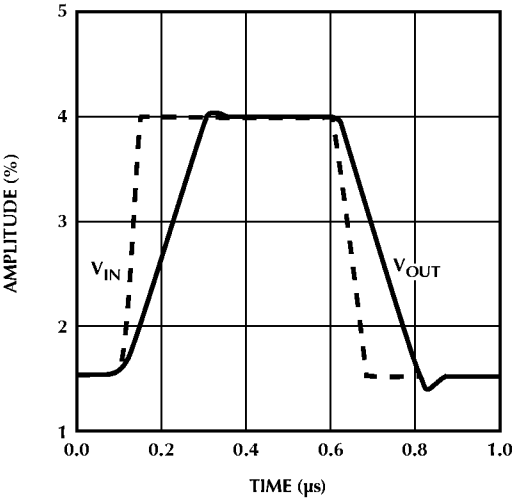


Figure 3. Unity Gain Slew Rate

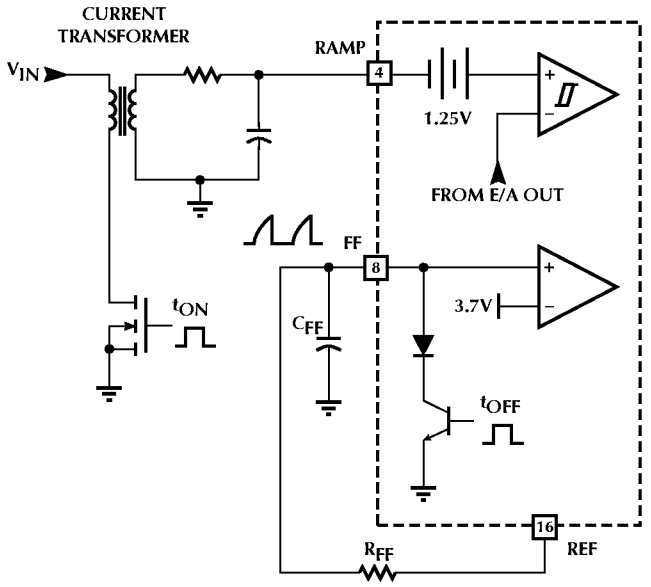


Figure 4. Current Mode Control with Maximum On-Time Clamp

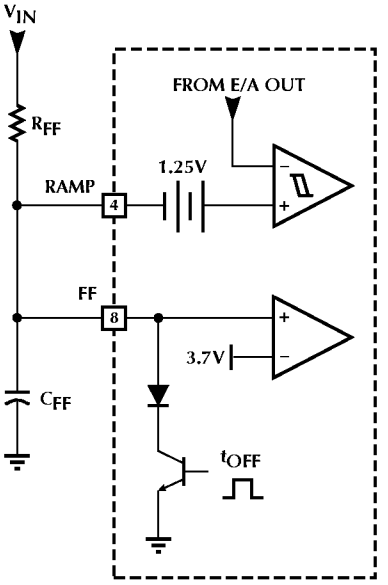


Figure 5. Feedforward Control

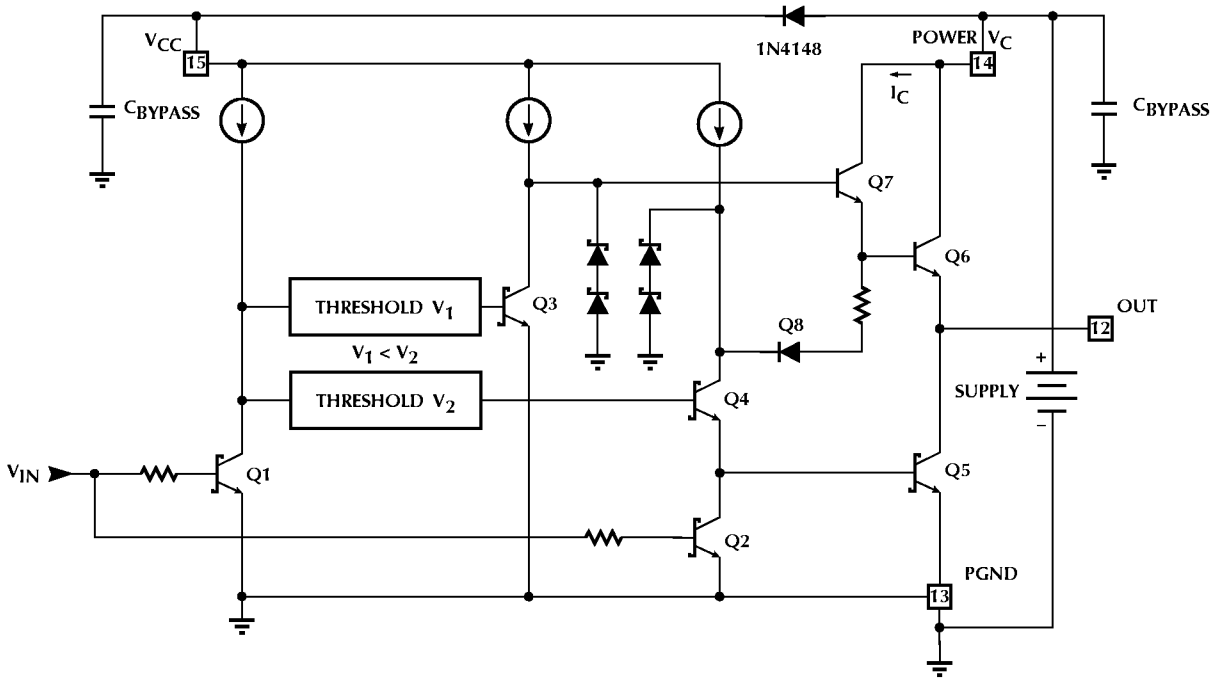


Figure 6. Totem Pole MOSFET Drive with Reduced Cross-Conduction

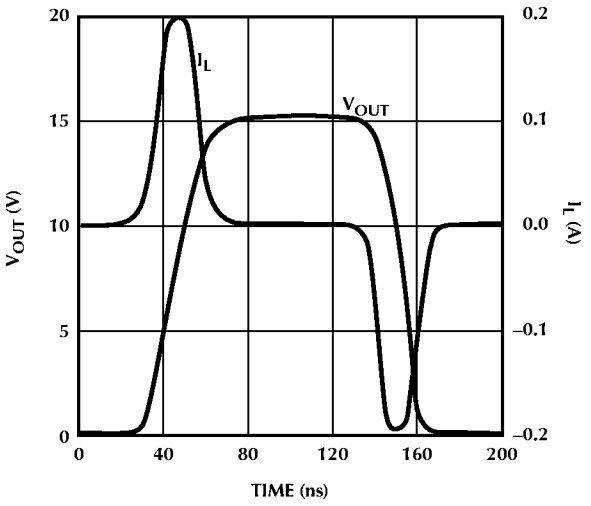


Figure 7. Rise and Fall Times when C_L = 1nF

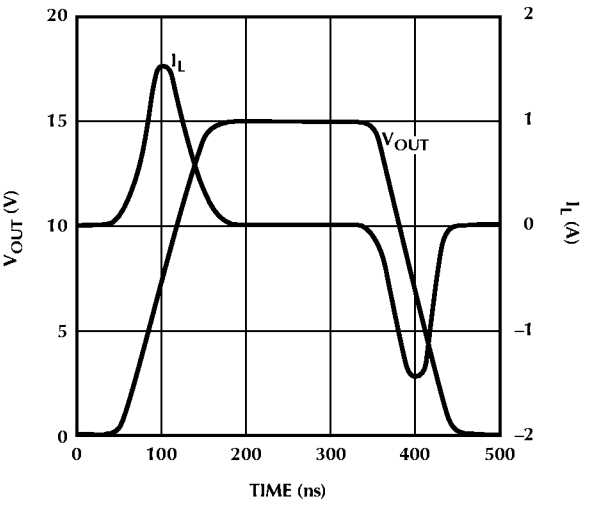


Figure 8. Rise and Fall Times when C_L = 10nF

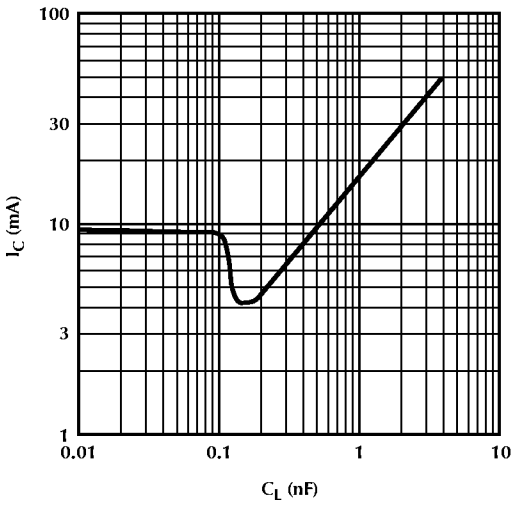


Figure 9. I_C vs C_L

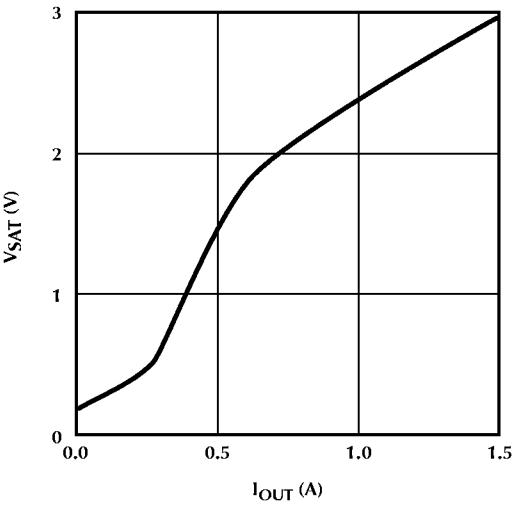


Figure 10. V_{OL} Curve

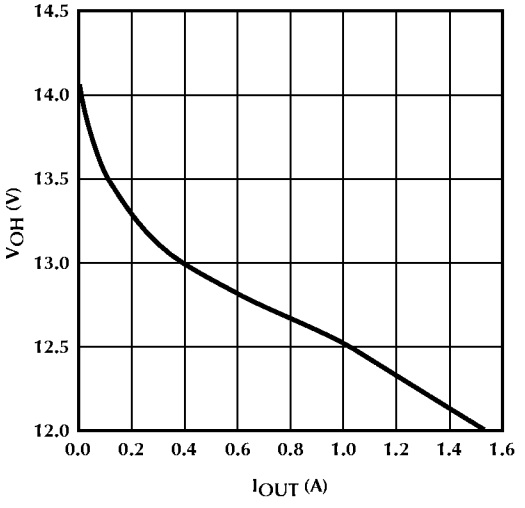


Figure 11. V_{OH} Curve

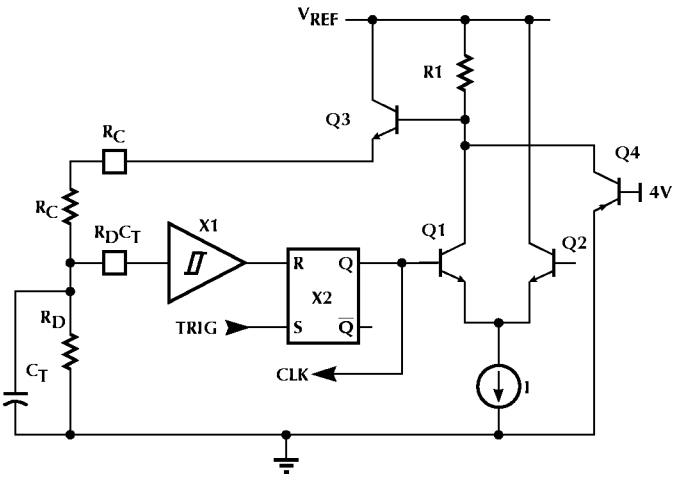


Figure 12. Block Diagram of the One-shot

FUNCTIONAL DESCRIPTION (Continued)

ONE-SHOT

Figure 12 shows the detailed block diagram of the one-shot circuitry. The one-shot is programmed with external resistors R_C & R_D and capacitor C_T. When CLK is low and Q2 conducts initially, the timing capacitor C_T is charged to 4V through R_C and Q3. This corresponds to the switch conduction cycle (on-time). When either the feedforward ramp or the sensed current signal exceeds the error amplifier output voltage a trigger pulse is sent to the one-shot which sets the R-S latch X2 and disables Q3. C_T voltage reaches the lower threshold (2V) of Schmitt-trigger X1. At this point the X1 output goes high, resetting X2, and Q1 turns off, allowing Q3 to recharge C_T to 4V. This time interval corresponds to the switch off-time. Since the off-time is simply the discharge time of C_T, one can express it this way:

$$t_{OFF} = 0.69 \times R_D C_T$$

The purpose of R_C is to slow the charging transient of C_T in order to widen the internal reset pulse. R_C is usually chosen such that the following inequality is satisfied:

$$\frac{R_C}{R_C + R_D} < 0.05$$

CONSTANT ON-TIME CLAMP (In Current-Mode Only)

In current-mode control, the maximum on-time can be clamped by using the comparator X1 (Figure 15a).

The internal transistors Q1 & Q2 and diode D2 discharge C_{FF} to approximately V_{BE}. The time taken to charge C_{FF} from V_{BE} to V_{BIAS} sets the maximum on-time, as follows:

$$t_{ON(MAX)} = \frac{V_{REF} + 0.488 \times V_{BE}}{1.488}$$

The diode D1 compensates the V_{BE} dependent C_{FF} valley voltage. It can be shown that $t_{ON(MAX)} \approx 1.115 \times R_{FF} \times C_{FF}$, and $t_{ON(MAX)}$ is relatively independent of temperature.

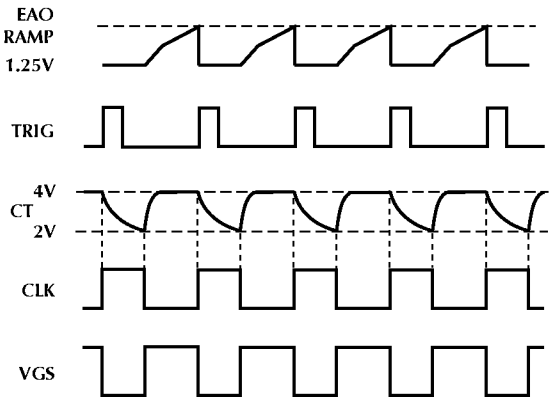


Figure 13. Timing Diagram of the One-shot

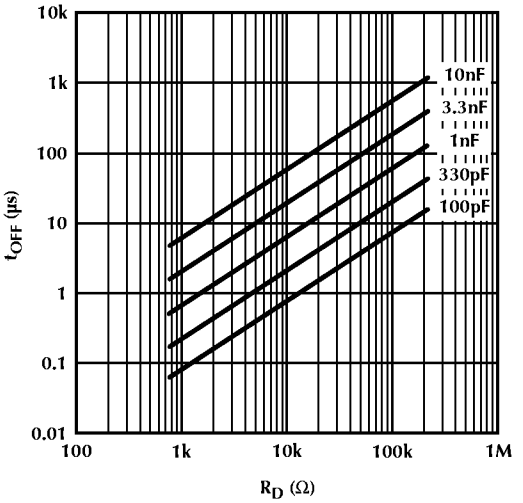


Figure 14. t_{OFF} vs R_D

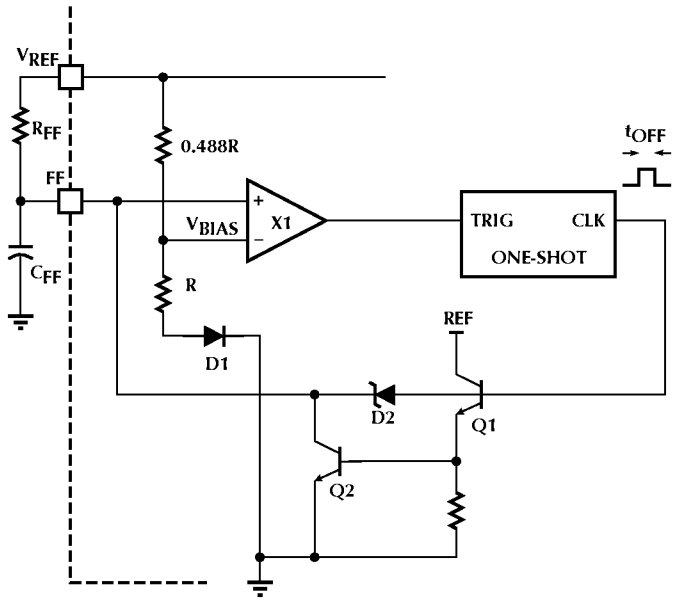


Figure 15a. Constant On-time Clamp Circuit

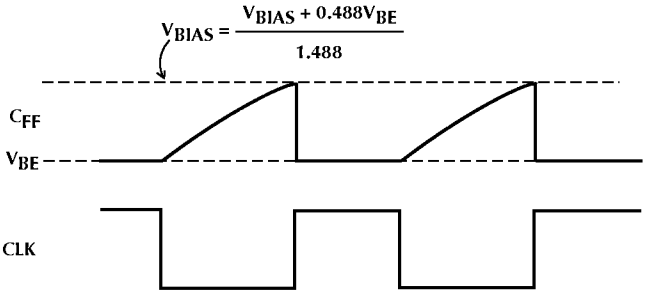


Figure 15b. Constant On-time Clamp Waveform

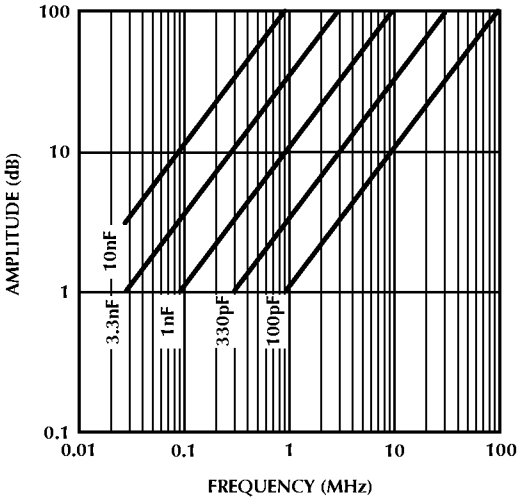


Figure 16. t_{OFF} vs R_{FF}

FUNCTIONAL DESCRIPTION (Continued)

CURRENT LIMITING, OVERLOAD SHUTDOWN AND FAULT MANAGEMENT

The ML4815 features a unique overload protection scheme. See Figure 17. The power transistor current is compared with the current-limit threshold (1.4V) of X3. When the sensed current exceeds this threshold the one-shot is triggered and the R-S latch X4 is set. The one-shot blanks the gate drive and latch X4 turns on the current source I_F. The external capacitor C_{RD}, which is normally fully discharged, is charged towards an overload threshold of 2.3V. The packet of charge delivered to C_{RD} in each overcurrent cycle is $I_F \times t_{OFF}$ (Figure 18). Latch X4 is reset after the off-time elapses. If the output short is removed before C_{RD} reaches the overload threshold, C_{RD} will be discharged through R_{RD} and normal operation will resume. However, under persistent output short circuit conditions C_{RD} is charged until it reaches 2.3V. Then the gate drive is immediately terminated, the soft-start capacitor is discharged (Figure 18), and C_{RD} discharges towards the restart threshold (1.1V) through R_{RD}. The gate drive remains off until C_{RD} is discharged below 1.1V. The time taken for C_{RD} to discharge to the restart threshold is the restart-delay time. This delay reduces the average power delivered to the load during overload conditions and protects both the load and the controller. If the overload condition persists the controller will continue to hiccup until the cause of the overload is removed. The controller undergoes soft-start at each restart. The overload shutdown and restart sequence for a converter with a non-bootstrapped power supply V_{CC} is illustrated in Figure 19.

For a bootstrapped converter (where controller V_{CC} is obtained from an auxiliary winding of the main transformer), overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage Lockout (UVLO) is activated and the onchip bandgap reference is disabled. ML4815 dissipates only 2mA of supply current during shutdown. Since I_{BLEED} is higher than the start-up current, C_S will be charged towards the UVLO start threshold. When this happens the entire controller becomes operational, except that the gate drive remains off. I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available I_{CC} will discharge C_S below the UVLO stop threshold. The onchip reference will again be disabled with the controller supply current reduced to 2mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RD} is discharged below the restart threshold. The shutdown and restart sequence is illustrated with the timing diagram in Figure 20.

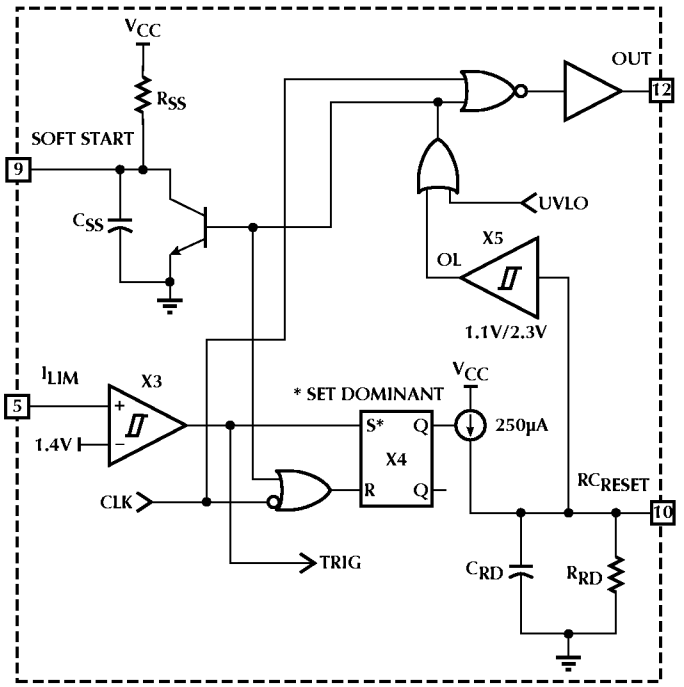


Figure 17. Overload Protection and Fault Management

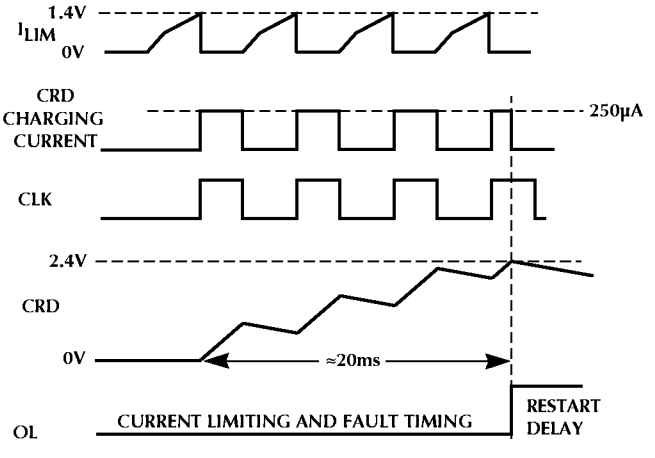


Figure 18. Current Limiting Overload Shutdown and Restart Sequence (Non-Bootstrapped Operation)

FUNCTIONAL DESCRIPTION (Continued)

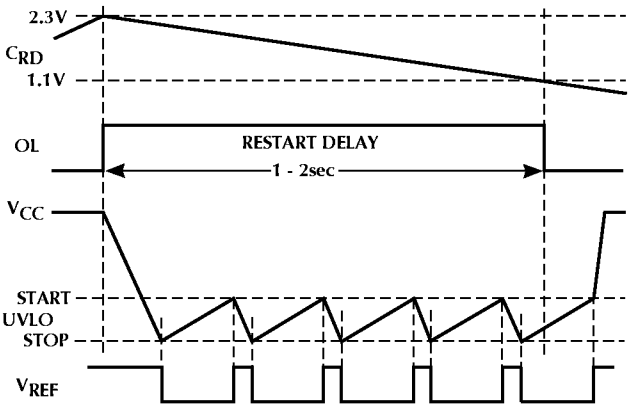


Figure 19. Overload Shutdown UVLO and Restart Sequence (Bootstrapped Operation)

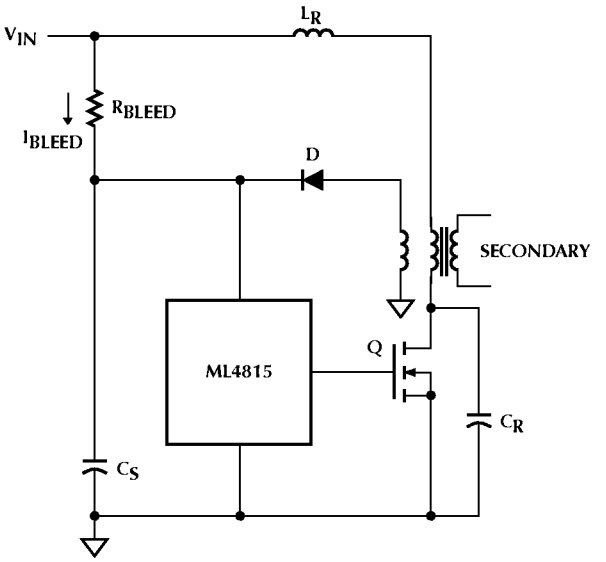


Figure 20. Simplified V_{CC} Bootstrapping Scheme

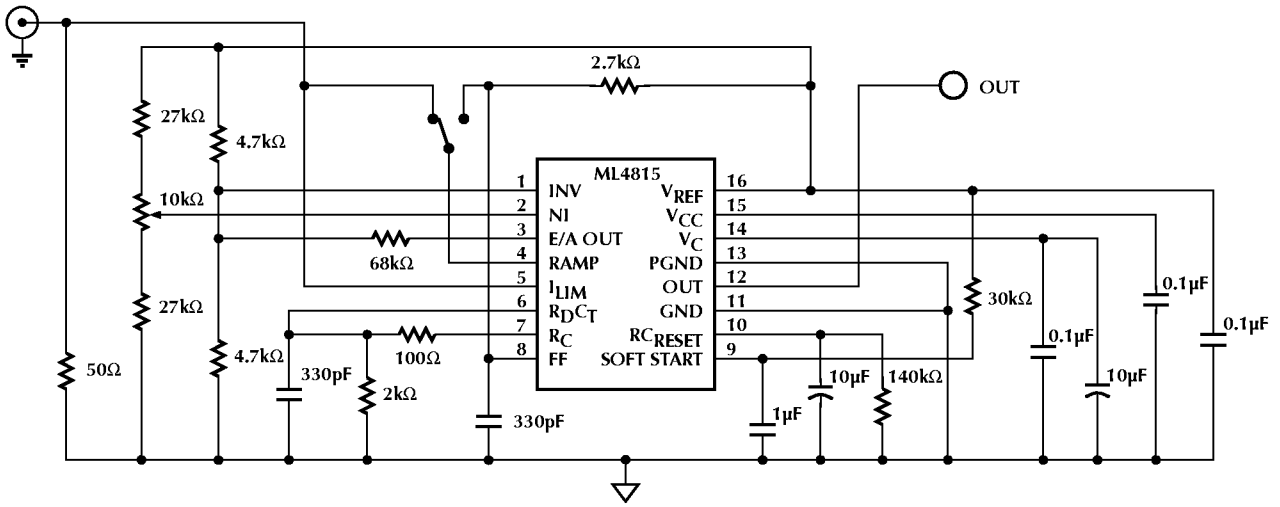


Figure 21. Open Loop Laboratory Test Fixture

FUNCTIONAL DESCRIPTION (Continued)

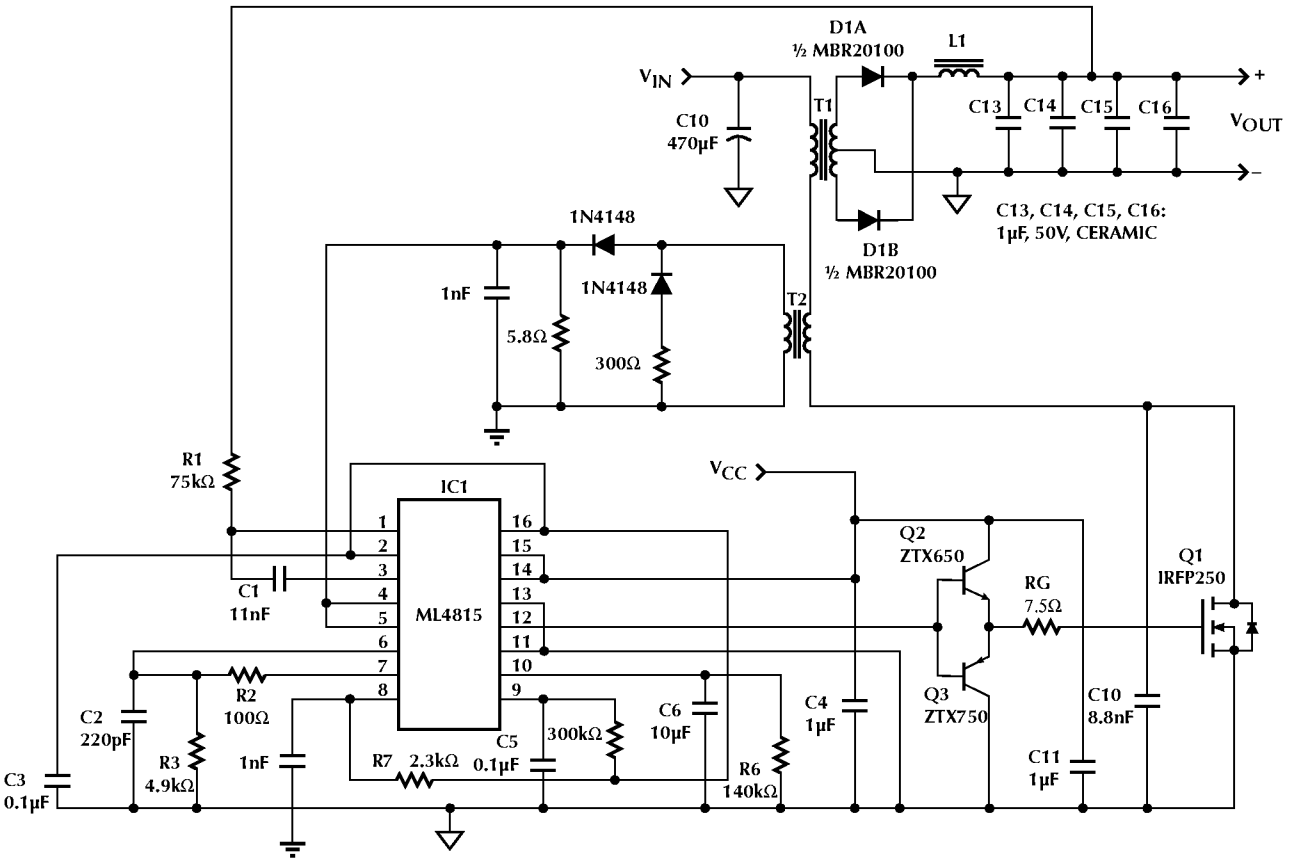
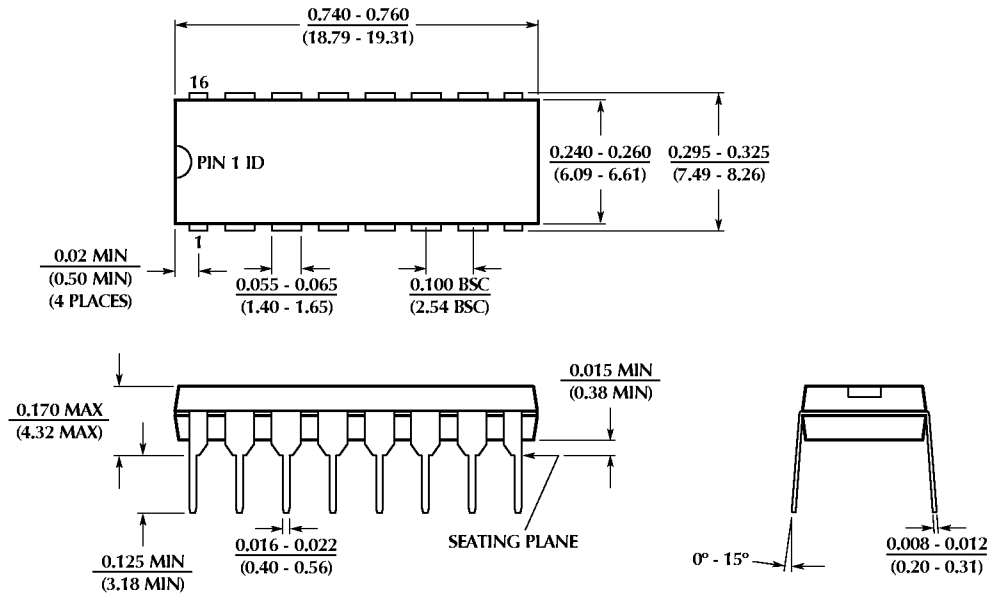


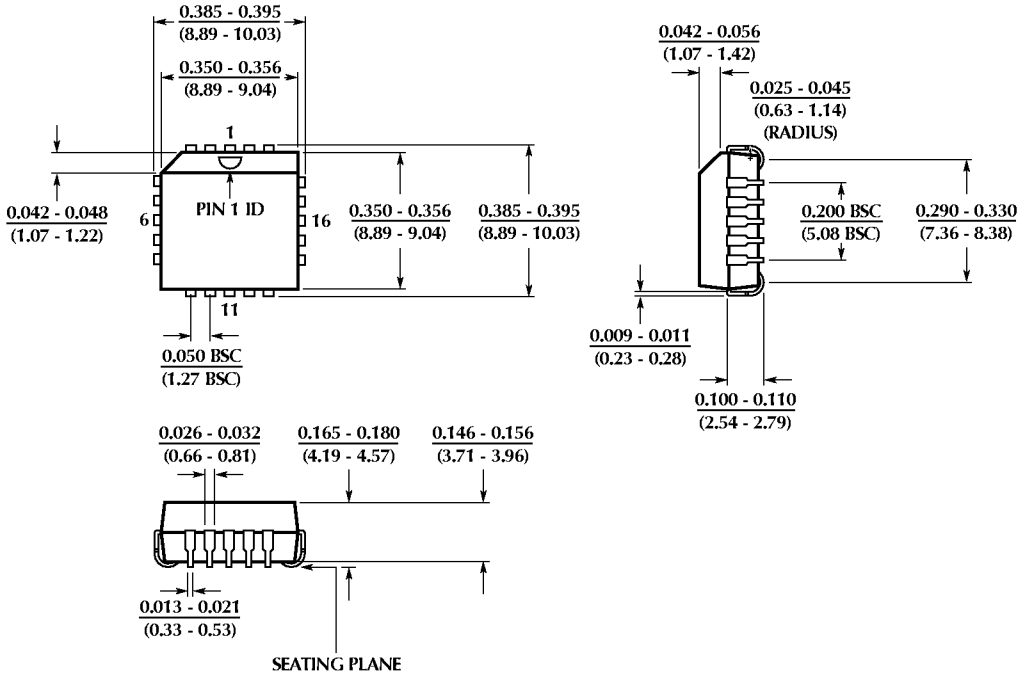
Figure 22. Schematic of a 50W ZVS DC to DC Converter

PHYSICAL DIMENSIONS inches (millimeters)

Package: P16
16-Pin PDIP



Package: Q20
20-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4815CP	0ºC to 70ºC	16-Pin PDIP (P16)
ML4815CQ	0ºC to 70ºC	20-Pin PLCC (Q20)

2092 Concourse Drive
San Jose, CA 95131
Tel: (408) 433-5200
Fax: (408) 432-0295
www.microlinear.com