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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E28RG12432LW2M450-R

Overview:

- 2.8-inch TFT: 240x320 (50.5x69.7)
- 3/4SPI+16/18- bit RGB
- 8/9/16/18-bit MCU
- 4-wire Resistive Touch Screen
- White LED back-light
- Transmissive
- Wide Temp
- 450 NITS
- Controller: ST7789V
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit and a backlight unit. The resolution of the 2.8" TFT-LCD contains 240(RGB)x320 pixels and can display up to 262k colors.

TFT Features

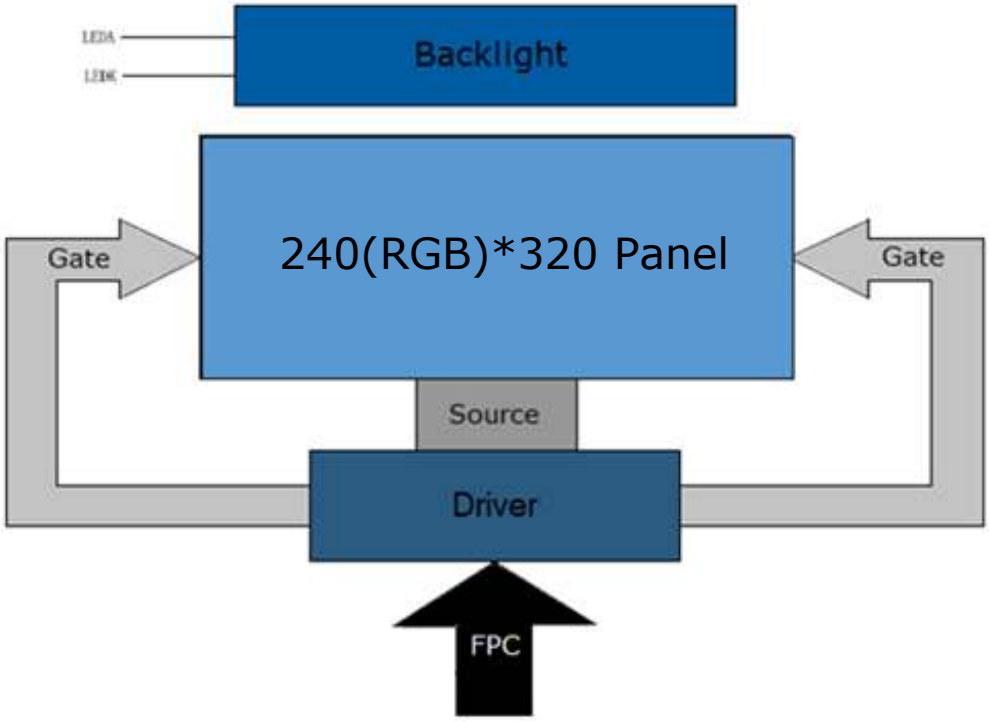
Low Input Voltage: 3.3V
Display Colors: 65k/262k colors
TFT Interfaces: 8/9/16/18-bit MCU
3/4SPI+16/18-bit RGB
3-line/4-line Serial

General Information Items	Specification Main Panel	Unit	Note
TFT Display area (AA)	43.20 (H) x 57.60 (V) (2.8 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65k/262k	colors	-
Number of pixels	240(RGB)x320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.18 (H) x 0.18 (V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ST7789V	-	-
LCM Interface	4-Lane LVDS	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

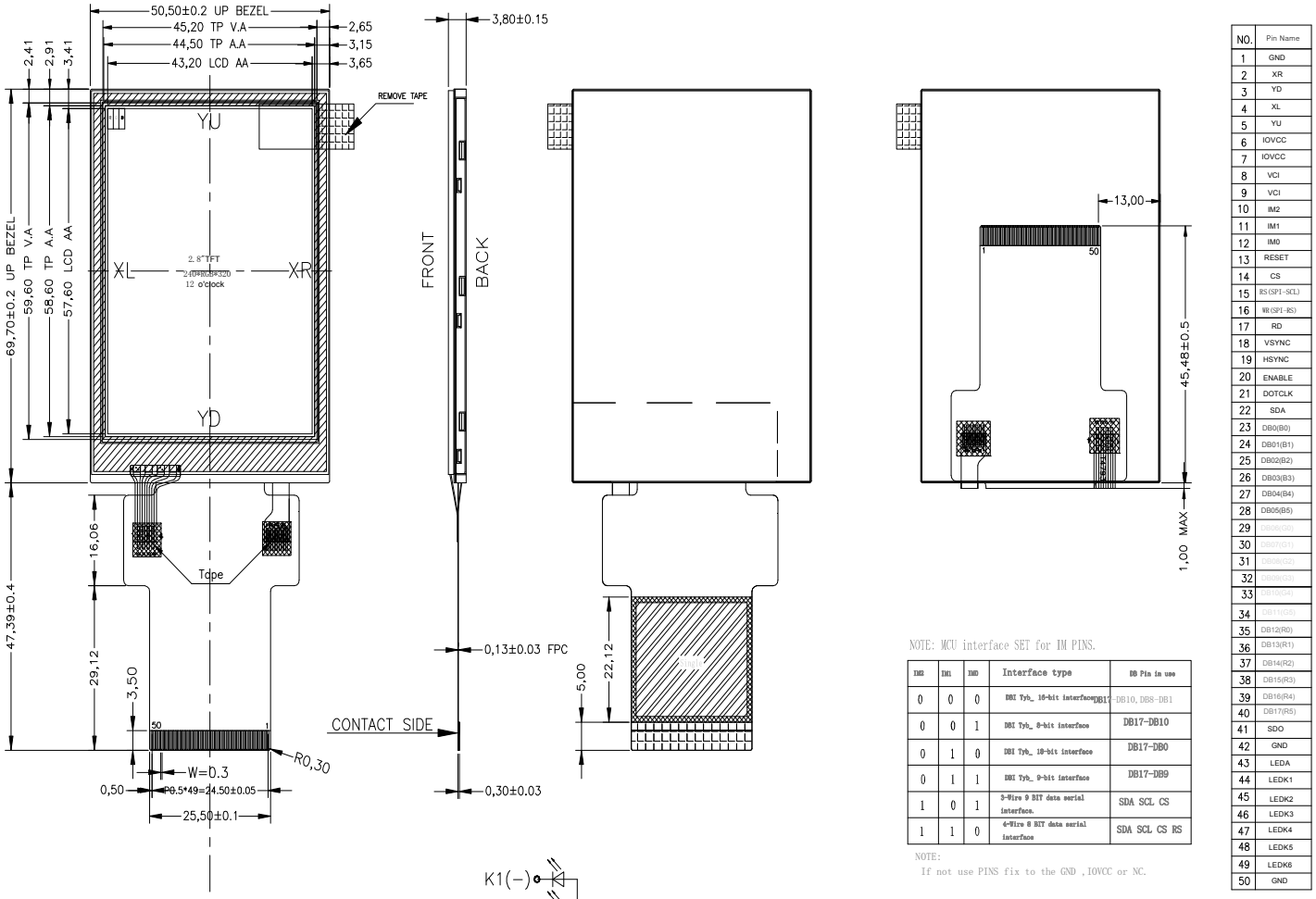
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Height (H)		50.50		mm	-
	Vertical (V)		69.70		mm	-
	Depth (D)		3.80		mm	-

1. Block Diagram



2. Outline Dimensions



NO.	Pin Name
1	GND
2	XR
3	YD
4	XL
5	YU
6	IOVCC
7	IOVCC
8	VCI
9	VCI
10	IM2
11	IM1
12	IM0
13	RESET
14	CS
15	RS (SPI-SCL)
16	WR (SPI-RS)
17	RD
18	VSYNC
19	HSYNC
20	ENABLE
21	DOTCLK
22	SDA
23	DB0(B0)
24	DB01(B1)
25	DB02(B2)
26	DB03(B3)
27	DB04(B4)
28	DB05(B5)
29	DB06(G0)
30	DB07(G1)
31	DB08(G2)
32	DB09(G3)
33	DB10(G4)
34	DB11(G5)
35	DB12(R0)
36	DB13(R1)
37	DB14(R2)
38	DB15(R3)
39	DB16(R4)
40	DB17(R5)
41	SDO
42	GND
43	LEDA
44	LEDK1
45	LEDK2
46	LEDK3
47	LEDK4
48	LEDK5
49	LEDK6
50	GND

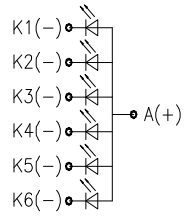
NOTE: MCU interface SET for IM PINS.

IM2	IM1	IM0	Interface type	DB Pin in use
0	0	0	DBI Typ_ 16-bit interface	DB17-DB10, DB8-DB1
0	0	1	DBI Typ_ 8-bit interface	DB17-DB10
0	1	0	DBI Typ_ 18-bit interface	DB17-DB0
0	1	1	DBI Typ_ 9-bit interface	DB17-DB9
1	0	1	3-Wire 9 BIT data serial interface.	SDA SCL CS
1	1	0	4-Wire 8 BIT data serial interface	SDA SCL CS RS

NOTE:
If not use PINS fix to the GND , IOVCC or NC.

NOTES:

1. DISPLAY TYPE: 2.8", TFT-LCD, 65K/262K COLORS
2. DISPLAY MODE: T/N NORMALLY WHITE
3. VIEWING DIRECTION: 12:00
4. DRIVER IC: ST7789V (COG)
5. VCI: 3.3V
6. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
7. BACK LIGHT: LED WHITE, 6 LED, 120mA, 3.2±0.3V
8. RoHS COMPLIANT.



BL CIRCUIT DIAGRAM

NOTE: RGB interface

RGB Interface	DB Pin in use
16(565) Bit RGB interface	DB17-DB13, DB11-DB8, DB5-DB1
18(666) Bit RGB interface	DB17-DB0

NOTE: If used RGB mode must select serial interface!

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3. Input Terminal Pin Assignment

Recommended TFT Connector: FH12S-50S-0.5SH(55) | Recommended RTP Connector: FH33-4S-1SH(10)

NO.	Symbol	Description	I/O
1	GND	Ground	
2	XR	Touch panel right glass terminal	
3	YD	Touch panel bottom film terminal	
4	XL	Touch panel left glass terminal	
5	YU	Touch panel top film terminal	
6	IOVCC	Supply voltage for IO (1.8-3.3V)	
7	IOVCC	Supply voltage for IO (1.8-3.3V)	
8	VCI	Supply voltage (3.3V)	
9	VCI	Supply voltage (3.3V)	
10	IM2	MPU parallel interface bus and serial interface select. If using RGB interface, you must select which serial interface. Fix to IOVCC and GND.	
11	IM1		
12	IM0		
13	RESET	Reset signal of the device. Must be applied to initialize chip.	
14	CS	Chip select input pin. Low enabled. Fix to IOVCC and GND when not in use.	
15	RS(SPI_SCL)	Data or command pin in parallel interface. D/CX=1, data is selected. When D/CX=0, command is selected. In the serial interface this pin is used as the data clock.	
16	WR(SPI_RS)	Write signal in parallel interface. In serial interface it is a data pin. Data is applied at the rising edge of the SCL signal. Fix to IOVCC or GND when not used.	
17	RD	Read signal for parallel interface and MCU read data at the rising edge. Fix to IOVCC or GND when not in use.	
18	VSYNC	Frame synchronizing signal for RGB interface. Fix to IOVCC or GND when not used.	
19	HSYNC	Line synchronizing signal for RGB interface. Fix to IOVCC or GND when not used.	
20	ENABLE	Data enable signal for RGB interface. Fix to IOVCC or GND when not used.	
21	DOTCLK	Dot clock signal for RGB interface. Fix to IOVCC or GND when not used.	
22	SDA	Serial input signal. The data is applied at the rising edge of the SCL signal. Fix to IOVCC or GND when not used.	
23-40	DB0-DB17	18-bit data bus. If not used please fix these pins to GND.	
41	SDO	SPI interface output pin. The data is output on the falling edge of the SCL signal. Leave this pin open if not used.	
42	GND	Ground	
43	LEDA	Anode pin of the backlight	
44	LEDK1	Cathode pin of the backlight	
45	LEDK2	Cathode pin of the backlight	
46	LEDK3	Cathode pin of the backlight	
47	LEDK4	Cathode pin of the backlight	
48	LEDK5	Cathode pin of the backlight	
49	LEDK6	Cathode pin of the backlight	
50	GND	Ground	

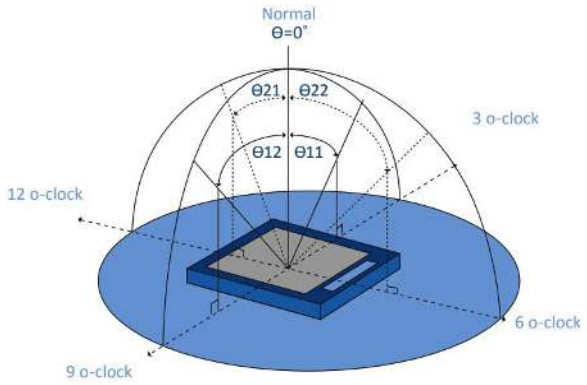
4. LCD Optical Characteristics

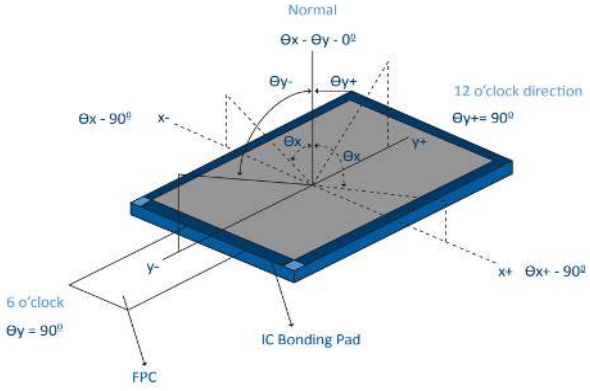
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Transmittance		T%		--	17.3	--	%	
Contrast Ratio		CR	θ=0 Normal viewing angle	400	500	--	%	(2)
Response Time	Rising	TR		--	4	8	ms	
	Falling	TF		--	12	24	ms	
Color Filter Chromaticity	White	W_X		0.283	0.303	0.323		(5)(6)
		W_Y		0.305	0.325	0.345		
	Red	R_X		0.606	0.626	0.646		
		R_Y		0.314	0.334	0.354		
	Green	G_X		0.257	0.277	0.297		
		G_Y		0.529	0.549	0.569		
	Blue	B_X		0.122	0.142	0.162		
		B_Y		0.102	0.122	0.142		
Viewing Angle	Hor.	ΘL	CR≥10	35	45	--	degree	(1)(6)
		ΘR		35	45	--		
	Ver.	ΘT		40	50	--		
		ΘB		10	20	--		
Option View Direction		12:00						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



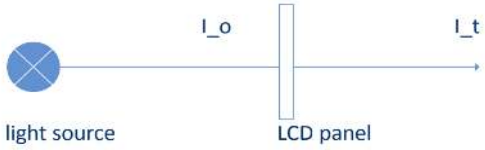


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$\mathrm{Cr} = \frac{\mathrm{Lw}}{\mathrm{Ld}}$$

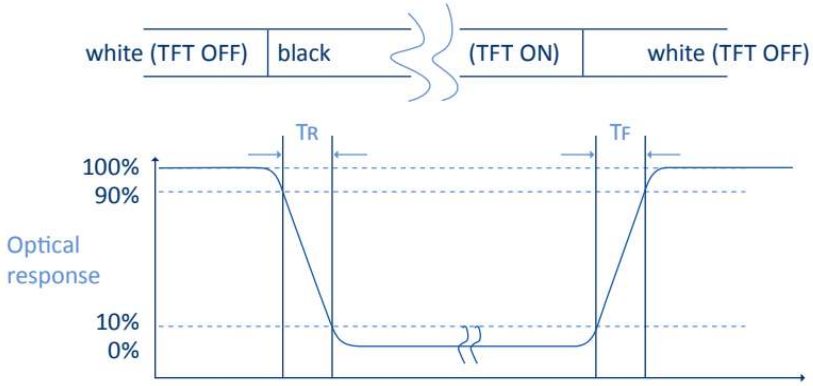
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$\mathrm{Tr} = \frac{\mathrm{It}}{\mathrm{Io}}\ x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

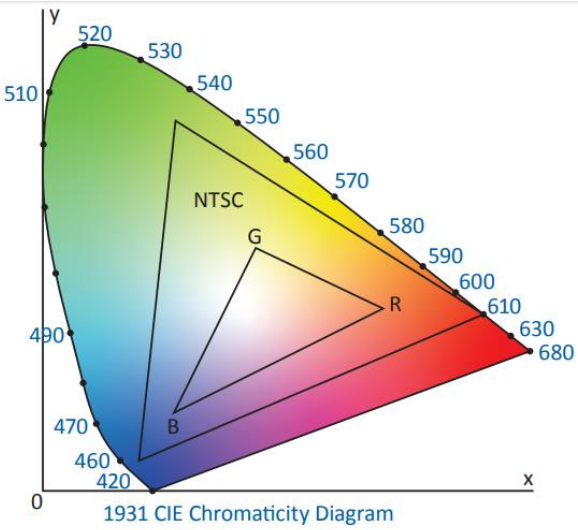
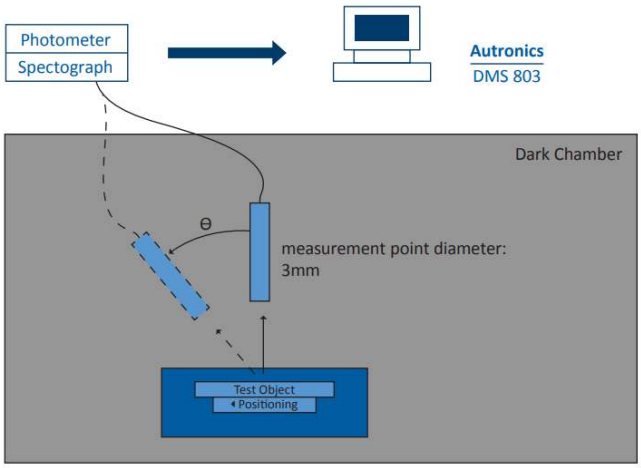


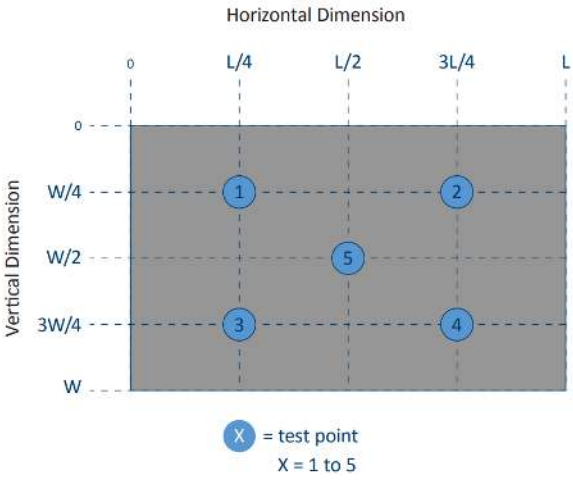
Fig. 1931 CIE chromacity diagram

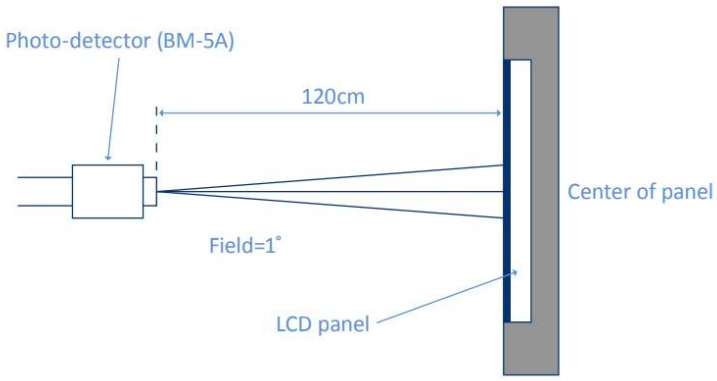
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	3.0	4.6	V
Digital Interface Supply Voltage	VDDIO	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	2.4	3.3	4.2	V	
Digital Interface Supply Voltage	VDDIO	1.65	3.3	4.2	V	
Normal Mode Current Consumption	IDD	--	8	--	mA	
Level Input Voltage	VIH	0.7VDDIO	--	VDDIO	V	
	VIL	GND	--	0.3VDDIO	V	
Level Output Voltage	VOH	0.8VDDIO	--	VDDIO	V	
	VOL	GND	--	0.2VDDIO	V	

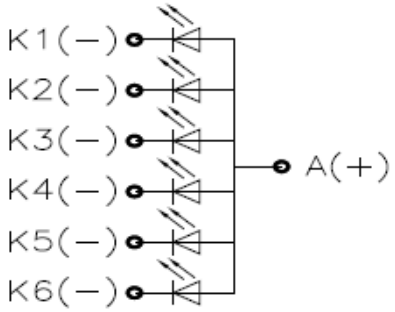
5.3 LED Backlight Characteristics

The backlight system is edge lighting type with 6 chips LED.

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	90	120	--	mA	
Forward Voltage	V_F	--	3.2	--	V	
LCM Luminance	LV	--	450	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

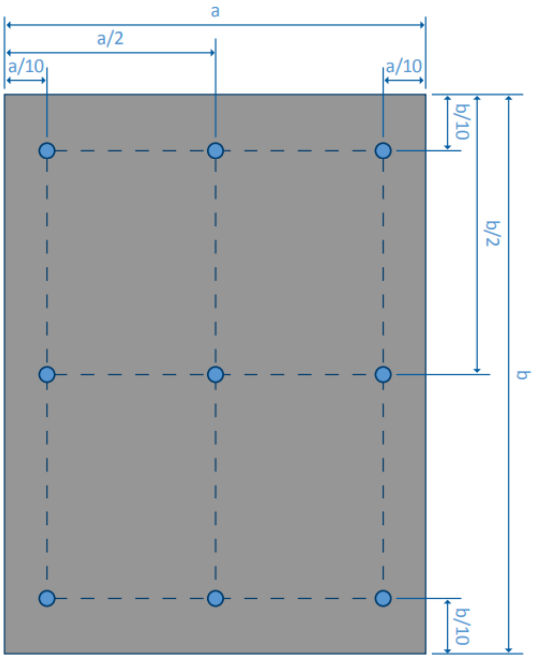
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 160mA



Backlight Circuit LED

Note 3: Luminance Uniformity of these 9 points is defined as below:

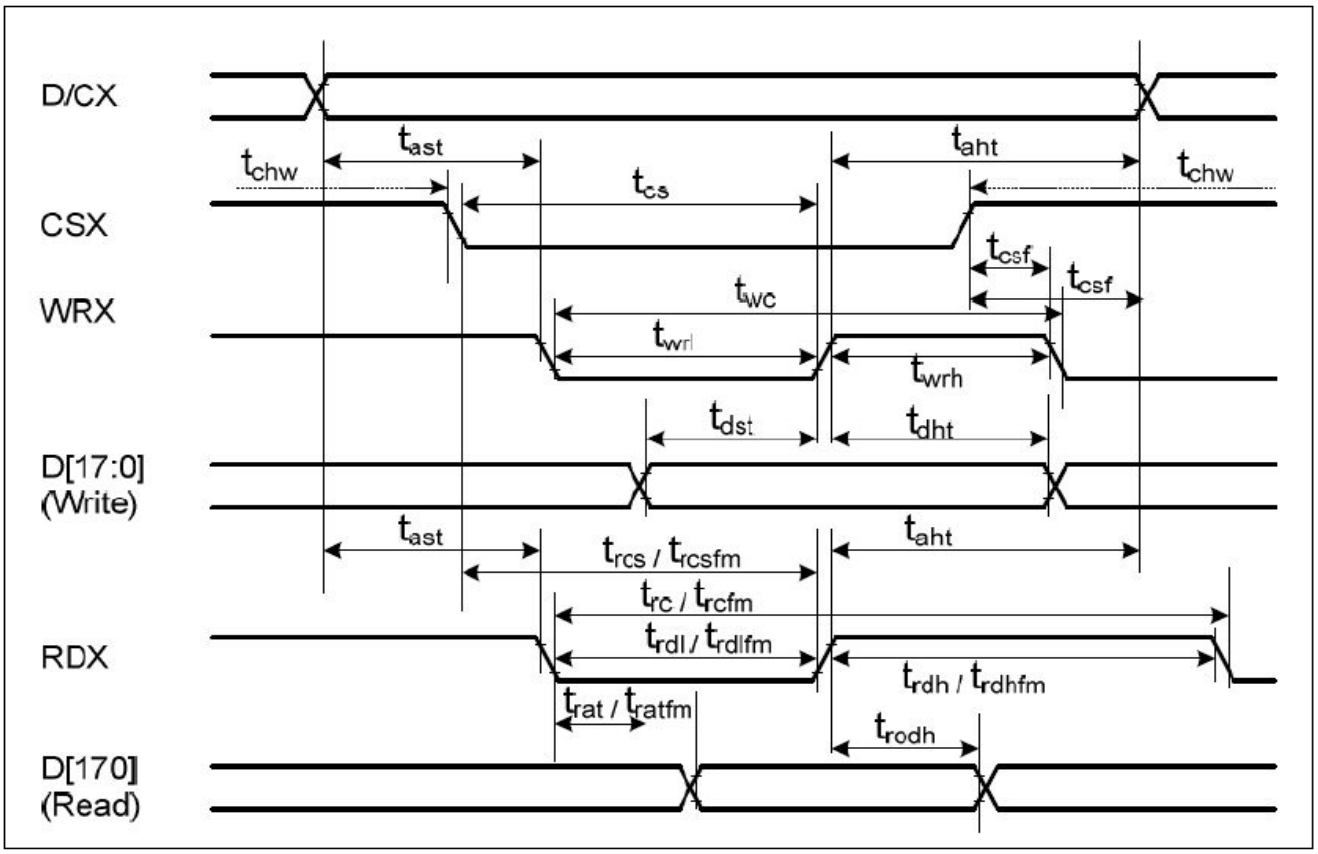


$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

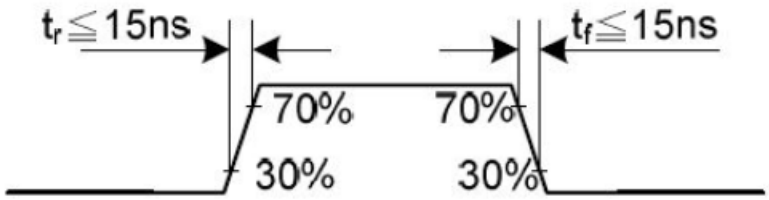
6. TFT AC Characteristics

6.1 DBI Type B (18/16/9/8 bit) Interface Timing Characteristics (8080-series)

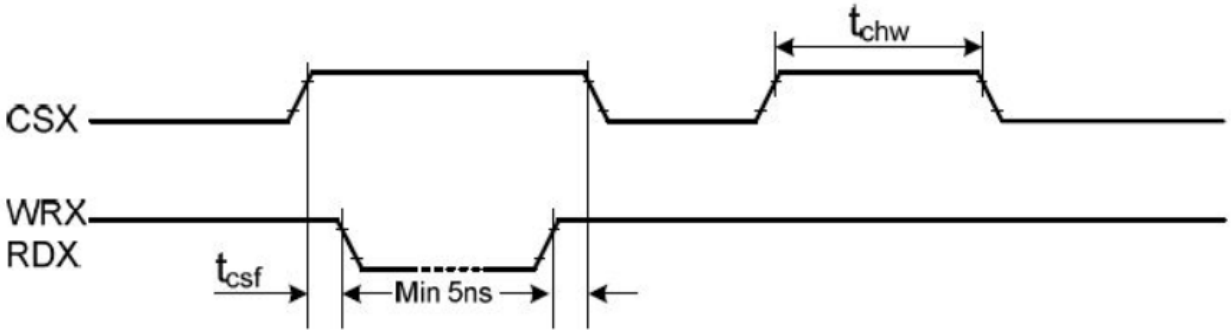


Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	that	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX “H’ pulse width	0	-	ns	
	tcs	Chip select setup time (Write)	15	-	ns	
	trcs	Chip select setup time (Read ID)	45	-	ns	
	trcsfm	Chip select setup time (Read FM)	355	-	ns	
	tcsf	Chip select wait time (Write/Read)	0	-	ns	
WRX	twc	Write cycle	50	-	ns	
	twrh	Write control pulse H duration	15	-	ns	
	twrl	Write control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read cycle (FM)	450	-	ns	When read from frame memory
	trdhfm	Read control H duration (FM)	90	-	ns	
	trdlfm	Read control L duration (FM)	355	-	ns	
RDX(ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read control pulse H duration	90	-	ns	
	trdl	Read control pulse L duration	45	-	ns	
DB[17:0] DB[15:0] DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum, CL=30pF For minimum, CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

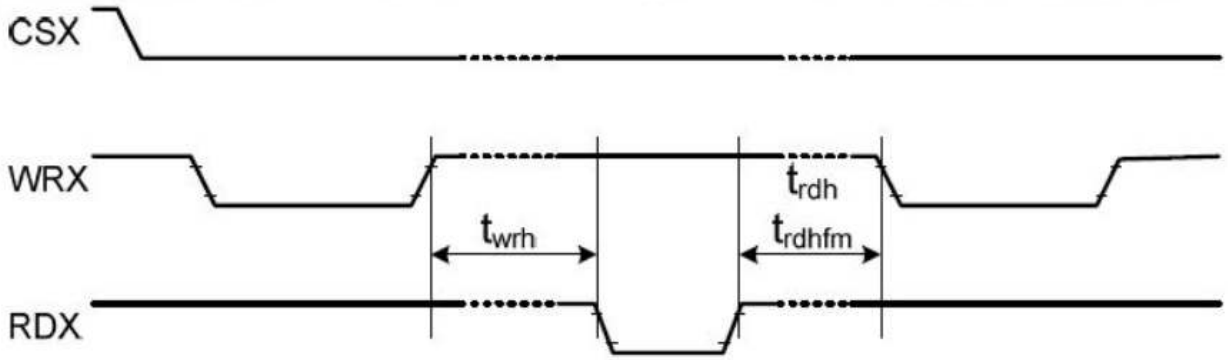
Note: (1) Ta = -30 to 70˚, IOVCC = 1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=DGND=0V



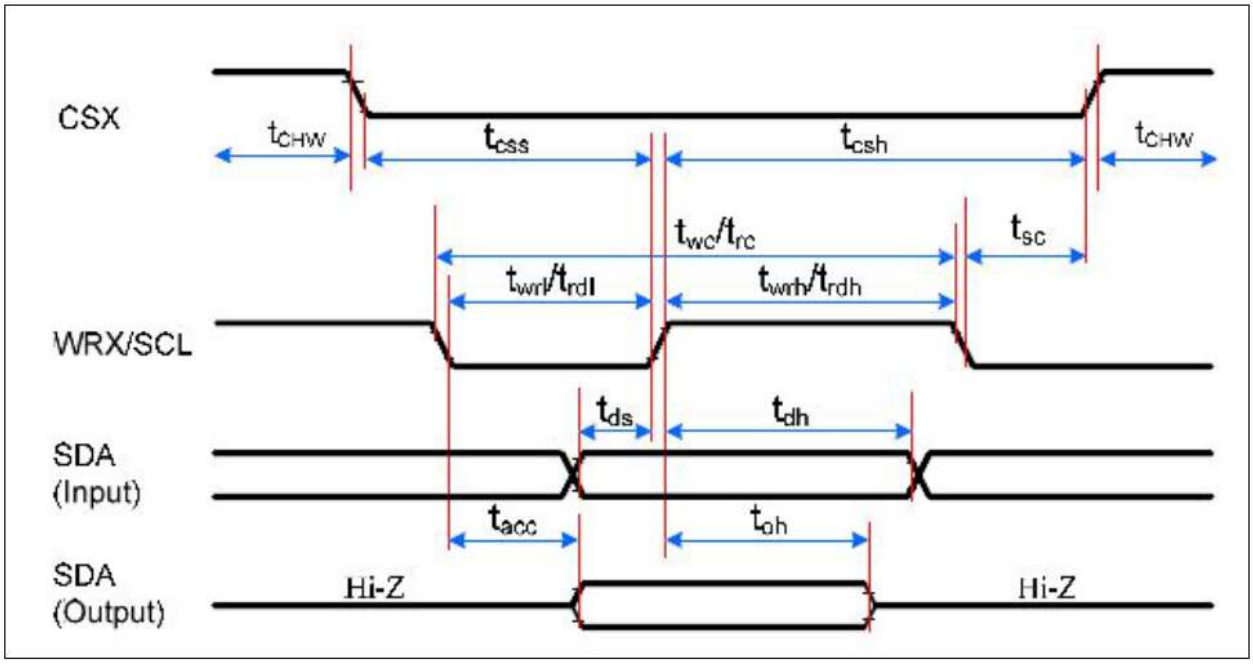
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



(3) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

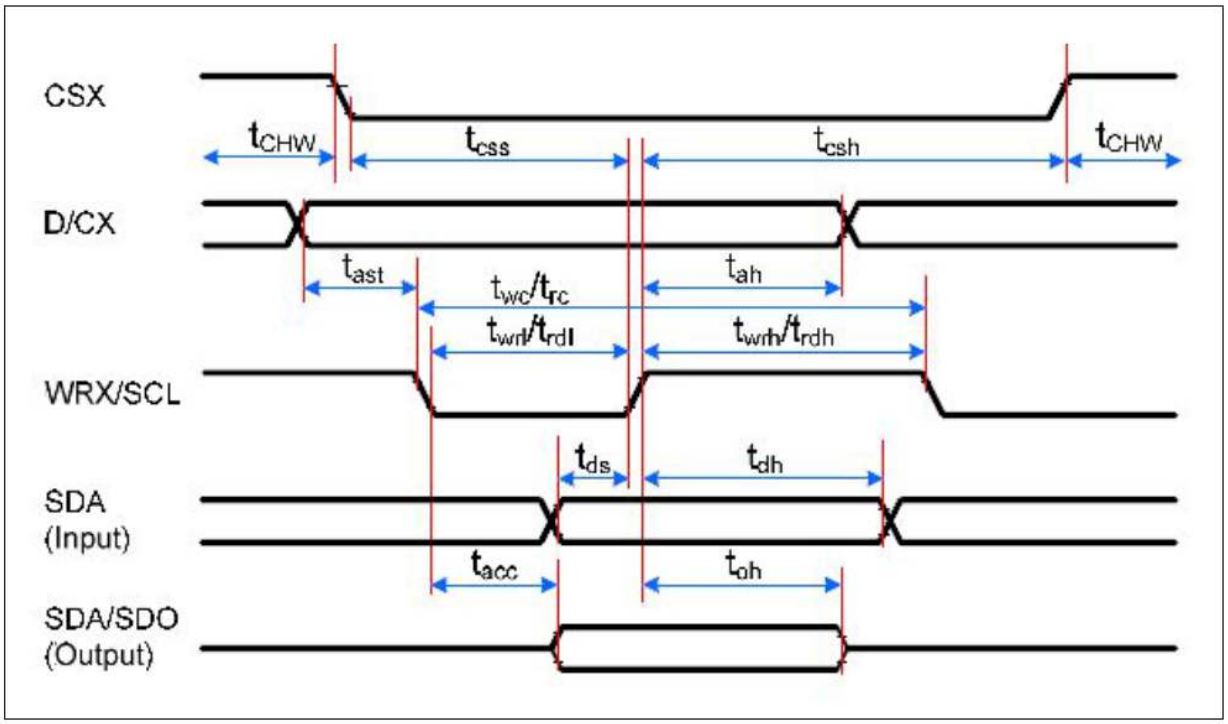


6.2 Display Serial Interface Timing Characteristics (3-line SPI system)



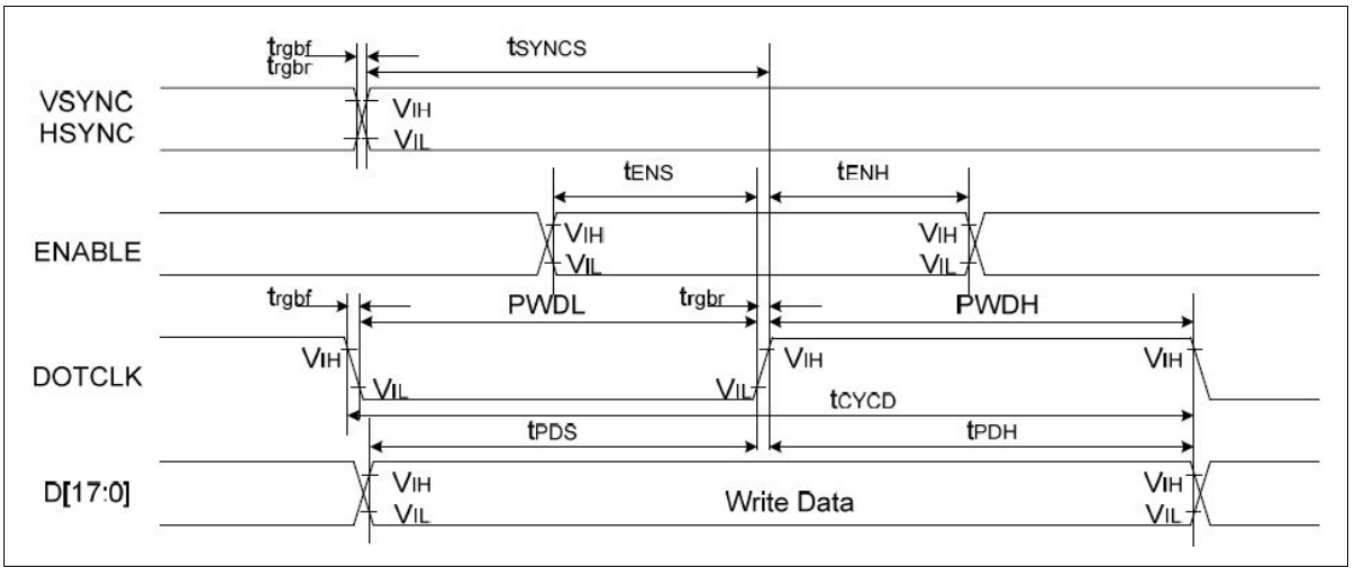
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H pulse width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL H pulse width (Write)	15	-	ns	
	twrl	SCL L pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	When read ID data
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For max, CL=30pF For mini, CL=8pF
	toh	Output disale time (Read)	15	50	ns	

6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

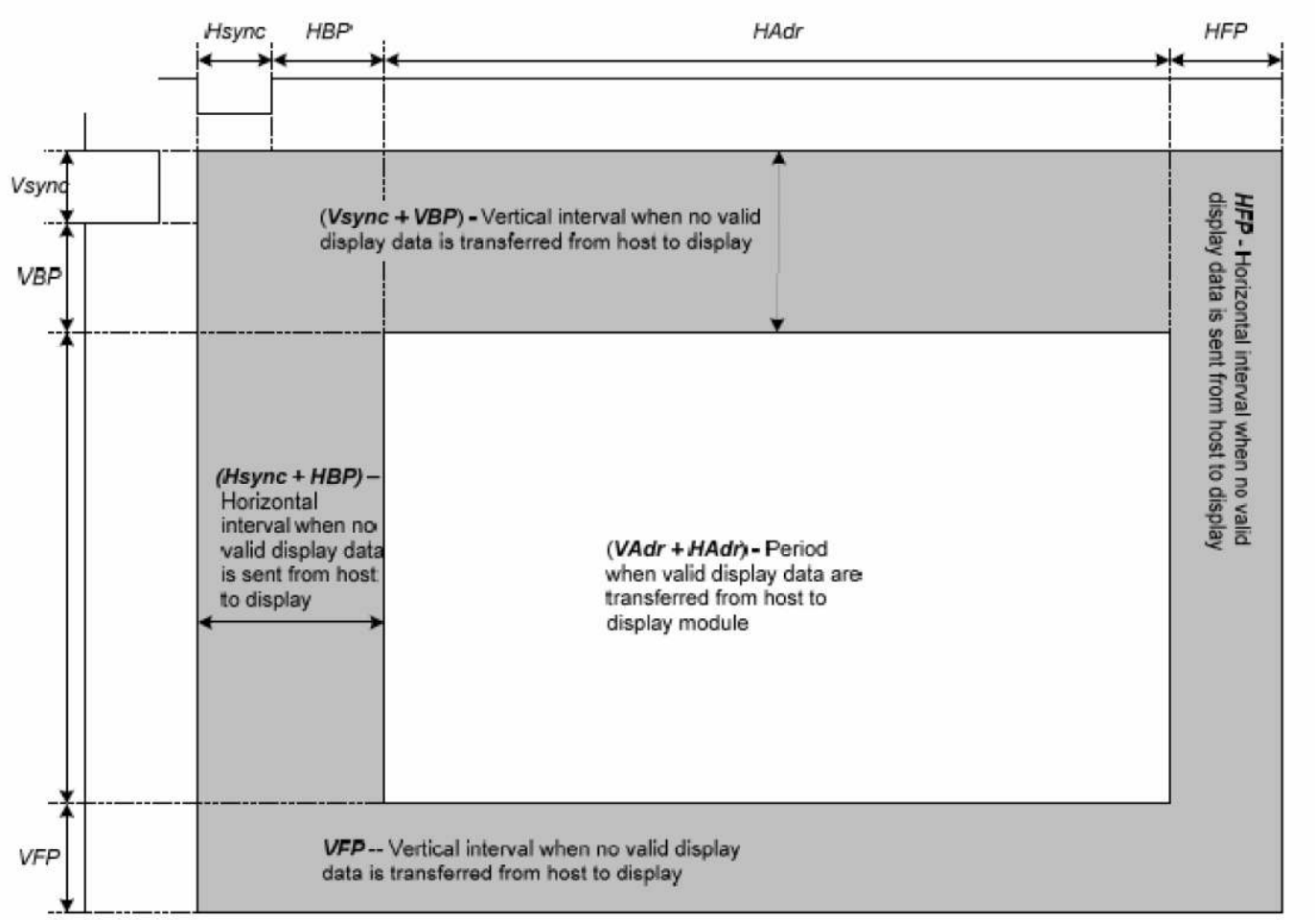


Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	tsc	SCL-CSX	15	-	ns	
	tchw	CSX H pulse width	40	-	ns	
	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	65	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL H pulse width (Write)	15	-	ns	
	twrl	SCL L pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL H pulse width (Read)	60	-	ns	
	trdl	SCL L pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	50	ns	For max, CL=30pF
	toh	Output disale time (Read)	15	50	ns	For mini, CL=8pF

6.4 Parallel 18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC/ HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	tENS	ENABLE setup time	15	-	ns	
	tENH	ENABLE hold time	15	-	ns	
DB[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	66	-	ns	
	trgbr,trgbf	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	



Parameters	Symbols	Min	Typ.	Max	Units
PCLK cycle	PCLKcyc	100	80	66.6	Ns
Horiontal synchronization	Hsync	3	3	-	PCLK
Horizontal back porch	HBP	3	3	-	PCLK
Horizontal address	HAdr	-	320	-	PCLK
Horizontal front porch	HFP	3	3	-	PCLK
Vertical synchronization	Vsync	2	2	-	Line
Vertical back porch	VBP	2	2	-	Line
Vertical address	Vadr	-	480	-	Line
Vertical front porch	VFP	2	2	-	Line
Vertical frequency(*)		50	60	80	Hz
Horizontal frequency(*)		-	33	-	kHz
PCLK frequency(*)		10	12.5	15	MHz

Notes:

(1) Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr +VFP.

(2) Horizontal period (one line) shall be equal to the sum Hsync + HBP +HAdr + HFP.

(3) Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pizels are transferred between the host processor and the display module.

6.5 Reset Timing

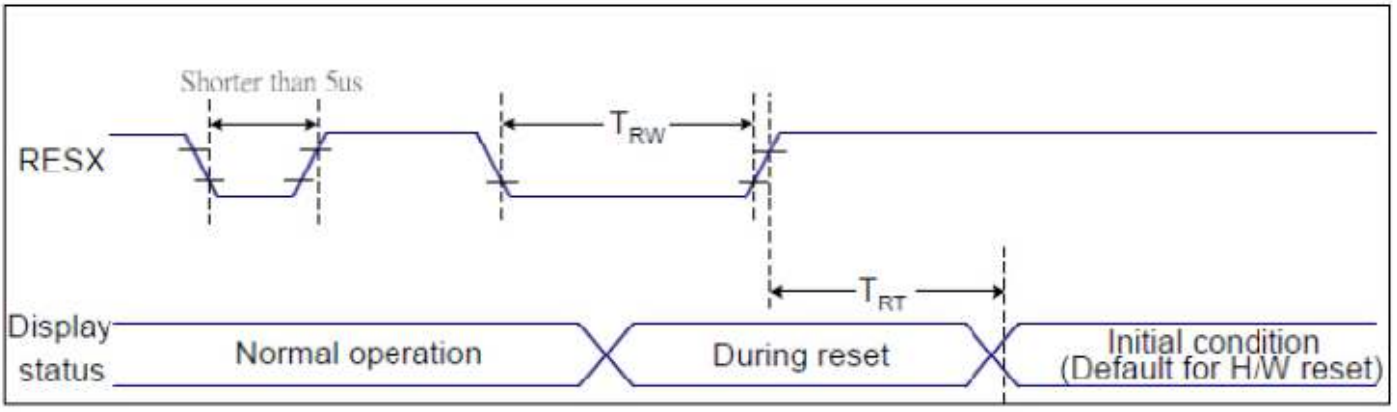


Figure 6.5: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

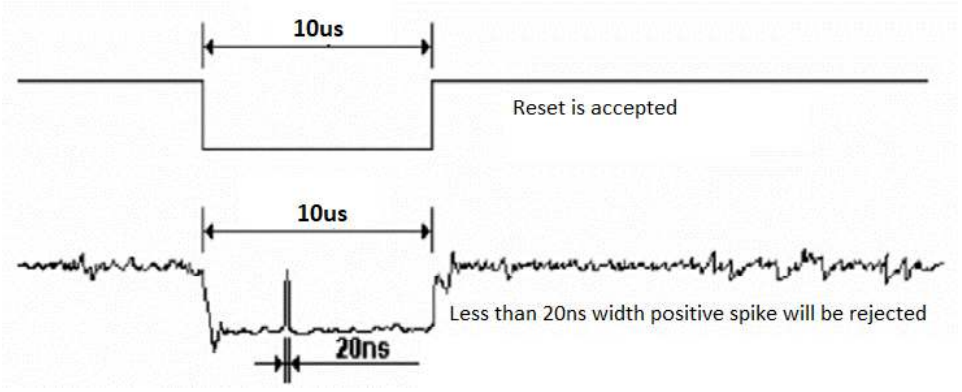
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

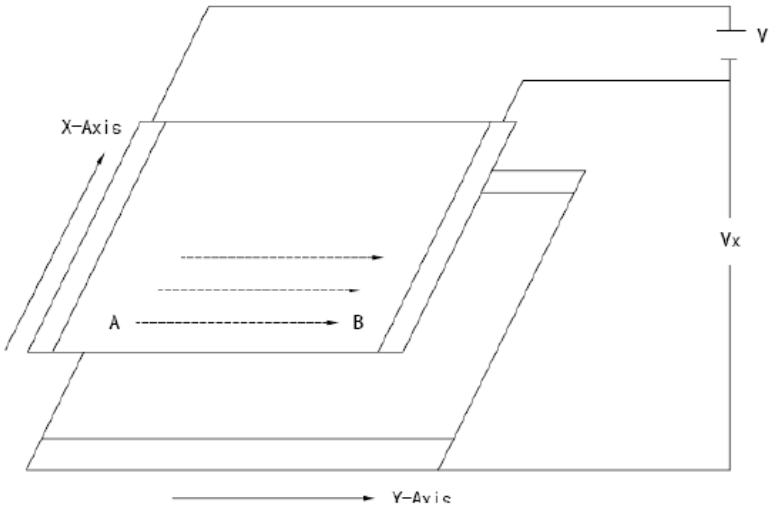
7. TP Feature

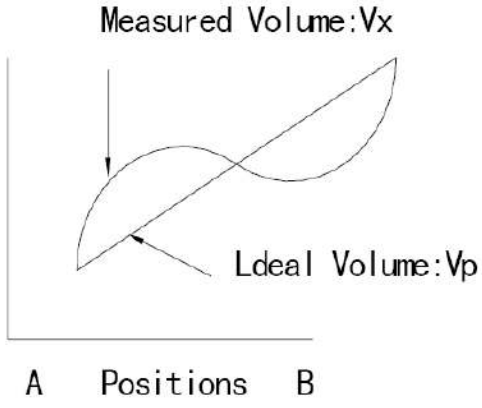
7.1 Conditions of Use and Storage

Item	Condition	Note
Temperature range upon operation	Humidity: 20%-90% non-dew, condensation -20℃~70℃	In a simple substance
Temperature range upon storage	Humidity: 20%-90% non-dew, condensation -30℃~80℃	In a simple substance

7.2 Electrical Property

Item	Value	Note
Maximum voltage	DC5V	
Resistance between terminal	X direction (film side): 200-600 Ω	
	Y direction (glass side): 300-900 Ω	
Insulation resistance	DC 25V, 20MΩ or above	Connect X + ~X and Y+ ~Y, apply 25VDC Between X and Y for perform measurements
Chattering	10ms or below	
Rating	Voltage is 5V DC	





7.3 Mechanical Property

Item	Value		Note
Input method	Used of an exclusive pen or finger		
Load upon operation	Exclusive pen	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: Stylus pen material: POM (ployacetal) Tip: Diameter 3.0mm, SR 0.8 mm
	Finger	60-100g or below	Operation and measurement with a pen must be carried out under the following tip conditions: Stylus pen material: Silicon rubber (Hardness: 30°Hs) Tip: Diameter 12.0mm, SR 12.5 mm
Surface hardness	Pencil Hardness: 3H or above		It complies with the way of test method JIS K5400

7.4 Optical Property

Item	Performance	Note
Total light transmittance	80% or above	JIS K7105
Haze	5% or below	JIS K7136
Film specification	Polished type with hard coated surface	

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.