## SQJ184EP

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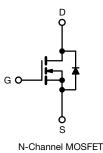
# Automotive N-Channel 80 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	80
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0075
I <sub>D</sub> (A)	118
Configuration	Single
Package	PowerPAK SO-8L

#### **FEATURES**

- TrenchFET<sup>®</sup> Gen IV power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	80	V	
Gate-source voltage		V <sub>GS</sub>	± 20		
Continuous drain current	T <sub>C</sub> = 25 °C	1	118		
Continuous drain current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	68		
Continuous source current (diode conduction)		IS	210	А	
Pulsed drain current		I <sub>DM</sub>	240		
Single pulse avalanche current		I <sub>AS</sub>	32		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	51	mJ	
Maximum neuror dissinction	T <sub>C</sub> = 25 °C	D	234	W	
Maximum power dissipation	T <sub>C</sub> = 125 °C	P <sub>D</sub>	78	vv	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) b			260	-0	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>a</sup>	R <sub>thJA</sub>	42	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	0.64	0/10

Notes

a. When mounted on 1" square PCB (FR4 material)

b. See solder profile (<u>www.vishay.com/doc?73257</u>). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

1

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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static	•						
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = 250 \ \mu A$		80	-	-	v
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μΑ	2.2	2.7	3.5	v
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 20 V$	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 80 V	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 80 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50	μA
		$V_{GS} = 0 V$	$V_{DS} = 80 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \geq 5 \ V$	30	-	-	А
Drain-source on-state resistance <sup>a</sup>		$V_{GS} = 10 V$	I <sub>D</sub> = 15 A	-	0.0060	0.0075	
	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C	-	-	0.0124	Ω
		$V_{GS} = 10 V$	I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C	-	-	0.0156	
Forward transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub>	-	67	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	2484	3478	pF
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	1029	1441	
Reverse transfer capacitance	C <sub>rss</sub>			-	76	107	
Total gate charge <sup>c</sup>	Qg			-	46	69	
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 40$ V, $I_D = 30$ A	-	12	-	nC
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	13	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.6	1.2	1.8	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>				12	18	- ns
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 40 V, R <sub>L</sub> = 1.33 Ω, I <sub>D</sub> ≅ 30 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	4	6	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	23	35	
Fall time <sup>c</sup>	t <sub>f</sub>			-	5	8	
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>				-	240	Α
Forward voltage	V <sub>SD</sub>	$I_F = 15 \text{ A}, V_{GS} = 0 \text{ V}$		-	-	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs		-	37	74	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	38	76	nC
Reverse recovery fall time	t <sub>a</sub>			-	21	-	ne
Reverse recovery rise time	t <sub>b</sub>			-	15	-	ns
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-2.0	-	А

#### Notes

a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing

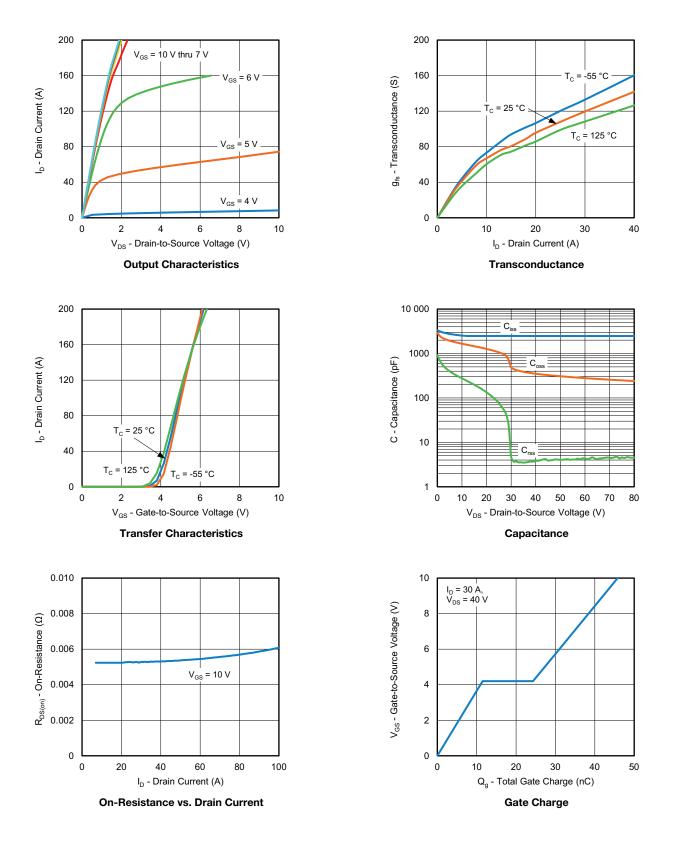
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



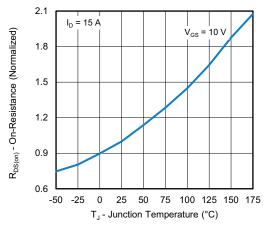
S22-0857-Rev. A, 17-Oct-2022

3

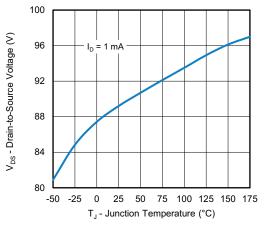
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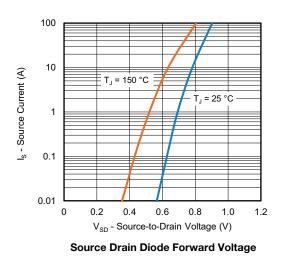
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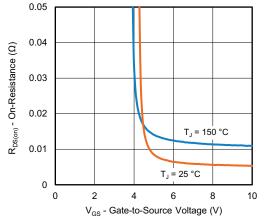


On-Resistance vs. Junction Temperature

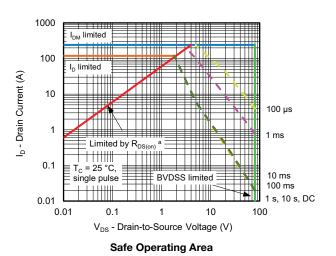


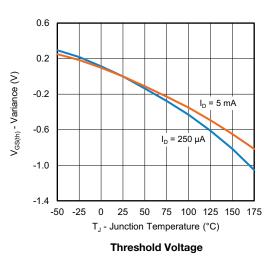
Drain Source Breakdown vs. Junction Temperature





**On-Resistance vs. Gate-to Source Voltage** 





Note

a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

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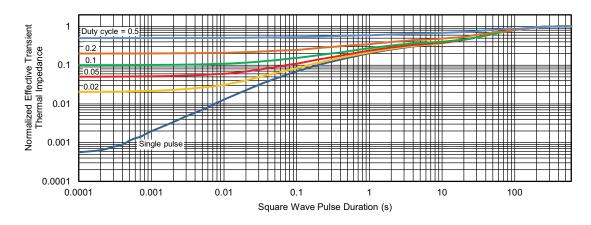
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Document Number: 62032

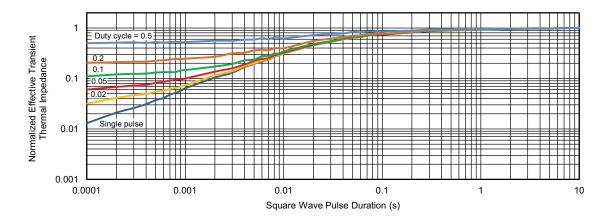
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#### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

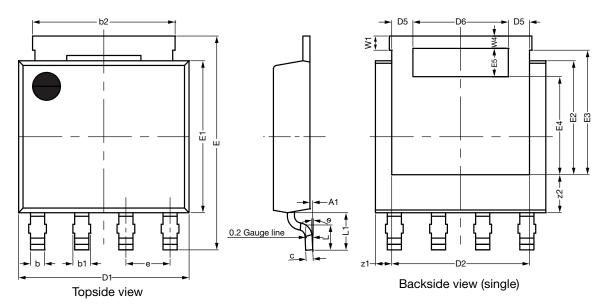
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

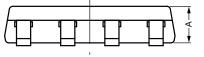
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# PowerPAK<sup>®</sup> SO-8L (PPKSO8LWLA) Case Outline 3





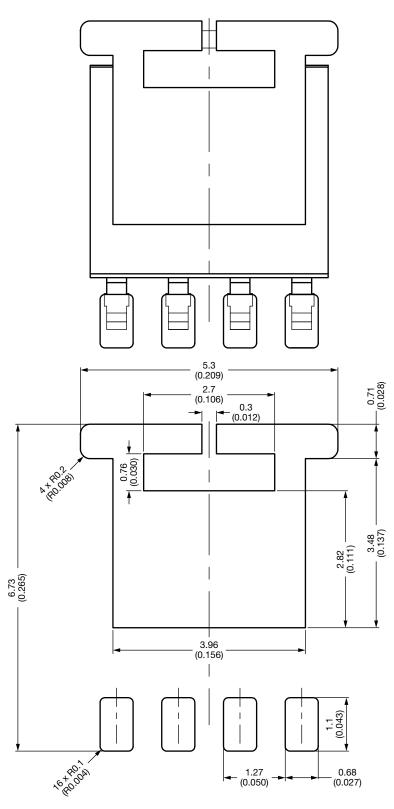
DIM.	MILLIMETERS			INCHES			
DIN.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.00	1.05	1.10	0.039	0.041	0.043	
A1	0.00		0.127	0.000		0.005	
b	0.33	0.41	0.49	0.013	0.016	0.019	
b1	0.43	0.51	0.59	0.017	0.020	0.023	
b2	4.00	4.10	4.20	0.157	0.161	0.165	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D5	0.51	0.61	0.71	0.020	0.024	0.028	
D6	2.64	2.74	2.84	0.104	0.108	0.112	
е		1.27 BSC		0.050 BSC			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
E3	3.48	3.58	3.68	0.137	0.141	0.145	
E4	2.72	2.82	2.92	0.107	0.111	0.115	
E5	0.71	0.81	0.91	0.028	0.032	0.036	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
W1	0.31	0.41	0.51	0.012	0.016	0.020	
W4	0.31	0.36	0.41	0.012	0.014	0.016	
z1	0.37	0.47	0.57	0.015	0.019	0.022	
z2	0.99	1.09	1.19	0.039	0.043	0.047	
θ	0°		5°	0°		5°	

Note

• Millimeter will govern



# **Recommended Land Pattern PowerPAK® SO-8L Single Short Ear**



Dimensions in Millimeters (Inches)

Revision: 24-Aug-2021

Document Number: 78020



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