

**Features**

- High speed
  - 15 ns
- Fast  $t_{DOE}$
- Low active power
  - 715 mW
- Low standby power
  - 85 mW
- CMOS for optimum speed/power
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- Available in non Pb-free 28-pin (300-Mil) Molded SOJ, 28-pin (300-Mil) Molded SOIC and Pb-free 28-pin (300-Mil) Molded DIP

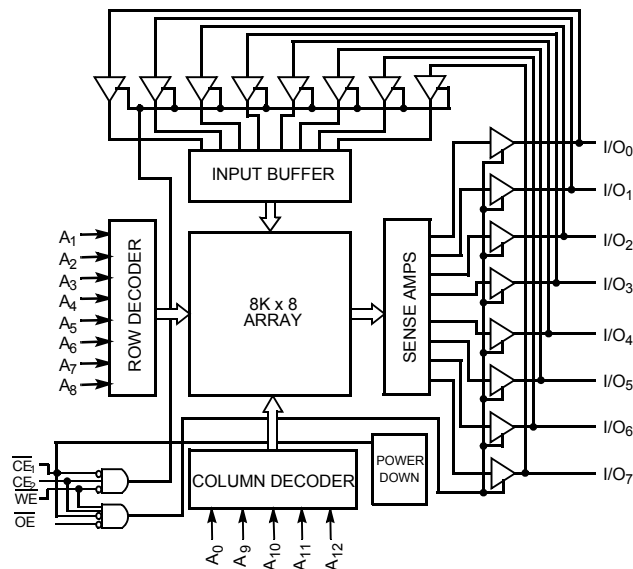
**Functional Description**

The CY7C185<sup>[1]</sup> is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), and active LOW output enable ( $\overline{OE}$ ) and tri-state drivers. This device has an automatic power-down feature ( $\overline{CE}_1$  or  $CE_2$ ), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP, SOJ, or SOIC package.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}_1$  and  $\overline{WE}$  inputs are both LOW and  $CE_2$  is HIGH, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{12}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}_1$  and  $\overline{OE}$  active LOW,  $CE_2$  active HIGH, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input or output pins.

The input or output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. A die coat is used to insure alpha immunity.

**Logic Block Diagram**



**Note**

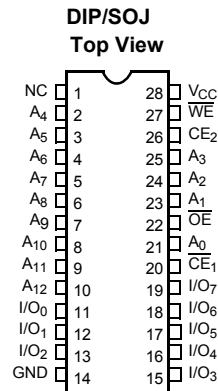
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configuration

Figure 1. 28-pin DIP / SOJ pinout (Top View)



## Selection Guide

Description	-15	-20	-35
Maximum Access Time (ns)	15	20	35
Maximum Operating Current (mA)	130	110	100
Maximum CMOS Standby Current (mA)	15	15	15

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage to ground potential .....	-0.5 V to +7.0 V
DC voltage applied to outputs in High Z State <sup>[2]</sup> .....	-0.5 V to +7.0 V
DC input voltage <sup>[2]</sup> .....	-0.5 V to +7.0 V

Output current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	>2001 V
Latch-up current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	5 V ± 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		-20		-35		Unit
			Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	2.4	-	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA	-	0.4	-	0.4	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	-	130	-	110	-	100	mA
I <sub>SB1</sub>	Automatic Power-down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ , Min. Duty Cycle = 100%	-	40	-	20	-	20	mA
I <sub>SB2</sub>	Automatic Power-down Current	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3$ V or $CE_2 \leq 0.3$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V	-	15	-	15	-	15	mA

### Note

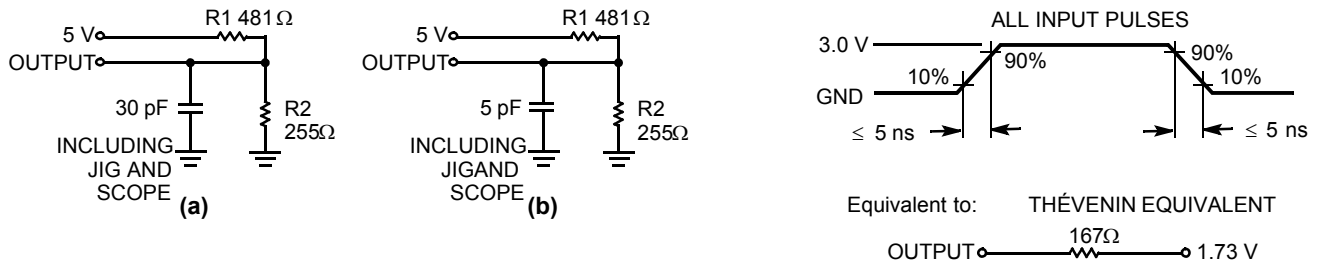
- Minimum voltage is equal to -3.0 V for pulse durations less than 30 ns.

### Capacitance

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	7	pF
C <sub>OUT</sub>	Output capacitance		7	pF

### AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



**Note**

3. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[4]</sup>	Description	-15		-20		-35		Unit
		Min	Max	Min	Max	Min	Max	
<b>Read Cycle</b>								
$t_{RC}$	Read Cycle Time	15	–	20	–	35	–	ns
$t_{AA}$	Address to Data Valid	–	15	–	20	–	35	ns
$t_{OHA}$	Data Hold from Address Change	3	–	5	–	5	–	ns
$t_{ACE1}$	$\overline{CE}_1$ LOW to Data Valid	–	15	–	20	–	35	ns
$t_{ACE2}$	$CE_2$ HIGH to Data Valid	–	15	–	20	–	35	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	8	–	9	–	15	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	3	–	3	–	3	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[5]</sup>	–	7	–	8	–	10	ns
$t_{LZCE1}$	$\overline{CE}_1$ LOW to Low Z <sup>[6]</sup>	3	–	5	–	5	–	ns
$t_{LZCE2}$	$CE_2$ HIGH to Low Z	3	–	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH to High Z <sup>[5, 6]</sup> $CE_2$ LOW to High Z	–	7	–	8	–	10	ns
$t_{PU}$	$\overline{CE}_1$ LOW to Power-up $CE_2$ to HIGH to Power-up	0	–	0	–	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH to Power-down $CE_2$ LOW to Power-down	–	15	–	20	–	20	ns
<b>Write Cycle <sup>[7, 8]</sup></b>								
$t_{WC}$	Write Cycle Time	15	–	20	–	35	–	ns
$t_{SCE1}$	$\overline{CE}_1$ LOW to Write End	12	–	15	–	20	–	ns
$t_{SCE2}$	$CE_2$ HIGH to Write End	12	–	15	–	20	–	ns
$t_{AW}$	Address Setup to Write End	12	–	15	–	25	–	ns
$t_{HA}$	Address Hold from Write End	0	–	0	–	0	–	ns
$t_{SA}$	Address Setup to Write Start	0	–	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12	–	15	–	20	–	ns
$t_{SD}$	Data Setup to Write End	8	–	10	–	12	–	ns
$t_{HD}$	Data Hold from Write End	0	–	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5]</sup>	–	7	–	7	–	8	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	3	–	5	–	5	–	ns

### Notes

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady state voltage.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE1}$  and  $t_{LZCE2}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle pulse width of Write cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum  $t_{HZWE}$  and  $t_{SD}$ .

### Switching Waveforms

Figure 3. Read Cycle No. 1 [9, 10]

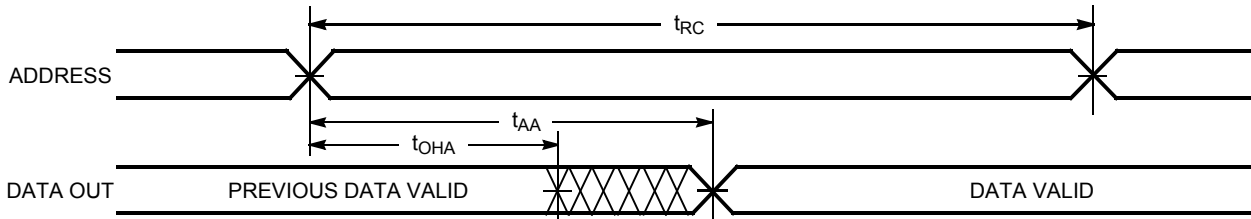
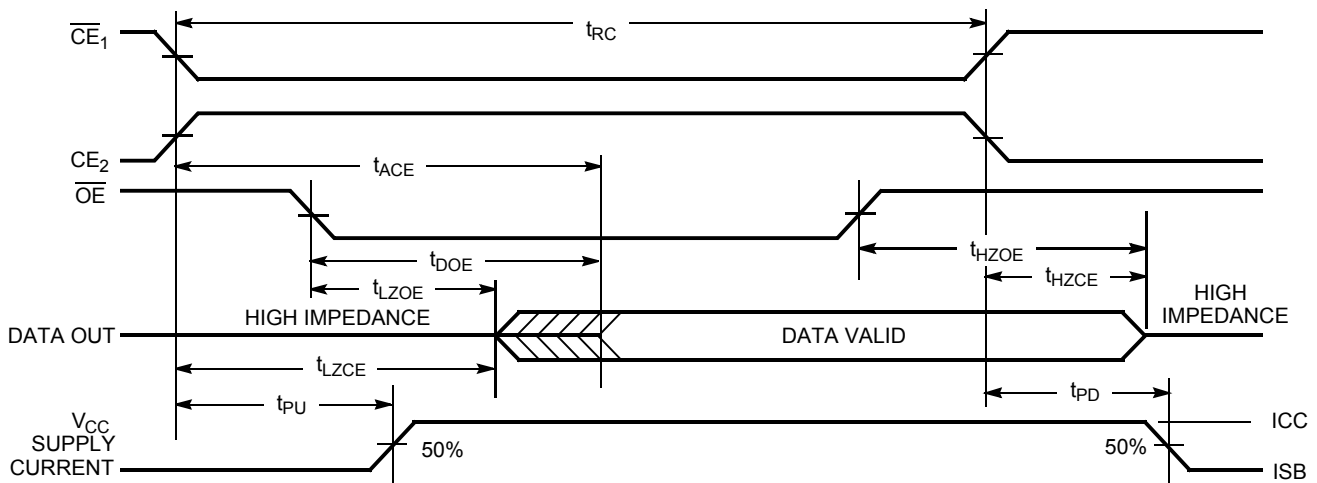


Figure 4. Read Cycle No. 2 [11, 12]



**Notes**

- 9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ .  $CE_2 = V_{IH}$ .
- 10.  $\overline{WE}$  is HIGH for read cycle.
- 11. Data I/O is High Z if  $\overline{OE} = V_{IH}$ ,  $\overline{CE}_1 = V_{IH}$ ,  $\overline{WE} = V_{IL}$ , or  $CE_2 = V_{IL}$ .
- 12. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  must be HIGH to initiate write. A write can be terminated by  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH or  $CE_2$  going LOW. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [13, 14]

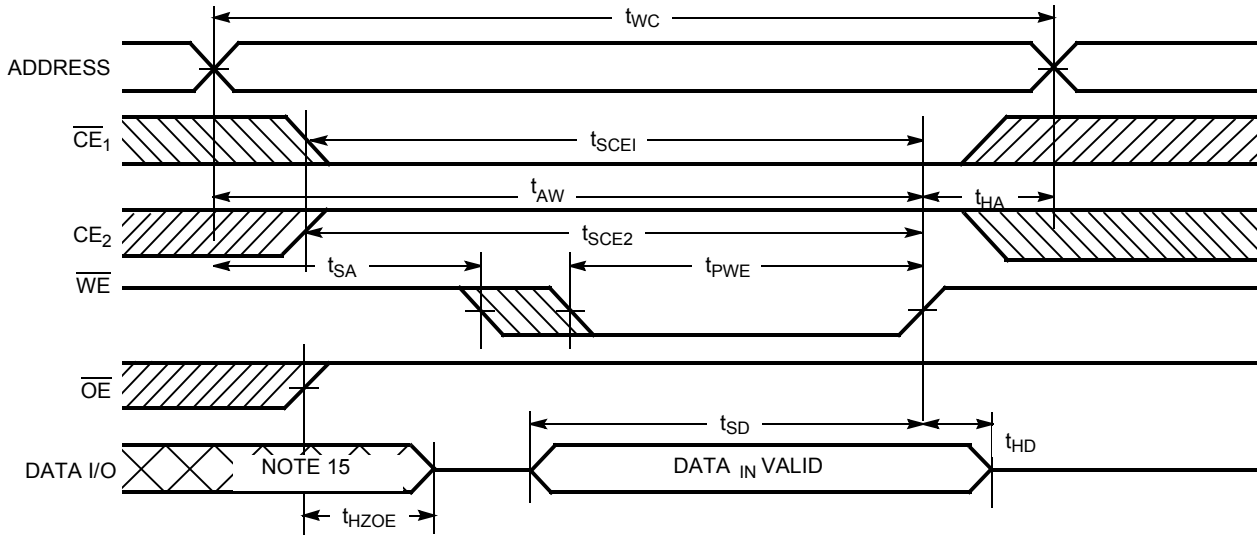
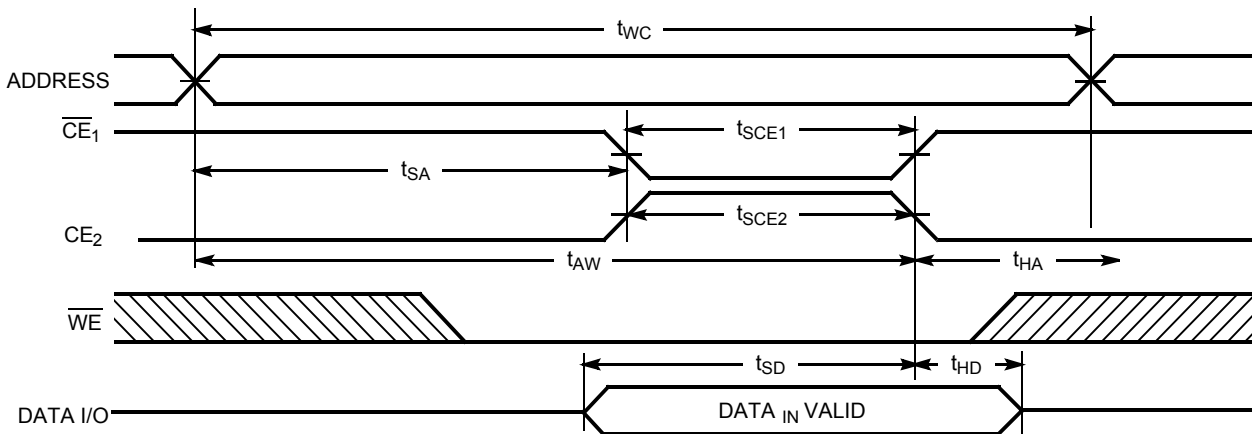


Figure 6. Write Cycle No. 2 ( $\overline{CE}$  Controlled) [14, 15, 16]



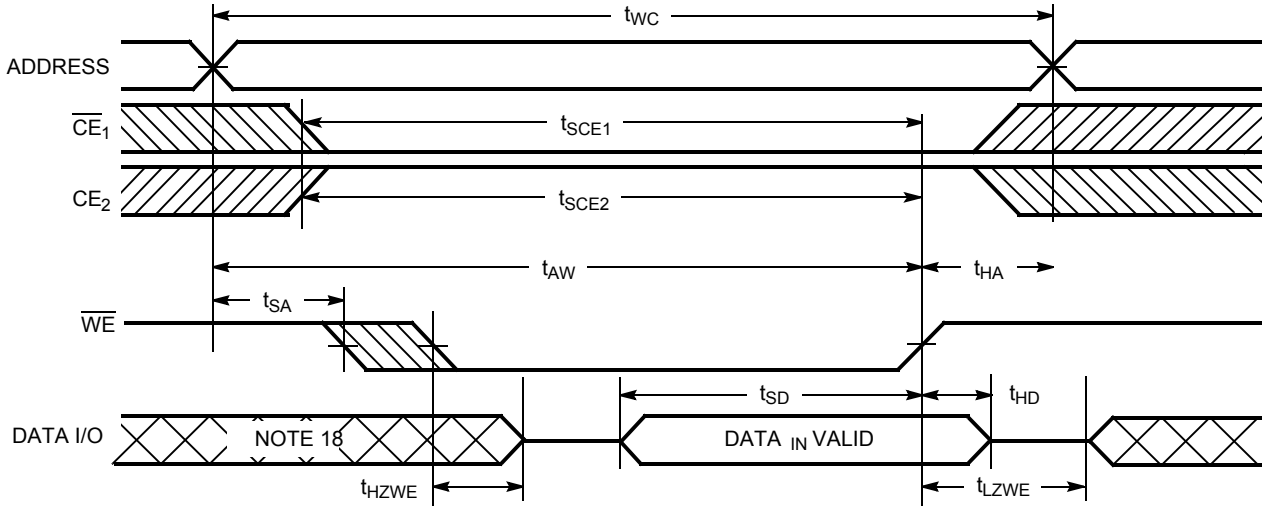
Notes

- 13.  $\overline{WE}$  is HIGH for read cycle.
- 14. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $CE_2$  HIGH and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $CE_2$  must be HIGH to initiate write. A write can be terminated by  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH or  $CE_2$  going LOW. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.
- 15. During this period, the I/Os are in the output state and input signals must not be applied.
- 16. The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .



Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [17, 19, 20]



Notes

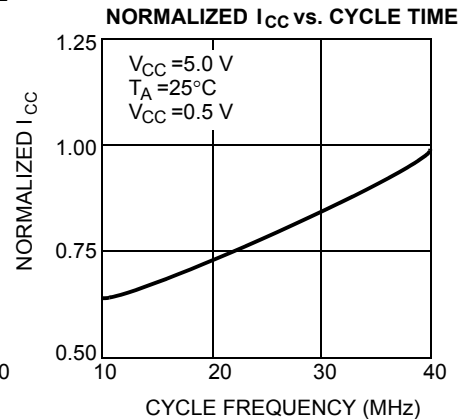
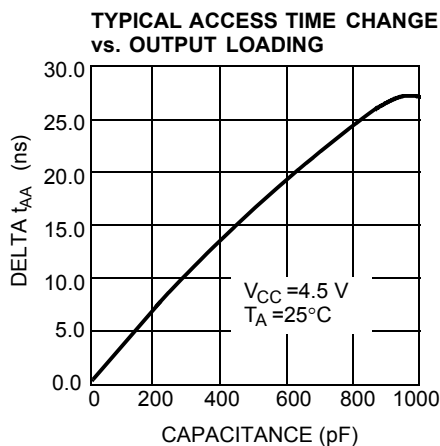
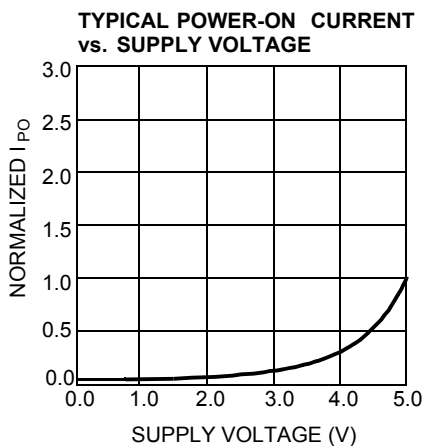
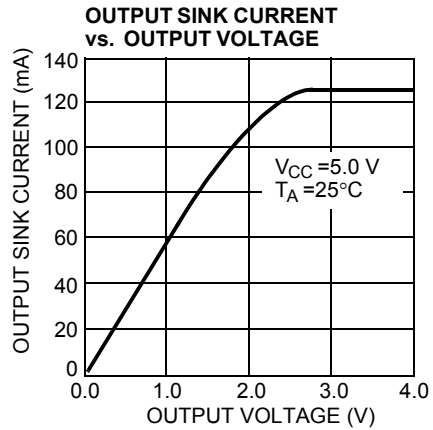
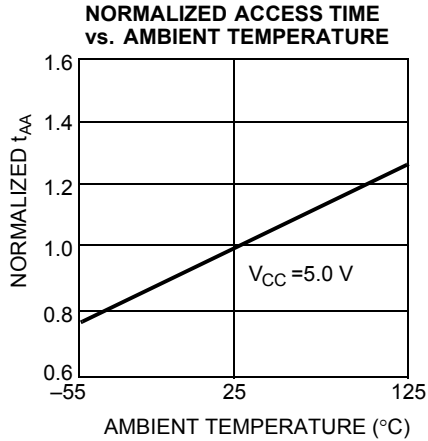
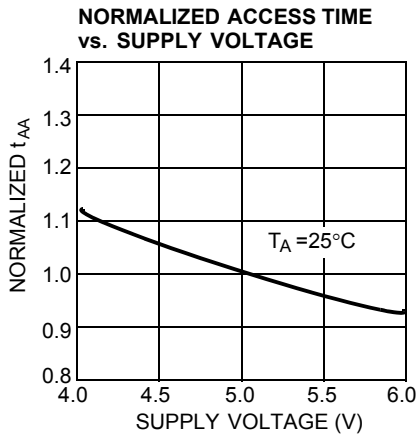
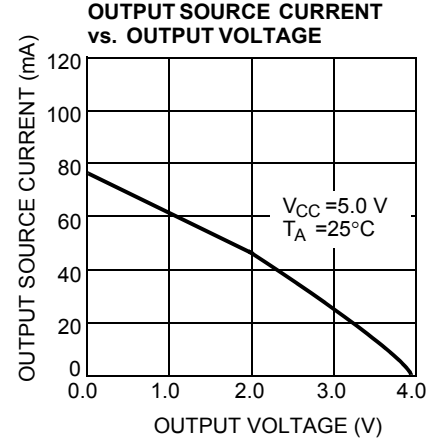
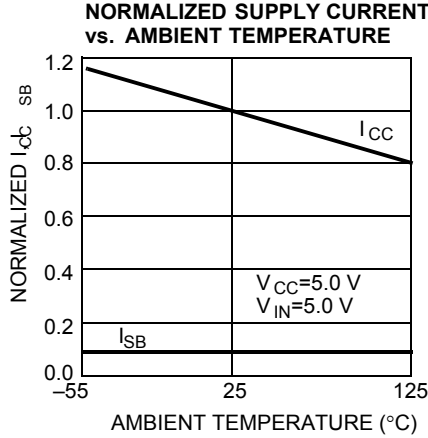
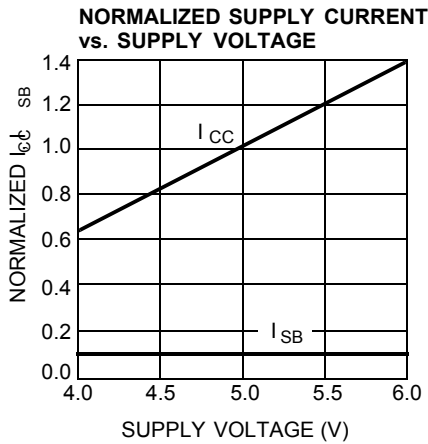
17. The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and  $\overline{WE}$  LOW.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW and  $\overline{CE}_2$  must be HIGH to initiate write. A write can be terminated by  $\overline{CE}_1$  or  $\overline{WE}$  going HIGH or  $\overline{CE}_2$  going LOW. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

18. During this period, the I/Os are in the output state and input signals must not be applied.

19. The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

20. If  $\overline{CE}_1$  goes HIGH or  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	X	High Z	Deselect/ Power-down
X	L	X	X	High Z	Deselect/ Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

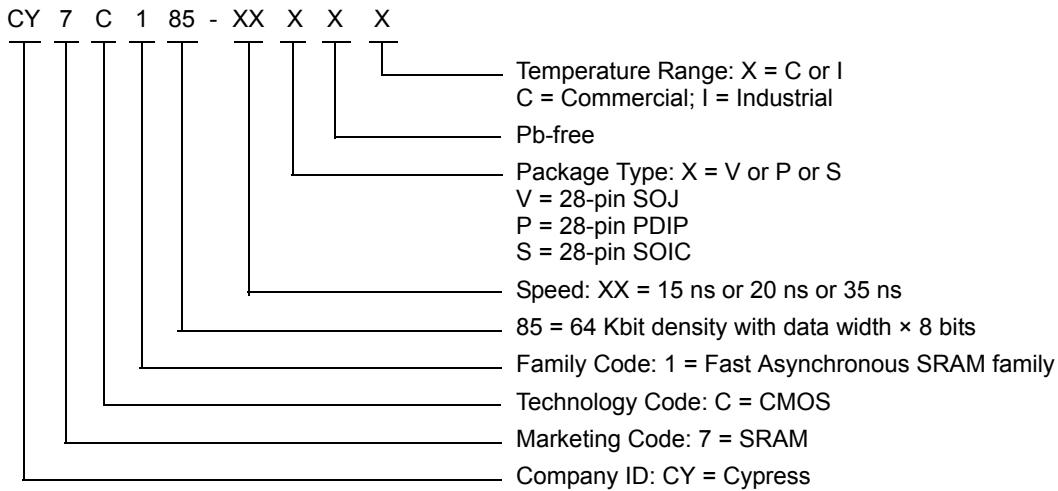
**Address Designators**

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

**Ordering Information**

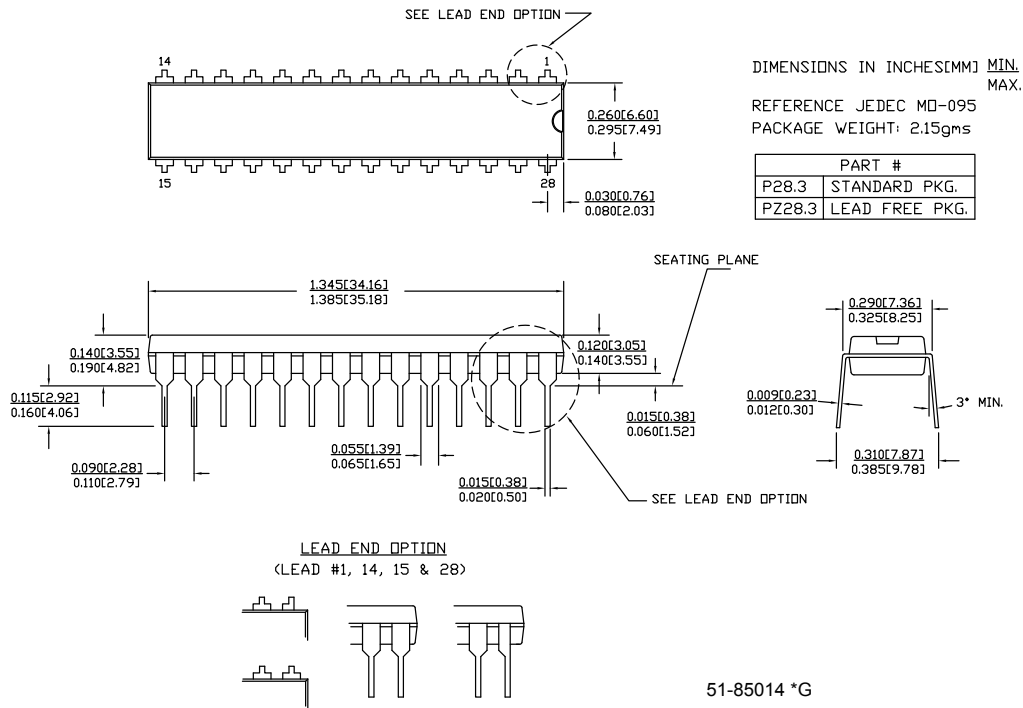
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185-15VI	51-85031	28-pin SOJ	Industrial
20	CY7C185-20PXC	51-85014	28-pin PDIP (Pb-free)	Commercial
35	CY7C185-35SC	51-85026	28-pin SOIC	Commercial

**Ordering Code Definitions**



Package Diagrams

Figure 8. 28-pin PDIP (300 Mil) Package Outline, 51-85014

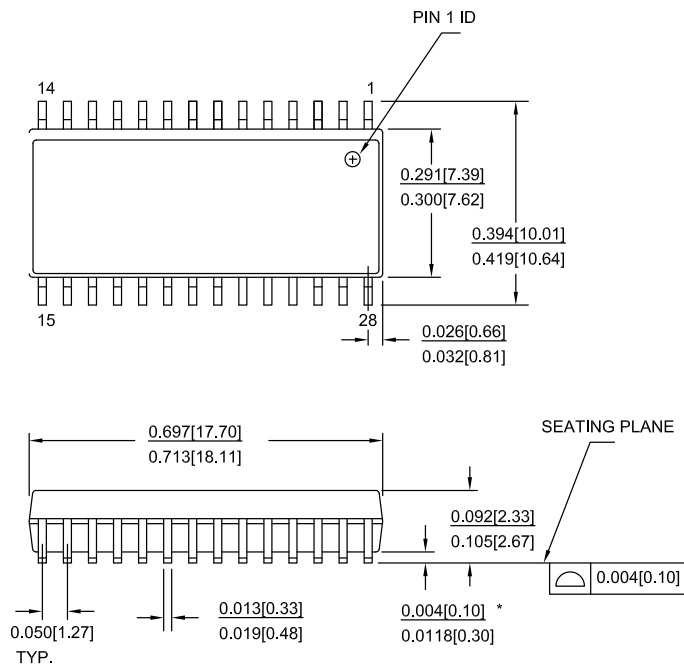


Package Diagrams (continued)

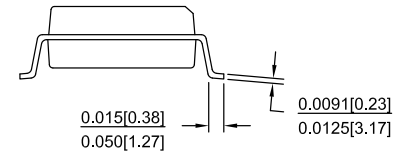
Figure 9. 28-pin SOIC (0.713 × 0.300 × 0.0932 Inches) Package Outline, 51-85026

NOTE :

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



PART #	
S28.3	STANDARD PKG.
SZ28.3	LEAD FREE PKG.
SX28.3	LEAD FREE PKG.



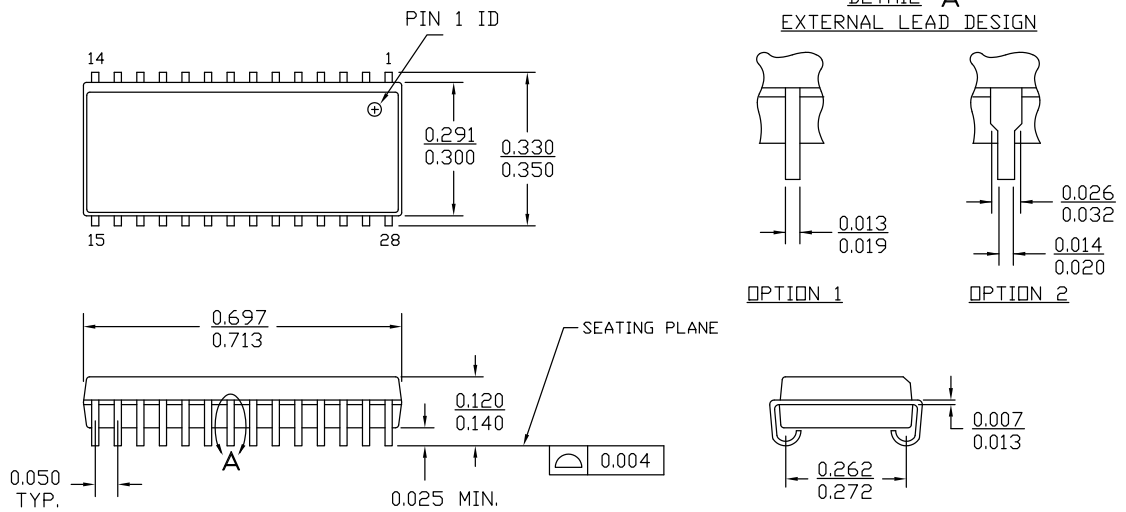
51-85026 \*H

Package Diagrams (continued)

Figure 10. 28-pin SOJ (300 Mils) Package Outline, 51-85031

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



51-85031 \*E

### Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt



Document History Page

Document Title: CY7C185, 64-Kbit (8 K × 8) Static RAM Document Number: 38-05043				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	107145	09/10/01	SZV	Change from Spec number: 38-00037 to 38-05043
*A	116470	09/16/02	CEA	Add applications foot note to data sheet
*B	486744	See ECN	NXR	Changed Low standby power from 220 mW to 85 mW  Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I <sub>OS</sub> parameter from DC Electrical Characteristics table  Updated the Ordering Information table
*C	2263686	See ECN	VKN / AESA	Removed 25 ns speed bin  Updated the Ordering Information table as per the current product offerings
*D	3105329	12/09/2010	AJU	Added <a href="#">Ordering Code Definitions</a> .  Updated <a href="#">Package Diagrams</a> .
*E	3235800	04/20/2011	PRAS	Updated package diagram spec 51-85026 to *F.  Added Acronyms and Units of Measure.  Template changes.
*F	4383597	05/19/2014	VINI	Updated <a href="#">Switching Characteristics</a> : Added Note 8 and referred the same note in "Write Cycle".  Updated <a href="#">Package Diagrams</a> : spec 51-85014 – Changed revision from *E to *G. spec 51-85026 – Changed revision from *F to *H. spec 51-85031 – Changed revision from *D to *E.  Updated in new template.  Completing Sunset Review.

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