SiR846BDP Vishay Siliconix

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PRODUCT SUMMARY

V _{DS} (V)	100
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.0080
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.0090
Q _g typ. (nC)	26.5
I _D (A)	65.8
Configuration	Single

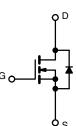
FEATURES

N-Channel 100 V (D-S) MOSFET

- TrenchFET[®] Gen IV power MOSFET
- Very low R_{DS} x Q_g figure-of-merit (FOM)
- Tuned for the lowest R_{DS} x Q_{oss} FOM
- 100 % R_{q} and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous rectification
- · Primary side switch
- DC/DC converters
- Power supplies
- Motor drive control



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR846BDP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	v	
Gate-source voltage		V _{GS}	± 20		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		65.8		
	T _C = 70 °C		52.6		
	T _A = 25 °C	I _D	16.1 ^{b, c}		
	T _A = 70 °C		12.9 ^{b, c}		
Pulsed drain current (t = 100 µs)		I _{DM}	150	— A	
	T _C = 25 °C		75.7		
Continuous source-drain diode current	T _A = 25 °C	I _S	4.5 ^{b, c}		
Single pulse avalanche current		I _{AS}	30		
Single pulse avalanche energy $L = 0.1 \text{ mH}$		E _{AS}	45	mJ	
	T _C = 25 °C		83.3		
Maximum power dissipation	T _C = 70 °C		53.3	W	
	T _A = 25 °C	P _D	5 b, c		
	T _A = 70 °C		3.2 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	•••	
Soldering recommendations (peak temperature) c			260	°C	

THERMAL RESISTANCE RATIN	GS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.2	1.5	0/10

Notes

a. Package limitedb. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 65 °C/W

g. T_C = 25 °C

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SiR846BDP

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•			
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_D = 1 mA$	100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 1 mA	-	63	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-7.3	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2	-	4	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	100	nA
Zara gata valtaga drain aurrant		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	
Zero gate voltage drain current	IDSS	V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 70 °C	-	-	15	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \geq$ 10 V, V_{GS} =10 V	40	-	-	Α
Ducin actures on state resistance à	D	V _{GS} = 10 V, I _D = 15 A - 0.0066		0.0066	0.0080	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.0074	0.0090	Ω
Forward transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	-	72	-	S
Dynamic ^b	· · · ·					
Input capacitance	C _{iss}		-	2440	-	
Output capacitance	C _{oss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	-	255	-	pF
Reverse transfer capacitance	C _{rss}		-	16.2	-	
Total acta charge	0	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$	-	34.5	52	
Total gate charge	Q _g		-	26.5	40	
Gate-source charge	Q _{gs}	$V_{DS}=50$ V, $V_{GS}=7.5$ V, $I_{D}=15$ A	-	12	-	nC
Gate-drain charge	Q _{gd}		-	5.3	-	
Output charge	Q _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	46	-	
Gate resistance	Rg	f = 1 MHz	0.3	0.8	1.4	Ω
Turn-on delay time	t _{d(on)}		-	15	30	
Rise time	t _r	V_{DD} = 50 V, R_L = 3.33 Ω , $I_D \cong$ 15 A,	-	7	14	
Turn-off delay time	t _{d(off)}	$V_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	25	50]
Fall time	t _f		-	6	12	
Turn-on delay time	t _{d(on)}		-	18	36	ns
Rise time	tr	$V_{DD}=50~V,~R_L=3.33~\Omega,~I_D\cong15~A,$	-	8	16	
Turn-off delay time	t _{d(off)}	V_{GEN} = 7.5 V, R_g = 1 Ω	-	22	44	
Fall time	t _f		-	7	14	
Drain-Source Body Diode Characteristi	cs					
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	65.8	^
Pulse diode forward current	I _{SM}			150	A	
Body diode voltage	V _{SD}	$I_{S} = 5 \text{ A}, \text{ V}_{GS} = 0 \text{ V}$	-	0.75	1.1	V
Body diode reverse recovery time	t _{rr}		-	42	84	ns
Body diode reverse recovery charge	Q _{rr}	I _F = 10 A, di/dt = 100 A/µs,	-	55	110	nC
Reverse recovery fall time	ta	$T_J = 25 \ ^{\circ}C$	-	26	-	
Reverse recovery rise time	t _b		-	16	-	ns

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

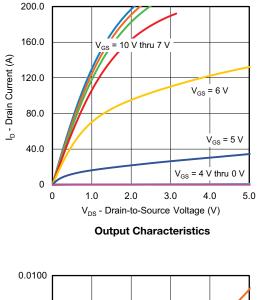
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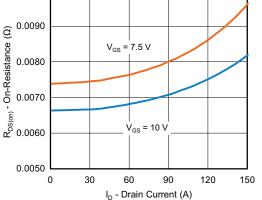


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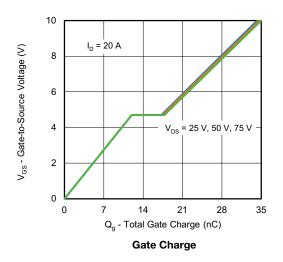
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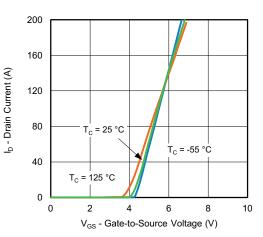
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



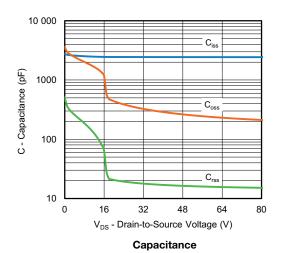


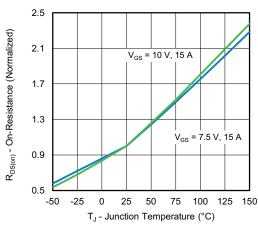
On-Resistance vs. Drain Current and Gate Voltage





Transfer Characteristics





On-Resistance vs. Junction Temperature

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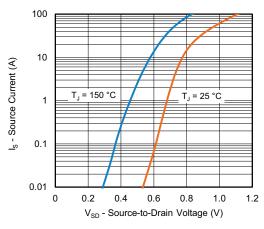
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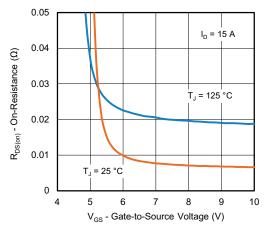


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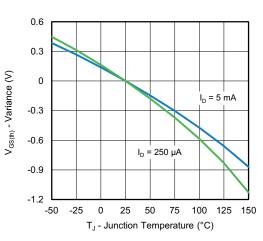
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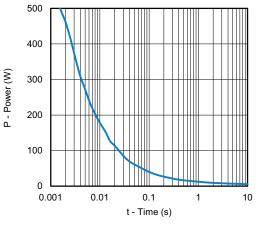
Source-Drain Diode Forward Voltage



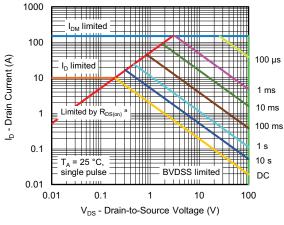
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

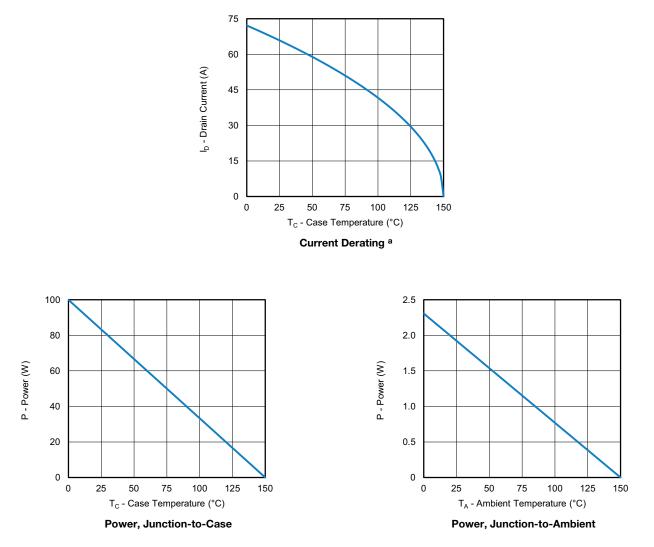
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



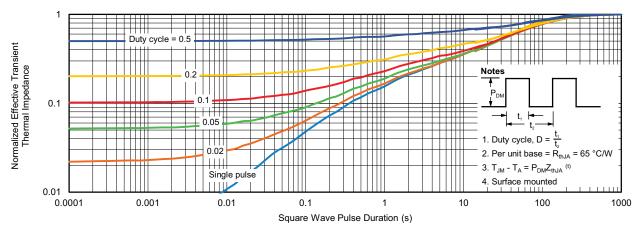
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

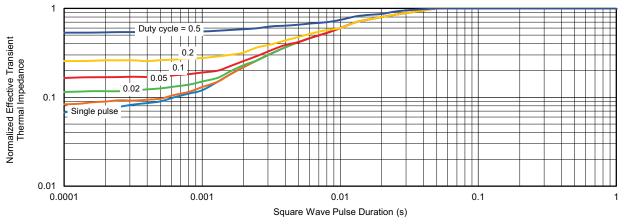


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77275.

D2

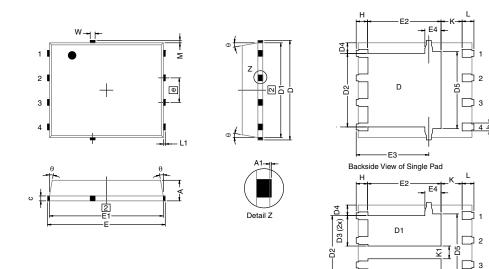
E3

Backside View of Dual Pad



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PowerPAK[®] SO-8, (Single/Dual)



Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

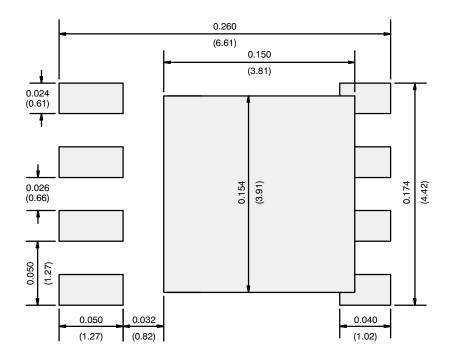
5.14		MILLIMETERS			INCHES		
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX	
А	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4		0.57 typ.			0.0225 typ.		
D5		3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4		0.75 typ.			0.030 typ.		
е		1.27 BSC			0.050 BSC		
К		1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М		0.125 typ.			0.005 typ.		



Application Note 826

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RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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