







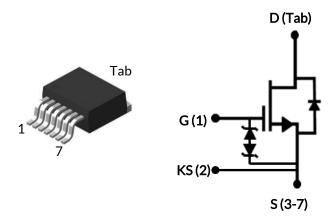








# JJ4SC075009B7S



Part Number	Package	Marking
UJ4SC075009B7S	D <sup>2</sup> PAK-7L	UJ4SC075009B7S







### 750V-9m $\Omega$ SiC FET

Rev. A, January 2022

### Description

The UJ4SC075009B7S is a 750V,  $9m\Omega$  G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D<sup>2</sup>PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

#### **Features**

- On-resistance R<sub>DS(on)</sub>: 9mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q<sub>rr</sub> = 338nC
- ◆ Low body diode V<sub>FSD</sub>: 1.1V
- ◆ Low gate charge: Q<sub>G</sub> =75nC
- Threshold voltage V<sub>G(th)</sub>: 4.5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected, HBM class 2
- D<sup>2</sup>PAK-7L package for faster switching, clean gate waveforms

### Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













## **Maximum Ratings**

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		750	V
Gate-source voltage	V	DC	-20 to +20	V
	V <sub>GS</sub>	AC (f > 1Hz)	-25 to +25	V
Continuous drain current <sup>1</sup>		T <sub>C</sub> < 61°C	106	Α
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> = 100°C	86	Α
Pulsed drain current <sup>2</sup>	I <sub>DM</sub>	T <sub>C</sub> = 25°C	344	Α
Single pulsed avalanche energy <sup>3</sup>	E <sub>AS</sub>	$L=15mH, I_{AS} = 5.2A$	202	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \le 500V$	100	V/ns
Power dissipation	P <sub>tot</sub>	T <sub>C</sub> = 25°C	375	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	$T_J,T_STG$		-55 to 175	°C
Reflow soldering temperature	$T_{solder}$	reflow MSL 1	245	°C

- 1. Limited by bondwires
- 2. Pulse width  $t_p$  limited by  $T_{J,max}$
- 3. Starting  $T_J = 25^{\circ}C$

### **Thermal Characteristics**

Parameter	Symbol	Test Conditions		Limita		
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.31	0.40	°C/W















# Electrical Characteristics (T<sub>J</sub> = +25°C unless otherwise specified)

# **Typical Performance - Static**

Parameter	Symbol	Test Conditions		Units		
rai ailietei			Min	Тур	Max	UIIILS
Drain-source breakdown voltage	BV <sub>DS</sub>	$V_{GS}$ =0V, $I_D$ =1mA	750			V
Total drain leakage current  Total gate leakage current		V <sub>DS</sub> =750V,		4	84	- μΑ
	I <sub>DSS</sub>	$V_{GS}=0V, T_J=25$ °C				
Total di alli leakage cull'elit	DSS	V <sub>DS</sub> =750V,		35		
Total gate leakage current		$V_{GS}=0V, T_{J}=175^{\circ}C$				
Total gata leakage surrent	I <sub>GSS</sub>	V <sub>DS</sub> =0V, T <sub>J</sub> =25°C,		2	±20	μА
l otal gate leakage current		V <sub>GS</sub> =-20V / +20V				
	R <sub>DS(on)</sub>	V <sub>GS</sub> =12V, I <sub>D</sub> =70A,		9	11.5	mΩ
		T <sub>J</sub> =25°C				
Drain-source on-resistance		$V_{GS}$ =12V, $I_{D}$ =70A,		14.8		
Drain-source on-resistance		T <sub>J</sub> =125°C				
		V <sub>GS</sub> =12V, I <sub>D</sub> =70A,		10.4		
		175°C رT		19.4		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}$ =5V, $I_{D}$ =10mA	3.5	4.5	5.5	V
Gate resistance	$R_{G}$	f=1MHz, open drain		2.3		Ω

# Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Units			
			Min	Тур	Max	UTILS	
Diode continuous forward current <sup>1</sup>	I <sub>S</sub>	T <sub>C</sub> < 61°C			106	Α	
Diode pulse current <sup>2</sup>	I <sub>S,pulse</sub>	T <sub>C</sub> =25°C			344	Α	
Forward voltage	V <sub>FSD</sub>	V <sub>GS</sub> =0V, I <sub>F</sub> =35A, T <sub>J</sub> =25°C		1.10	1.24	V	
		V <sub>GS</sub> =0V, I <sub>F</sub> =35A, T <sub>J</sub> =175°C		1.14			
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, $I_F$ =70A, $V_{GS}$ =0V, $R_{G\_EXT}$ =33 $\Omega$		338		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=2500A/μs, T <sub>J</sub> =25°C		29		ns	
Reverse recovery charge	Q <sub>rr</sub>	$V_R$ =400V, $I_F$ =70A, $V_{GS}$ =0V, $R_{G\_EXT}$ =33 $\Omega$		375		nC	
Reverse recovery time	t <sub>rr</sub>	di/dt=2500A/μs, Τ <sub>J</sub> =150°C		32		ns	













## Typical Performance - Dynamic

Parameter	C. w. d d	Total Constitutions	Value			
	Symbol	Test Conditions	Min	Тур	Max	Units
Input capacitance	$C_{iss}$	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		3340		
Output capacitance	$C_{oss}$	f=100kHz		230		pF
Reverse transfer capacitance	$C_{rss}$	L= TOOKHZ		1.4		
Effective output capacitance, energy related	$C_{oss(er)}$	V <sub>DS</sub> =0V to 400V, V <sub>GS</sub> =0V		286		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}$ =0V to 400V, $V_{GS}$ =0V		605		pF
C <sub>OSS</sub> stored energy	E <sub>oss</sub>	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V		23		μЈ
Total gate charge	$Q_{G}$	V <sub>DS</sub> =400V, I <sub>D</sub> =70A,		75		
Gate-drain charge	$Q_{GD}$	$V_{DS} = 400 \text{ V}, V_{D} = 700 \text{ A},$ $V_{GS} = 0 \text{ V to } 15 \text{ V}$		13		nC
Gate-source charge	$Q_{GS}$	V <sub>GS</sub> - 0V to 13V		22		
Turn-on delay time	$t_{d(on)}$			17		- ns
Rise time	t <sub>r</sub>	Notes 4 and 5, $V_{DS}$ =400V, $I_D$ =70A, Gate		25		
Turn-off delay time	t <sub>d(off)</sub>	$V_{DS}=400V, I_D=70A, Gate$ $Driver = 0V to +15V,$ $Turn-on R_{G,EXT}=1\Omega,$ $Turn-off R_{G,EXT}=5\Omega,$ $inductive Load, FWD:$ $same device with V_{GS}=0V$ $and R_G=5\Omega, RC snubber:$ $R_S=5\Omega and C_S=560pF,$ $T_1=25°C$		65		
Fall time	t <sub>f</sub>			14		
Turn-on energy including R <sub>S</sub> energy	E <sub>ON</sub>			220		_
Turn-off energy including R <sub>S</sub> energy	E <sub>OFF</sub>			181		
Total switching energy	E <sub>TOTAL</sub>			401		μJ
Snubber R <sub>S</sub> energy during turn-on	E <sub>RS_ON</sub>			13		
Snubber R <sub>S</sub> energy during turn-off	E <sub>RS_OFF</sub>			50		1
Turn-on delay time	t <sub>d(on)</sub>			18		ns
Rise time	t <sub>r</sub>	Notes 4 and 5,		28		
Turn-off delay time	t <sub>d(off)</sub>	$V_{DS}\!=\!400V, I_{D}\!=\!70A, Gate$ $Driver=\!0V\ to +\!15V,$ $Turn-on\ R_{G,EXT}\!=\!1\Omega,$ $Turn-off\ R_{G,EXT}\!=\!5\Omega,$ inductive Load, FWD: same device with $V_{GS}=0V$ and $R_{G}=5\Omega, RC\ snubber:$ $R_{S}\!=\!5\Omega\ and\ C_{S}\!=\!560pF,$ $T_{J}\!=\!150^{\circ}C$		68		
Fall time	t <sub>f</sub>			13		
Turn-on energy including R <sub>S</sub> energy	E <sub>ON</sub>			245		
Turn-off energy including R <sub>S</sub> energy	E <sub>OFF</sub>			211		
Total switching energy	E <sub>TOTAL</sub>			456		μJ
Snubber R <sub>S</sub> energy during turn-on	E <sub>RS_ON</sub>			13		
Snubber R <sub>S</sub> energy during turn-off	E <sub>RS_OFF</sub>			50		

<sup>4.</sup> Measured with the switching test circuit in Figure 26.

<sup>5.</sup> In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.













#### **Typical Performance Diagrams**

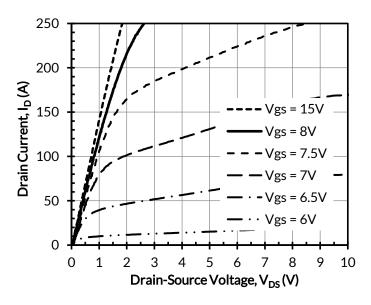


Figure 1. Typical output characteristics at  $T_J = -55$ °C, tp < 250 $\mu$ s

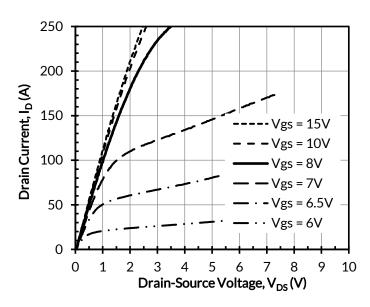


Figure 2. Typical output characteristics at  $T_J = 25$ °C, tp < 250µs

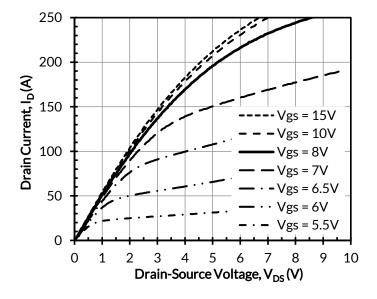


Figure 3. Typical output characteristics at  $T_J$  = 175°C, tp < 250 $\mu$ s

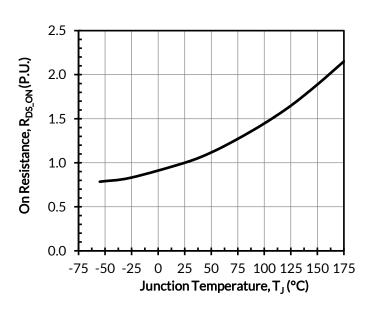


Figure 4. Normalized on-resistance vs. temperature at  $V_{GS}$  = 12V and  $I_D$  = 70A





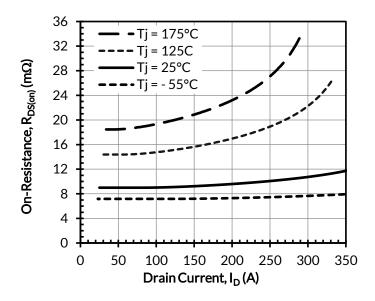








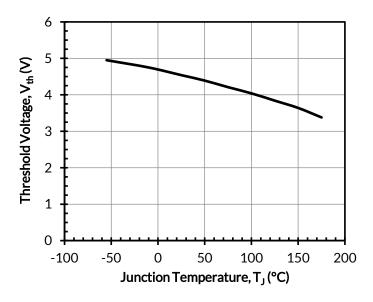




200 Tj = -55°C 175 Tj = 25°C 150 Tj = 175°C Drain Current, I<sub>D</sub> (A) 125 100 75 50 25 0 5 7 8 0 3 4 6 9 10 Gate-Source Voltage,  $V_{GS}(V)$ 

Figure 5. Typical drain-source on-resistances at  $V_{GS}$  = 12V

Figure 6. Typical transfer characteristics at  $V_{DS} = 5V$ 



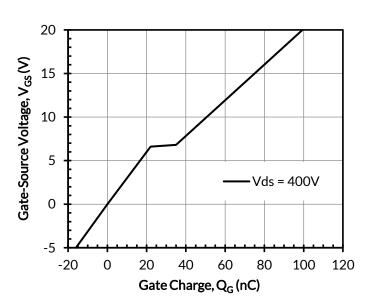


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS}$  = 5V and  $I_D$  = 10mA

Figure 8. Typical gate charge at  $I_D = 70A$ 



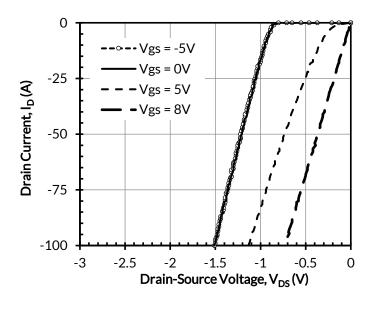








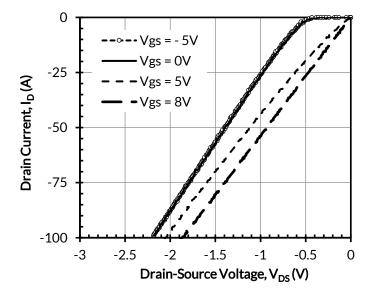




0 **--** Vgs = - 5V Vgs = 0V -25 **-** Vgs = 5V Drain Current, I<sub>D</sub> (A) • Vgs = 8V -50 -75 -100 -3 -2.5 -2 -1.5 -1 -0.5 Drain-Source Voltage, V<sub>DS</sub> (V)

Figure 9. 3rd quadrant characteristics at  $T_J = -55$ °C

Figure 10. 3rd quadrant characteristics at T<sub>J</sub> = 25°C



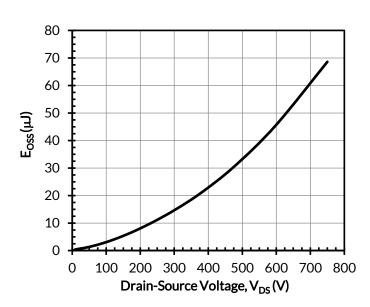


Figure 11. 3rd quadrant characteristics at  $T_J = 175$ °C

Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0V$ 



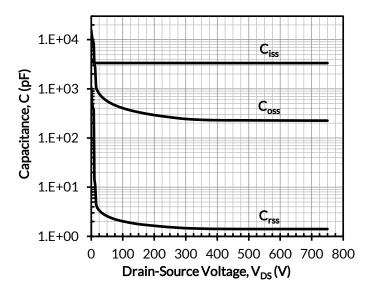








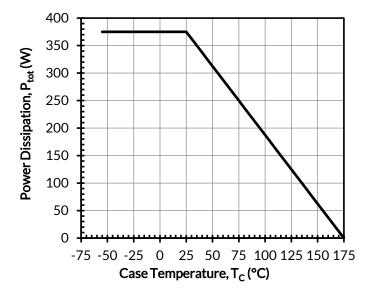




120 100 80 40 20 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T<sub>C</sub> (°C)

Figure 13. Typical capacitances at f = 100kHz and  $V_{GS}$  = 0V

Figure 14. DC drain current derating



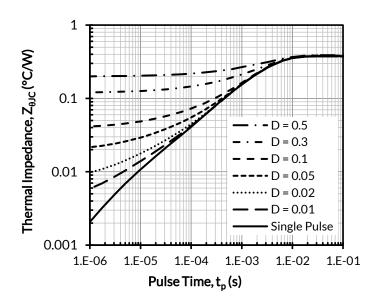


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













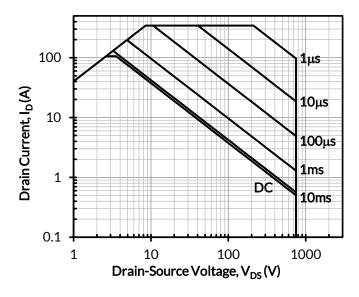


Figure 17. Safe operation area at  $T_C$  = 25°C, D = 0, Parameter  $t_o$ 

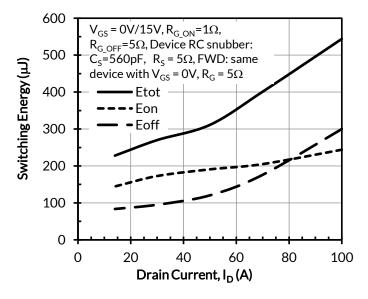


Figure 19. Clamped inductive switching energy vs. drain current at  $V_{DS}$  = 400V and  $T_J$  = 25°C

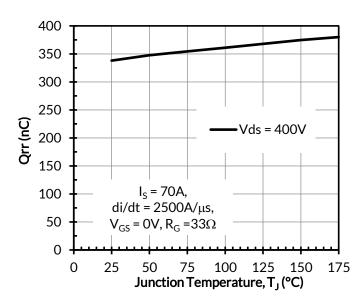


Figure 18. Reverse recovery charge Qrr vs. junction temperature

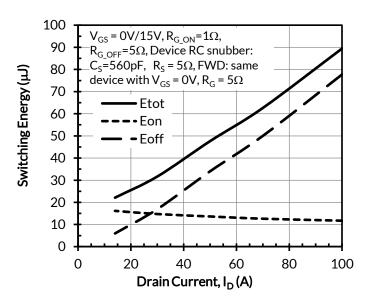


Figure 20. RC snubber energy loss vs. drain current at  $V_{DS}$  = 400V and  $T_J$  = 25°C



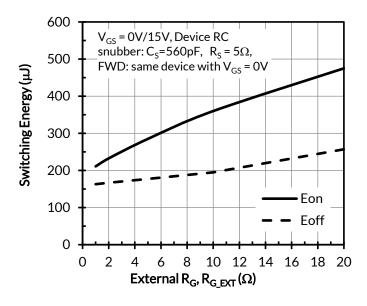








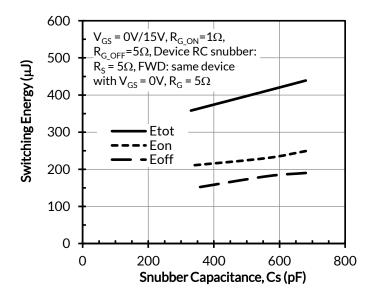




70 Rs\_Eon 60 - Rs\_Eoff Snubber R<sub>s</sub> Energy (μJ) 50 40  $V_{GS}$  = 0V/15V, Device RC snubber:  $C_S = 560 pF$ ,  $R_S = 5\Omega$ , FWD: same device with  $V_{GS} = 0V$ 30 20 10 0 2 8 10 12 14 16 18 0 External  $R_G$ ,  $R_{G,EXT}(\Omega)$ 

Figure 21. Clamped inductive switching energy vs.  $R_{G,EXT}$  at  $V_{DS}$  = 400V,  $I_D$  = 70A, and  $T_J$  = 25°C

Figure 22. RC snubber energy losses vs.  $R_{G,EXT}$  at  $V_{DS}$  = 400V,  $I_D$  = 70A, and  $T_J$  = 25°C



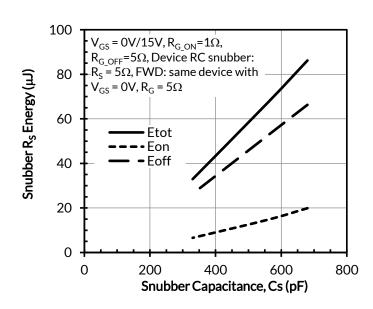


Figure 23. Clamped inductive switching energy vs. Snubber Capacitance Cs at  $V_{DS}$  = 400V,  $I_{D}$  = 70A, and  $T_{J}$  = 25°C

Figure 24. RC snubber energy loss vs. Snubber Capacitance Cs at  $V_{DS}$  = 400V,  $I_D$  = 70A, and  $T_J$  = 25°C



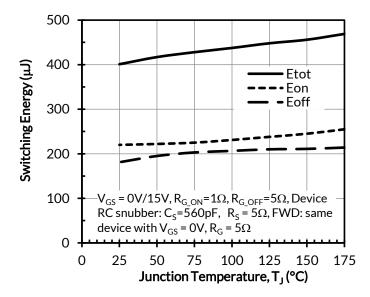












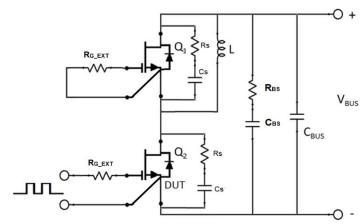


Figure 25. Clamped inductive switching energies vs. junction temperature  $T_J$  at  $V_{DS}$  = 400V, and  $I_D$  = 70A

Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ( $R_{BS}$  =  $1\Omega$ ,  $C_{BS}$ =100nF) is used to reduce the power loop high frequency oscillations.













#### **Applications Information**

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode. Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small  $R_{(G)}$ , or gate resistor, provides better EMI suppression with higher efficiency compared to using a high  $R_{(G)}$  value. There is no extra gate delay time when using the snubber circuitry, and a small  $R_{(G)}$  will better control both the turn-off  $V_{(DS)}$  peak spike and ringing duration, while a high  $R_{(G)}$  will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high  $R_{(G)}$ , while greatly reducing  $E_{(OFF)}$  from mid-to-full load range with only a small increase in  $E_{(ON)}$ . Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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