Click ***here*** *for production status of specific part numbers.*

MAX77860

USB Type-C, 3A Switch-Mode Buck Charger with Integrated CC Detection, Reverse Boost, and ADC

General Description

The MAX77860 is a high-performance single input switch mode charger that features USB Type-C CC detection capability in addition to reverse boost capability and a Safeout LDO.

This switched-mode battery charger with two integrated switches, provides small inductor and capacitor sizes, programmable battery charging current, and is ideally suited for portable devices such as smartphones, IoT devices, and other Li-ion battery powered electronics. The charger features a single input, which works for both USB and high voltage adapters. It supports USB Type-C CC detection under BC 1.2 specification, and the power-path switch is integrated in the chip. All MAX77860 blocks connected to the adapter/USB pin are protected from input overvoltage events up to 14V. The USB-OTG output provides true-load disconnect and is protected by an adjustable output current limit. It has an input current limit up to 4.0A and can charge a single-cell battery up to 3.15A. When configured in reverse-boost mode, the IC requires no additional inductors to power USB-OTG accessories. The switching charger is designed with a special CC, CV, and die temperature regulation algorithm, as well as I^2C programmable settings to accommodate a wide range of battery sizes and system loads. The on-chip ADC can help monitor the charging input voltage/current, battery voltage, charging/discharging current, and the battery temperature.

The MAX77860 communicates through an I^2C 3.0 compatible serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The IC is available in a 3.9mm x 4.0mm, 81-bump (9 x 9 array), 0.4mm pitch, wafer-level package (WLP).

Applications

- USB Type-C Charging for 1S Li-ion Applications
- Mobile Point-of-Sale Devices
- Portable Medical Equipment
- Portable Industrial Equipment

Benefits and Features

- Single-Cell Switch Mode Charger
  - Up to 14V Protection
  - 4.0V to 13.5V Input Operating Range
  - Switching Charger with D+/D- Charger Detection
  - Up to 4.0A Input Current Limit with Adaptive Input Current Limit (AICL)
  - Up to 3.15A Battery Charging Current Limit
  - Optional External Sense Resistor
  - CC, CV, and Die Temperature Control
  - Supports USB-OTG Reverse Boost, up to 1.5A Current Limit
  - Master-Slave Charging Capability, up to 6A Charge Current
  - Integrated Battery True-Disconnect FET
  - Rated up to $9A_{RMS}$, Discharge Current Limit (Programmable)
- USB Type-C Detection
  - Integrated V_{CONN} Switch
  - CC Pin
  - D+/D- Detection for USB HVDCP
  - BC 1.2 Support
- One Safeout LDO
- I^2C-Compatible Interface

Ordering Information ***appears at end of data sheet.***

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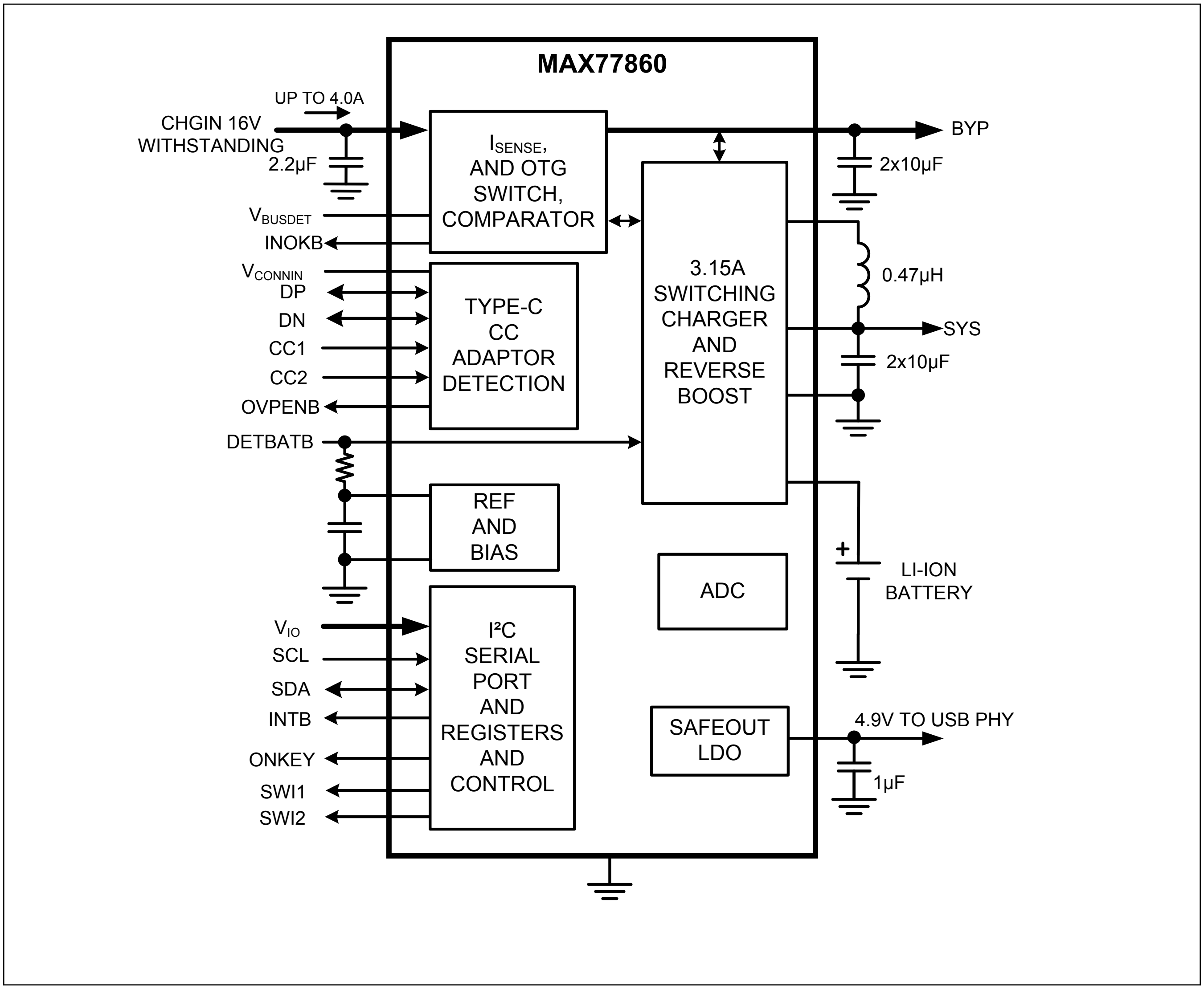
Simplified Block Diagram



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Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

81-WLP

Package Code	W813C3+1
Outline Number	21-0775
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SYS} = +3.6V, V_{CHGIN} = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, typical value for T_A is +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Shutdown Supply Current (BATT)	I_{SHDN}	All circuits off, BATT = 3.6V		25	50	µA
No Load Supply Current (BATT)	I_{NL}	USB Type-C on, all other circuits off, BATT = 3.6V		90	150	µA
SYS INPUT RANGE						
SYS Undervoltage Lockout Threshold	V_{SYS_UVLO}	V_{BATT} falling, 200mV hysteresis	2.4	2.5	2.6	V
SYS Overvoltage Lockout Threshold	V_{SYS_OVLO}	V_{BATT} rising, 200mV hysteresis	5.2	5.36	5.52	V
Low SYS Thresholds		Range programmable through LSDAC register, V_{SYS} falling, production tested at 3.60V setting		3.6		V
Low SYS Hysteresis		Range programmable through LSHYST register, production tested at 100mV setting		100		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	T_J rising		165		°C
Thermal Shutdown Hysteresis				15		°C
Thermal Interrupt 1				120		°C
Thermal Interrupt 2				140		°C
LOGIC AND CONTROL INPUTS						
SCL, SDA Input Low Level		T_A = +25°C			0.3 x V_{IO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 x V_{IO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x V_{IO}		V
SCL, SDA Logic Input Current		V_{IO} = 3.6V	-10		+10	µA
SCL, SDA Input Capacitance		(Note 1)		10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage (INTB)		I_{SINK} = 1mA			0.4	V
Output High Leakage (INTB)		V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
Interrupt Debounce Filter Timer		LOWSYS		16		ms

Electrical Characteristics (continued)

(V_{SYS} = +3.6V, V_{CHGIN} = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, typical value for T_A is +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I^{2}C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS (Note 1)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between START and STOP	t_{BUF}		0.5			µs
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 1)		50		ns
I^{2}C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 100pF) (Note 1)						
Clock Frequency	f_{SCL}	CB = 100pF			3.4	MHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 1)		10		ns
I^{2}C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (CB = 400pF) (Note 1)						
Clock Frequency	f_{SCL}	CB = 400pF			1.7	MHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns

Electrical Characteristics (continued)

(V_{SYS} = +3.6V, V_{CHGIN} = 0V, V_{IO} = 1.8V, T_A = -40°C to +85°C, typical value for T_A is +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that must be Suppressed by the Input Filter		(Note 1)		10		ns

Note 1: Design guidance only, not tested during final test.

Note 2: The CHGIN input must be less than V_{OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn on.

Note 3: The input voltage regulation loop decreases the input current to regulate the input voltage at V_{CHGIN_REG}. If the input current is decreased to $I_{CHGIN\_REG\_OFF}$ and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off.

Note 4: Production tested in charger DC-DC low-power mode (CHG_LPM bit = ‘1).

Note 5: Production tested to ¼ of the threshold with LPM bit = ‘1 (¼ FET configuration).

Electrical Characteristics—Charger

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN INPUT						
Operating Voltage			3.2		V_{OVLO}	V
CHGIN Overvoltage Threshold (Note 2)	$V_{CHGIN-OVLO}$	V_{CHGIN} Rising; CHGIN_OVP = 00	13.4	13.7	14	V
		V_{CHGIN} Rising; CHGIN_OVP = 01	9.9	10.2	10.5	
		V_{CHGIN} Rising; CHGIN_OVP = 10	7.8	8	8.3	
		V_{CHGIN} Rising; CHGIN_OVP = 11	5.65	5.85	6.05	
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\ H-OVLO}$	V_{CHGIN} Falling; CHGIN_OVP = 00		300		mV
		V_{CHGIN} Falling; CHGIN_OVP = 01		350		
		V_{CHGIN} Falling; CHGIN_OVP = 10		250		
		V_{CHGIN} Falling; CHGIN_OVP = 11		300		
CHGIN Overvoltage Delay (Note 1)	T_{D-OVLO}	V_{CHGIN} rising, 100mV overdrive, not production tested		10		μs
		V_{CHGIN} falling, 100mV overdrive, not production tested		20		

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BUSDET} to GND Minimum Turn-On Threshold Range (Note 2)	$V_{VBUSDET\_UVLO}$	$V_{VBUSDET}$ rising, 200mV hysteresis, programmable at 4.5V, 4.9V, 5.0V, and 5.1V (Note 2)	4.5		5.1	V
V_{BUSDET} to GND Minimum Turn-On Threshold Accuracy	$V_{VBUSDET\_UVLO}$	$V_{VBUSDET}$ rising, 4.5V setting	4.4	4.5	4.6	V
V_{BUSDET} to SYS Minimum Turn-On Threshold (Note 2)	$V_{VBUSDET2SYS}$	$V_{VBUSDET}$ rising, 50mV hysteresis, when valid CHGIN input is detected	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
V_{BUSDET} Turn-On Threshold Delay	$T_{D\text{-}UVLO}$	Not production tested		10		µs
CHGIN Adaptive Current Regulation Threshold Range (Note 3)	V_{CHGIN_REG}	Programmable at 4.2V, 4.6V, 4.7V, and 4.8V (Note 3)	4.2		4.8	V
CHGIN Adaptive Voltage Regulation Threshold Accuracy	V_{CHGIN_REG}	4.8V setting	4.7	4.8	4.9	V
CHGIN Current Limit Range		Programmable, 500mA default, production tested at 500mA, 1800mA, 4000mA settings only	0.1		4	A
CHGIN Supply Current	I_{IN}	V_{CHGIN} = 2.4V, the input is undervoltage and R_{INSD} is the only loading, CHGIN_PD_FST = 0 (default)		0.075		mA
		V_{CHGIN} = 5.0V, charger disabled, CHGIN_PD_FST = 0 (default)		0.17	0.5	
		V_{CHGIN} = 5.0V, charger enabled, V_{SYS} = V_{BATT} = 4.5V (no switching, battery charged), CHGIN_PD_FST = 0 (default)		2.7	4	
V_{CHGIN} Input Current Limit	$I_{INLIMIT}$	V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 500mA input current setting, T_A = +25°C	462.5	487.5	500	mA
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = +25°C	1710	1755	1800	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = 0°C to +85°C	1667	1755	1843	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = +25°C	3800	3900	4000	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = 0°C to +85°C	3705	3900	4095	

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause a 10µF input capacitor to decay from 6.0V to 4.3V, CHGIN_PD_FST = 0 (default)		100		ms
CHGIN Input Self-Discharge Resistance	R_{INSD}	CHGIN_PD_FST = 0 (default)		35		kΩ
		CHGIN_PD_FST = 1		7.3		
CHGINOK to Start Switching	T_{start}			26		ms
SWITCH IMPEDANCES AND LEAKAGE CURRENTS						
CHGIN to BYP Resistance	R_{IN2BYP}	Bidirectional		0.0144	0.04	Ω
CHGLX High-Side Resistance	R_{HS}			0.0327	0.1	Ω
CHGLX Low-Side Resistance	R_{LS}			0.0543	0.14	Ω
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$			0.0128	0.04	Ω
CHGIN to BATT Dropout Resistance	R_{IN2BAT}	Calculation estimates a 0.04Ω inductor resistance (R_L) $R_{IN2BAT} = R_{IN2BYP} + R_{HS} + R_L + R_{BAT2SYS}$		0.0999		Ω
CHGLX Leakage Current		CHGLX = CHGPG or BYP, T_A = +25°C		0.01	10	µA
		CHGLX = CHGPG or BYP, T_A = +85°C		1		
BST Leakage Current		BST = 5.5V, T_A = +25°C		0.01	10	µA
		BST = 5.5V, T_A = +85°C		1		
BYP Leakage Current		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled, T_A = +85°C		1		
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +25°C		0.01	10	µA
		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled, T_A = +85°C		1		

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Quiescent Current (I_{SYS} = 0A, I_{BYP} = 0A)	I_{MBAT}	V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is off, T_A = +25°C		20	30	µA
		V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is off, T_A = +85°C		20		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main battery overcurrent protection disabled, T_A = +25°C		15.3		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main battery overcurrent protection enabled, T_A = +25°C		20		
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main battery overcurrent protection enabled, T_A = +85°C		20		
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled, T_A = +25°C		0.01	10	
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled, T_A = +85°C		1		
	I_{MBDN}	V_{CHGIN} = 5V, V_{BATT} = 4.2V, Q_{BAT} is off, main battery overcurrent protection disabled, charger enabled (done mode), T_A = +25°C		3	10	
		V_{CHGIN} = 5V, V_{BATT} = 4.2V, Q_{BAT} is off, main battery overcurrent protection disabled, charger enabled (done mode), T_A = +85°C		3		
	I_{MBAT}	V_{CHGIN} = 0V, V_{BATT} = 4.2V, external Q_{BAT} is on, main battery overcurrent protection disabled, T_A = +85°C		15.3		
CHARGER DC-DC BUCK						
Minimum ON Time	t_{ON-MIN}			75		ns
Minimum OFF Time	t_{OFF}			75		ns

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit (Note 5)	I_{LIM}	T_A = 0°C to +85°C, IND = '0 (0.47μH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 00 (3.00A out) (Note 4)	4.15	5.05	5.95	A
		T_A = 0°C to +85°C, IND = '0 (0.47μH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 01 (2.75A out) (Note 4)		4.75		
		T_A = 0°C to +85°C, IND = '0 (0.47μH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 10 (2.50A out) (Note 4)		4.45		
		T_A = 0°C to +85°C, IND = '0 (0.47μH inductor option), production tested at I_{LIM} = 00 setting, I_{LIM} = 11 (2.25A out) (Note 4)		4.15		
		T_A = 0°C to +85°C, IND = '1 (1.0μH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 00 (3.00A out) (Note 4)		4.6		
		T_A = 0°C to +85°C, IND = '1 (1.0μH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 01 (2.75A out) (Note 4)		4.3		
		T_A = 0°C to +85°C, IND = '1 (1.0μH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 10 (2.50A out) (Note 4)		4		
		T_A = 0°C to +85°C, IND = '1 (1.0μH inductor option), production tested at I_{LIM} = 11 setting, I_{LIM} = 11 (2.25A out) (Note 4)	3	3.7	4.4	
REVERSE BOOST						
BYP Voltage Adjustment Range		2.6V/V_{BATT} < 4.5V, adjustable from 3V to 5.5V, min		3		V
		2.6V/V_{BATT} < 4.5V, adjustable from 3V to 5.5V, max		5.5		
Reverse Boost Quiescent Current	I_{BYP}	Not switching: output forced 200mV above its target regulation voltage		1150		μA
Reverse Boost Converter Maximum Output Current		3.6V < V_{BATT} < 4.5V	2			A
Reverse Boost BYP Voltage in OTG Mode	$V_{BYP.OTG}$	5.1V setting	4.94	5.1	5.26	V

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V < V_{BATT} < 4.5V, T_A = +25°C, OTG_ILIM = 00	500		550	mA
		3.4V, T_A = +25°C, OTG_ILIM = 01 (Note 1)	900		990	
		3.4V, T_A = +25°C, OTG_ILIM = 10 (Note 1)	1200		1320	
		3.4V < V_{BATT} < 4.5V, T_A = +25°C, OTG_ILIM = 11	1500		1650	
Reverse Boost Output Voltage Ripple (Note 1)		Discontinuous inductor current (i.e., skip mode)		±150		mV
		Continuous inductor current		±150		
CHARGER						
BATT Regulation Voltage Range	$V_{BATTREG}$	Programmable in 12.5mV steps (4 bits), production tested at 4.2V and 4.5V only	4.2		4.5	V
BATT Regulation Voltage Accuracy		4.2V and 4.5V settings, T_A = +25°C	-0.75		+0.75	%
		4.2V and 4.5V settings, T_A = 0°C to +85°C	-1		+1	
Fast-Charge Current Program Range		100mA to 3.15A in 50mA steps, production tested at 500mA and 3000mA settings	0.1		3.15	A
Fast-Charge Current Accuracy		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode), production tested at 500mA and 3000mA settings, T_A = +25°C	-4		+4	%
		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode), production tested at 500mA and 3000mA settings, T_A = 0°C to +85°C	-5		+5	
		Programmed currents ≥ 500mA, V_{BATT} < V_{SYSMIN} (LDO mode), production tested at 800mA	-10		+10	
Fast-Charge Currents	I_{FC}	T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3.0A	2880	3000	3120	mA
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 0.5A	480	500	520	
Low-Battery Prequalification Threshold	V_{PQLB}	V_{BATT} rising	2.8	2.9	3	V
Dead-Battery Prequalification Threshold	V_{PQDB}	V_{BATT} rising	1.9	2	2.1	V
Prequalification Threshold Hysteresis	$V_{PQ\text{-}H}$	Applies to both V_{PQLB} and V_{PQDB}		100		mV

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Battery Prequalification Charge Current Program Range	I_{PQLB_RANGE}	Default setting = enabled (50mA)	50		400	mA
Low-Battery Prequalification Charge Current	I_{PQLB}	I_PREQUAL = 00 (default)		50		mA
		I_PREQUAL= 01		100		
		I_PREQUAL = 10		200		
		I_PREQUAL = 11	300	400	500	
Dead-Battery Prequalification Charge Current	I_{PQDB}		40	55	80	mA
Charger Restart Threshold Range	V_{RSTRT}	Adjustable, 100, 150, and 200, it can also be disabled	100	150	200	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time		130		ms
Topoff Current Program Range		Programmable from 100mA to 350mA in 8 steps	100		350	mA
Topoff Current Accuracy - Gain (Note 1)		Gain			5	%
Topoff Current Accuracy - Offset (Note 1)		Offset			20	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time		30		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
Charger Soft-Start Time	t_{SS}	(Note 1)		1.5		ms
BATT TO SYS FET DRIVER						
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 10mA		30		mV
		I_{BATT} = 1A		60		
		Load regulation during the reverse regulation mode		30		mV/A
MINSYS Voltage Accuracy	V_{SYSMIN}	Programmable from 3.4V to 3.7V in 100mV steps, V_{BATT} = 2.8V, tested at 3.4V, 3.6V, and 3.7V settings	-3		+3	%
Maximum SYS Voltage	V_{SYSMAX}	The maximum system voltage: $V_{SYSMAX} = V_{BATREG} + R_{BAT2SYS} \times I_{BATT}$ V_{BATREG} = 4.2V, I_{BATT} = 3.0A		4.245	4.32	V
		The maximum system voltage: $V_{SYSMAX} = V_{BATREG} + R_{BAT2SYS} \times I_{BATT}$ V_{BATREG} = 4.7V, I_{BATT} = 3.0A		4.745	4.82	

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER						
Watchdog Timer Period	t_{WD}		80			s
Watchdog Timer Accuracy			-20	0	+20	%
CHARGE TIMER						
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes		35		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 4 hrs to 16 hrs in two hour steps including a disable setting		8		hrs
Topoff Time	t_{TO}	Adjustable from 0 min to 70 min in 10 min steps		30		min
Timer Accuracy			-20		+20	%
AVL FILTER						
Internal AVL Filter Resistance				12.5		Ω
THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{JREG}	Junction temperature when charge current is reduced, programmable from +85°C to +130°C in +5°C steps, default value is +115°C	85		130	°C
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 6.7% of the fast-charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.0A is reduced to 0A by the time the junction temperature is +20°C above the programmed loop set point. For lower programmed charge currents such as 500mA, this slope is valid for charge current reductions down to 100mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is +20°C above the programmed loop set point		-150		mA/°C
BATTERY OVERCURRENT PROTECTION						
Programmable Battery Overcurrent Threshold Alarm	I_{BOVCR}	Overcurrent from BATT to SYS sensed through internal Q_{BAT} FET Programmable range from 3A to 9A in 0.5A/step, default to 4.5A	3		9	A

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Overcurrent Debounce Time	t_{BOVRC}	This is the response time for generating the overcurrent interrupt flag	3	6	10	ms
	t_{BOVRC2}	This is the response time from overcurrent interrupt flag to Q_{BAT} turn off		12		
Battery Overcurrent Protection Quiescent Current	I_{BOVRC}			(3 + I_{BATT})/2 2000		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} rising, 100mV hysteresis	1.9	2.1	2.2	V
System Power-Up Response Time	t_{SYSPU}	Time required for circuit to activate from an unpowered state (i.e., main battery hot insertion)		1		µs
SYSTEM SELF-DISCHARGE WITH NO POWER						
BATT Self-Discharge Resistor				600		Ω
SYS Self-Discharge Resistor				600		Ω
Self-Discharge Latch Time				300		ms
DETBATB, INOKB						
DETBATB Logic Threshold	V_{IH}	4% Hysteresis		0.8 x V_{IO}		V
Logic Input Leakage Current	$I_{DETBATB}$			0.1	1	µA
Output Low Leakage (INOKB)		I_{SINK} = 1mA			0.4	V
Output High Leakage (INOKB)		V_{SYS} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V, T_A = +85°C		0.1		
THERMISTOR MONITOR (The thresholds are calculated for R25 = 10kΩ and β = 3435k)						
T1: THM Threshold, Cold, No Charge (0°C)	T_1	V_{THM}/V_{SYS} rising, 2% hysteresis (thermistor temperature falling), default OTP option	71.68	74.18	76.68	%
T1: THM Threshold, Cold, No Charge (-7°C)	T_1	V_{THM}/V_{SYS} rising, 2% hysteresis (thermistor temperature falling), OTP programmable for -7°C (Note 1)	77.51	80.01	82.51	%
THM Leakage Current		V_{THM} = V_{SYS} or 0V, T_A = +25°C	-0.2	0.01	+0.2	µA
T4: THM Threshold, Hot, No Charge (+60°C)	T_4	V_{THM}/V_{SYS} falling, 2% hysteresis (thermistor temperature rising)	20.44	22.94	25.44	%

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVPDRV INPUT FET						
OVPENB Logic Output Low Threshold	$V_{OL,OVPENB}$	I_{SINK} = 200µA, V_{OVPENB} = GND			0.4	V
OVPENB Logic Output High Threshold	$V_{OH,OVPENB}$	I_{SOURCE} = 200µA, V_{OVPENB} = V_{AVL} = V_{BATT} = 3.6V	0.7 x V_{AVL}			V
CHARGER INDICATOR (GPIO)						
Output Low Voltage		I_{SINK} = 10mA			0.4	V
Output High Leakage		V_{SYS} = 5.5V; T_A = +25°C	-1	0	+1	µA
		V_{SYS} = 5.5V; T_A = +85°C		0.1		
ONKEY						
ONKEY Input Leakage Current	ONKEY I_L	0V < V_{ONKEY} < 5.5V, T_A = +25°C	-1		+1	µA
ONKEY Rising Threshold	V_{ONKEYR}		0.3 x V_{BAT}			V
ONKEY Falling Threshold	V_{ONKEYF}				0.7 x V_{BAT}	V
ONKEY Debounce Timer	ONKEY TDEB	From ONKEY press to buck-on and Q_{BAT} switch ON		800		msecs
MASTER-SLAVE CHARGING						
SWI Output High Voltage	V_{OH}	I_{SINK} = 100µA	V_{SYS} - 0.4			V
SWI Output Low Voltage	V_{OL}	I_{SOURCE} = 100µA			0.4	V
SWI Rising Time	T_R	(Note 1)		200		ns
SWI Falling Time	T_F	(Note 1)		200		ns
SWI Input Frequency	F_{SWI}	Inferred to scan test		250		kHz
SWI Turn-On Detection Time	T_{wait_int}	Inferred to scan test		200		µs
SWI Turn-Off Detection Time	T_{off_dly}	Inferred to scan test	50		90	µs
SWI High Time	T_{sH}	Inferred to scan test	5	8	12	µs
SWI Low Time	T_{sL}	Inferred to scan test	5	8	12	µs
SWI Signal Stop Indicate Time	T_{stop}	Inferred to scan test	100			µs
SWI Interrupt Trigger Current	I_{SWI_FAULT}	T_A = +25°C			200	µA
SLAVE Input Low Level	V_{IL}	V_{SYS} = 3.6V; T_A = +25°C			0.3 x V_{SYS}	V
SLAVE Input High Level	V_{IH}	V_{SYS} = 3.6V; T_A = +25°C	0.7 x V_{SYS}			V

Electrical Characteristics—Charger (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Fast-charge current is set for 1.5A. Done current is set for 150mA. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SLAVE Input Hysteresis	V_{IHYS}	V_{SYS} = 3.6V; T_A = +25°C		0.05 x V_{SYS}		V
SLAVE Input Leakage Current	I_{SLAVE}	T_A = +25°C	-1	0	+1	µA

Electrical Characteristics—SAFEOUT LDO

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage (Default ON)		5.0V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT = 01 (default)	4.65	4.9	5.15	V
Output Voltage		SAFEOUT = 00		4.85		V
		SAFEOUT = 10		4.95		
		SAFEOUT = 11		3.3		
PSRR (Note 1)		V_{CHGIN} = 5.5, F = 100kHz, C_{OUT} = 1µF		60		dB
Maximum Output Current			60			mA
Output Current Limit				150		mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note1)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ	0.7	1		µF
Minimum Output Capacitor for Stable Operation (Note 1)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		0.7		µF
Internal Off-Discharge Resistance				1200		Ω

Electrical Characteristics—SAR ADC

(V_{CHGIN} = 5V, V_{BATT} = 3.6V, V_{SYS} = 3.6V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSP Input Leakage Current	I_{CSP}	T_A = +25°C	-1	0	+1	µA

Electrical Characteristics—SAR ADC (continued)

(V_{CHGIN} = 5V, V_{BATT} = 3.6V, V_{SYS} = 3.6V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSN Input Leakage Current	I_{CSN}	T_A = +25°C	-1	0	+1	µA
ADC Resolution	RES			8		Bits
V_{BUS} Voltage Range	V_{BUS_RANGE}	$V_{BUS\_HV\_RANGE}$ = 0	2.7		6.3	V
V_{BUS} Voltage Measurement Accuracy	V_{BUS_RES}	$V_{BUS\_HV\_RANGE}$ = 0		14		mV
V_{BUS} Voltage Range	V_{BUS_RANGE}	$V_{BUS\_HV\_RANGE}$ = 1	6.3		14.7	V
V_{BUS} Voltage Measurement Accuracy	V_{BUS_RES}	$V_{BUS\_HV\_RANGE}$ = 1		33		mV
V_{BUS} Current Range	I_{VBUS_RANGE}		0		4.1	A
V_{BUS} Current Measurement Accuracy	I_{VBUS_RES}			16		mA
V_{BATT} Voltage Range	V_{BATT_RANGE}		2.1		4.9	V
V_{BATT} Voltage Measurement Accuracy	V_{BATT_RES}			11		mV
V_{BATT} Current Range	I_{VBATT_RANGE}		0		3.1	A
V_{BATT} Current Measurement Accuracy	I_{VBATT_RES}			12		mA
I_{REXT} Current Range	I_{REXT_RANGE}		-10		+10	A
I_{REXT} Current Measurement Accuracy	I_{REXT_RES}			78		mA
Temperature Sensing Range	TEMP_RANGE	In terms of (THMB/THMV)	20		80	%
Temperature Sensing Measurement Accuracy	TEMP_RES	In terms of (THMB/THMV)		0.24		%
THMB Output Drive	V_{OH_THMB}	I_{OH_THMB} = -0.5mA	V_{SYS} - 0.1			V
THMB Precharge Time	t_{PRE_THMB}			12.7		ms
THMB Operating Range	V_{THMB}		2.8		V_{SYS}	V
THMB Input Leakage	I_{IN_THMB}	THMB = 5V	-1	0	+1	µA
THMV Input Leakage	I_{IN_THMV}		-1	0	+1	µA

Electrical Characteristics—USB Type-C

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SYS} Voltage	V_{SYS}		2.45		5.5	V
V_{BUS} Voltage	V_{BUS}			5	20	V

Electrical Characteristics—USB Type-C (continued)

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCINT} Voltage	V_{CCINT}	V_{BUS} present	3.6		5.5	V
		No V_{BUS}	2.45		5.5	
V_{REF} Voltage	V_{REF}		1.24375	1.25	1.25625	V
Oscillator Frequency	F_{OSC}		44	50	56	kHz
COMN1/COMP2 Load Resistor	R_{USB}	Load resistor on COMN1/COMP2	3	6.1	12	MΩ
IDCD Supply Voltage Range	V_{DCD}	IDCD enabled and 300kΩ load on DP	3.6		4.5	V
DP/DN Capacitance		All internal resources disconnected—idle state			2	pF
DP/DN Max Operating Voltage	$V_{DPDNMAX}$				4.5	V
OVDX Comparator Rising Threshold	V_{OVDX_THR}	Rising COMN1/COMP2 threshold with respect to VCC1	0		120	mV
OVDX Comparator Falling Threshold	V_{OVDX_THF}	Falling COMN1/COMP2 threshold with respect to VCC1	-40		+80	mV
V_{DP_SRC} Voltage	V_{DP_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DN_SRC} Voltage	V_{DN_SRC}/V_{SRC06}	Accurate over I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{D33} Voltage	V_{DP/DM_3p3} V_{SRC}/V_{SRC33}	Tested at zero load and at 200µA load	2.6		3.4	V
V_{DAT_REF} Voltage	V_{DAT_REF}		0.25	0.32	0.4	V
V_{LGC} Voltage	V_{LGC}		1.62	1.7	1.9	V
I_{DM_SINK} Current	$I_{DM\_SINK}/I_{DATSINK}$	Accurate over 0.15V to 3.6V	55	80	105	µA
I_{DP_SRC} Current	I_{DP_SRC}/I_{DCD}	Accurate over 0V to 2.5V	7	10	13	µA
R_{DM_DWN} Resistor	R_{DM_DWN}/R_{DWN15}		14.25	20	24	kΩ
I_{WEAK} Current	I_{WEAK}		0.01	0.1	0.5	µA
V_{BUS31} Threshold	V_{BUS31}	DP and DN pins, threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V	26	31	36	%
V_{BUS47} Threshold	V_{BUS47}	DP and DN pins, threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V	43.3	47	51.7	%
V_{BUS64} Threshold	V_{BUS64}	DP and DN pins, threshold in percent of V_{BUS} voltage 3V < V_{BUS} < 5.5V	57	64	71	%
Charger Detection Debounce	t_{CDDeb}		45	50	55	ms
Primary to Secondary Timer	$t_{PDSDWait}$		27	35	39	ms

Electrical Characteristics—USB Type-C (continued)

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Proprietary Charger Debounce	t_{PRDeb}		5	7.5	10	ms
Data Contact Detect Timeout	t_{DCDtmo}		700	800	900	ms
BC 1.2 State Timeout	t_{TMO}		180	200	220	ms
DP/DN Overvoltage Debounce	$t_{OVDxDeb}$		90	100	110	µs
V_{BUS} Supply Current Consumption 12V	I_{VBUS}	V_{SYS} = 0V, V_{BUS} = 12V, CC1/CC2 open, CC detection enabled, CCDRPPhase = 00b		185		µA
V_{CONN} Source Requirements		Note: Min may need to be adjusted by resistance of V_{CONN} internal switch at 1W load, for V_{CONNIN} Min > 4.9V	4.75		5.5	V
V_{CONN} Bulk Capacitance	C_{VCONN}	Must be on V_{CONN} source	10		220	µF
CC Pin Operational Voltage Range					5.5	V
CC Pin Voltage in DFP 3.0A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load, $I_{DFP3.0\_CC}$ enable, and V_{CCINT} ≥ 3.65V	3.1			V
CC Pin voltage in DFP 1.5A Mode	V_{CC_PIN}	Measured at CC pins with 126kΩ load, $I_{DFP1.5\_CC}$ enable, and V_{CCINT} ≥ 2.45V	1.85			V
CC Pin Clamp Requirements		60µA ≤ $I_{CC\_}$ ≤ 600µA		1.1	1.32	V
CC UFP Pulldown Resistance	$R_{DUFP\_CC\_}$		-10%	5.1K	+10%	Ω
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC\_}$	0.25V ≤ CC pin voltage ≤ 1.5V	-10%	80	+10%	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC\_}$	0.45V ≤ CC pin voltage ≤ 1.5V	-8%	180	+8%	µA
CC DFP 3.0A Current Source	$I_{DFP3.0\_CC\_}$	0.85V ≤ CC pin voltage ≤ 2.45V	-8%	330	+8%	µA
CC RA RD Threshold	$V_{RA\_RD0.5}$		0.15	0.2	0.25	V
CC RA RD Hysteresis	$V_{RA\_RD0.5\_H}$		0.0		0.03	V
CC UFP 0.5A RD Threshold	$V_{UFP\_RD0.5}$		0.61	0.66	0.7	V
CC UFP 0.5A RD Hysteresis	$V_{UFP\_RD0.5\_H}$		0.0		0.03	V
CC UFP 1.5A RD Threshold	$V_{UFP\_RD1.5}$		1.16	1.23	1.31	V
CC UFP 1.5A RD Hysteresis	$V_{UFP\_RD1.5\_H}$		0.0		0.03	V

Electrical Characteristics—USB Type-C (continued)

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC V_{CONN} Detect Threshold	V_{VCONN_DET}		2.10	2.25	2.4	V
CC V_{CONN} Detect Hysteresis	$V_{VCONN\_DET\_H}$			0.015		V
CC DFP V_{OPEN} Detect Threshold	V_{DFP_VOPEN}		1.50	1.575	1.65	V
CC DFP V_{OPEN} Detect Hysteresis	$V_{DFP\_VOPEN\_H}$			0.015		V
CC DFP V_{OPEN} with 3.0A Detect Threshold	$V_{DFP\_VOPEN3A}$	V_{CCINT} ≥ 3.5V	2.45	2.6	2.75	V
CC DFP V_{OPEN} with 3.0A Detect Hysteresis	$V_{DFP\_VOPEN3A\_H}$	V_{CCINT} ≥ 3.5V	0.0		0.03	V
V_{BUS} Valid	V_{BDET}	Rising	3.8	4.12	4.4	V
	V_{BDET_h}	Falling hysteresis		0.7		
V_{BUS} Discharge Value Threshold	V_{SAFE0V}	Falling voltage level where a connected UFP finds V_{BUS} removed	0.6	0.77	0.82	V
V_{BUS} Discharge Value Hysteresis	V_{SAFE0V_h}	Rising hysteresis		100		mV
CC Pin Power-Up Time	$t_{ClampSwap}$	Max time allowed from removal of voltage clamp till 5.1k resistor attached			15	ms
Type-C CC Pin Detection Debounce	$t_{CCDebounce}$		100		200	ms
Type-C Debounce	$t_{PDDebounce}$		10		20	ms
Type-C Quick Debounce	$t_{QDebounce}$		0.9	1	1.1	ms
V_{BUS} Debounce	t_{VBDeb}		9	10	11	ms
V_{SAFE0V} Debounce	$t_{VSAFE0VDeb}$		9	10	11	ms
Type-C Error Recovery Delay	$t_{ErrorRecovery}$		25			ms
Type-C DRP Toggle Time	t_{DRP}		50		100	ms
Duty Cycle of DRP Swap		Duty cycle of swap of UFP to DFP roles	30		70	%
DRP Transition Time	$t_{DRPTransition}$	Time a role swap from DFP to UFP or reverse is completed			1	ms
V_{CONN} Enable Time	$t_{VCONNON}$	Time from when V_{BUS} is supplied in DFP mode in state Attach.DFP.DRPWait			2	ms
V_{CONN} Disable Time	$t_{VCONNOFF}$	Time from UFP detached or as directed by I^2C command until V_{CONN} is removed			35	ms
CC Pin Current Change Time	$t_{SINKADJ}$	Time from CC pin changes state in UFP mode till current drawn from DFP reaches new value			60	ms

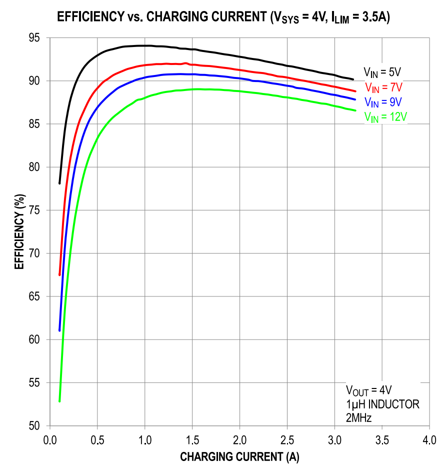
Electrical Characteristics—USB Type-C (continued)

(V_{CHGIN} = 5V, V_{BATT} = 3.8V, T_A = -40°C to +85°C unless otherwise specified, typical values are for T_A = +25°C. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BUS} On time	t_{VBUSON}	Time from UFP is attached till V_{BUS} on, for reference only			275	ms
V_{BUS} Off Time	$t_{VBUSOFF}$	Time from UFP is deteched till V_{BUS} reaches VSAFE0V, for reference only			650	ms
BVCEN Output Low Voltage		I_{SINK} = 1mA	0.4			V
BVCEN Output High Voltage		I_{SOURCE} = 1mA			V_{SYS} - 0.4	V
GENERAL						
V_{BUS} Supply Current Consumption 12V CC Detection Disabled		V_{SYS} = 0V, V_{BUS} = 12V, CC1/CC2 open, CC detection disabled, CCDRPPhase = 00b		183		µA
V_{BUS} Supply Current Consumption 5V	I_{VBUS5V}	V_{SYS} = 0V, V_{BUS} = 5V, CC1/CC2 open, CC detection enabled, CCDRPPhase = 00b		131		µA
V_{BUS} Supply Current Consumption 5V CC Detection Disabled	I_{VBUS5V_detdis}	V_{SYS} = 0V, V_{BUS} = 5V, CC1/CC2 open, CC detection disabled, CCDRPPhase = 00b		120		µA
SYS Power Supply Current	I_{CCSYS}	V_{BUS} = 0V, V_{SYS} = 4.2V, CC1/CC2 open, CC detection enabled, CCDRPPhase = 00b		45.3		µA
SYS Power Supply Current CC Detection Disabled	Icc_{sys4v2_detdis}	V_{BUS} = 0V, V_{SYS} = 4.2V, CC1/CC2 open, CC detection disabled, CCDRPPhase = 00b		7.2		µA
SYS Power Supply Current 5V	Icc_{sys5v}	V_{BUS} = 0V, V_{SYS} = 5V, CC1/CC2 open, CC detection enabled, CCDRPPhase = 00b		49		µA
SYS Power Supply Current CC Detection Disabled 5V	Icc_{sys5v_detdis}	V_{BUS} = 0V, V_{SYS} = 5V, CC1/CC2 open, CC detection disabled, CCDRPPhase = 00b		10.4		µA
SYS Power Supply Current 3V	Icc_{sys3v}	V_{BUS} = 0V, V_{SYS} = 3V, CC1/CC2 open, CC detection enabled, CCDRPPhase = 00b		40.7		µA
SYS Power Supply Current CC Detection Disabled 3V	Icc_{sys3v_detdis}	V_{BUS} = 0V, V_{SYS} = 3V, CC1/CC2 open, CC detection disabled, CCDRPPhase = 00b		4		µA
CC DETECTION						
V_{CONN} On Resistance	R_{VCONN_ON}	200mA load, V_{CONNIN} = 4.9V		0.4	0.75	Ω
CC Pin Clamp Requirements (5.5V)		$I_{CC\_}$ ≤ 2mA		5.25	5.5	V

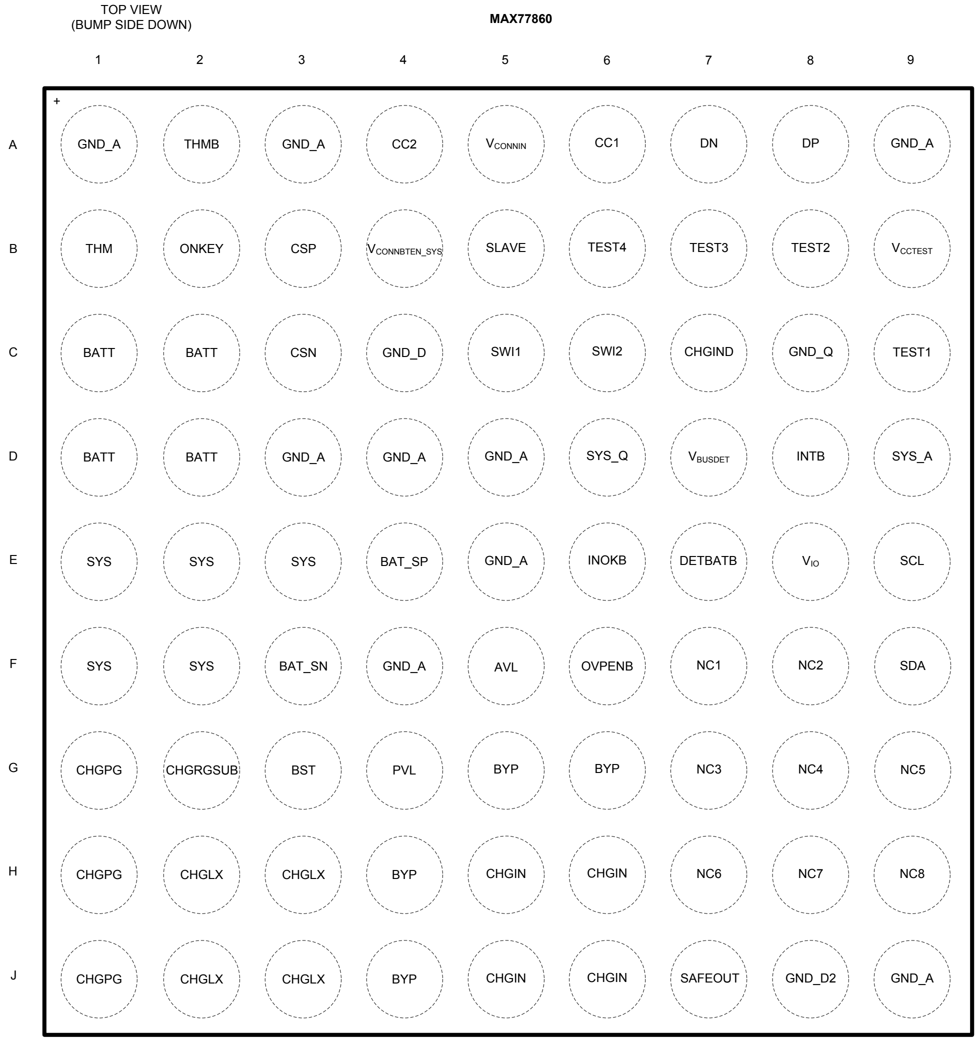
Typical Operating Characteristics

(T_A = +25 to +50°C, unless otherwise noted.)



Pin Configuration

MAX77860



	1	2	3	4	5	6	7	8	9
A	GND_A	THMB	GND_A	CC2	V_{CONNIN}	CC1	DN	DP	GND_A
B	THM	ONKEY	CSP	$V_{CONNBTEN\_SYS}$	SLAVE	TEST4	TEST3	TEST2	V_{CCTEST}
C	BATT	BATT	CSN	GND_D	SWI1	SWI2	CHGIND	GND_Q	TEST1
D	BATT	BATT	GND_A	GND_A	GND_A	SYS_Q	V_{BUSDET}	INTB	SYS_A
E	SYS	SYS	SYS	BAT_SP	GND_A	INOKB	DETBATB	V_{IO}	SCL
F	SYS	SYS	BAT_SN	GND_A	AVL	OVPENB	NC1	NC2	SDA
G	CHGPG	CHGRGSUB	BST	PVL	BYP	BYP	NC3	NC4	NC5
H	CHGPG	CHGLX	CHGLX	BYP	CHGIN	CHGIN	NC6	NC7	NC8
J	CHGPG	CHGLX	CHGLX	BYP	CHGIN	CHGIN	SAFEOUT	GND_D2	GND_A

WLP
(81 BUMP 9X9 ARRAY 0.4mm PITCH)
N/C PINS ARE UNCONNECTED AND CAN BE CONNECTED AT BOARD-LEVEL IF NEEDED.
ALL TEST PINS (TEST 1-4 AND V_{CCTEST}) SHOULD BE GROUNDED IN THE END-USE APPLICATION.
*TOP VIEW = WAFER BACK-SIDE VIEW (BUMPS NOT VIEWABLE)

Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
D6	SYS_Q	Quiet SYS Input		Power
D9	SYS_A	Analog SYS Input	2	Power
A1, A3, A9, D3, D4, D5, E5, F4, J9	GND_A	Analog Ground. Short to GND_D, GND_D2 and GND_Q.	GND	GND
C4	GND_D	Digital Ground Connection. Short to GND_D2, GND_A, and GND_Q.	1	GND
C8	GND_Q	Quiet Ground Connection. Short to GND_A, GND_Q, GND_D, and GND_D2.	1	GND
J8	GND_D2	Digital Ground Connection. Short to GND_D, GND_A, and GND_Q.		GND
E1, E2, E3, F1, F2	SYS	System Power Connection. Connect system loads to this node. Bypass with 2 x 10µF/10V ceramic capacitors from SYS to CHGPG ground plane.	5	Power
H5, H6, J5, J6	CHGIN	High Current Charger Input. Bypass to CHGPG with a 2.2µF/25V ceramic capacitor. It also serves as the reverse boost output.	CHGIN	Power
G5, G6, H4, J4	BYP	CHGIN Bypass Pin. This pin can see up to OVP limit. Output of adapter input current limit block and input to switching charger. BYP is also the boost converter output when the charger is operating in 'reverse boost' mode. Bypass with 2 x 10µF/25V ceramic capacitors from BYP to CHGPG ground plane.		
H2, H3, J2, J3	CHGLX	Charger Switching Node. Connect the inductor between CHGLX and SYS.	4	
G3	BST	High-side FET Driver Supply. Bypass BST to CHGLX with a 0.1µF/6.3V ceramic capacitor.	1	
G1, H1, J1	CHGPG	Charger Power Ground Connection	2	GND
G2	CHGRGSUB	Substrate Charger Ground Connection	1	GND
F5	AVL	Analog Voltage Level. Output of on-chip 5V LDO used to power on-chip, low-noise circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND. Powering external loads from AVL is not recommended, other than pulldown resistors.	1	
G4	PVL	Internal bias regulator high current output bypass pin. Supports internal noisy and high current gate drive loads. Bypass to PGND with a minimum 10µF/10V ceramic capacitor.	1	
C7	CHGIND	Charging Status Indication GPIO output. Open-drain, option to tie to charger as an active-low output that indicates when the charging is active.	AVL	I/O
C1, C2, D1, D2	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li-ion battery. Bypass BATT to CHGPG ground plane with a 10µF/10V ceramic capacitor.	4	
E4	BAT_SP	Battery Positive Differential Sense Connection. Connect to the positive terminal close to the battery.	BATT	
F3	BAT_SN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery.	BATT	

Pin Description (continued)

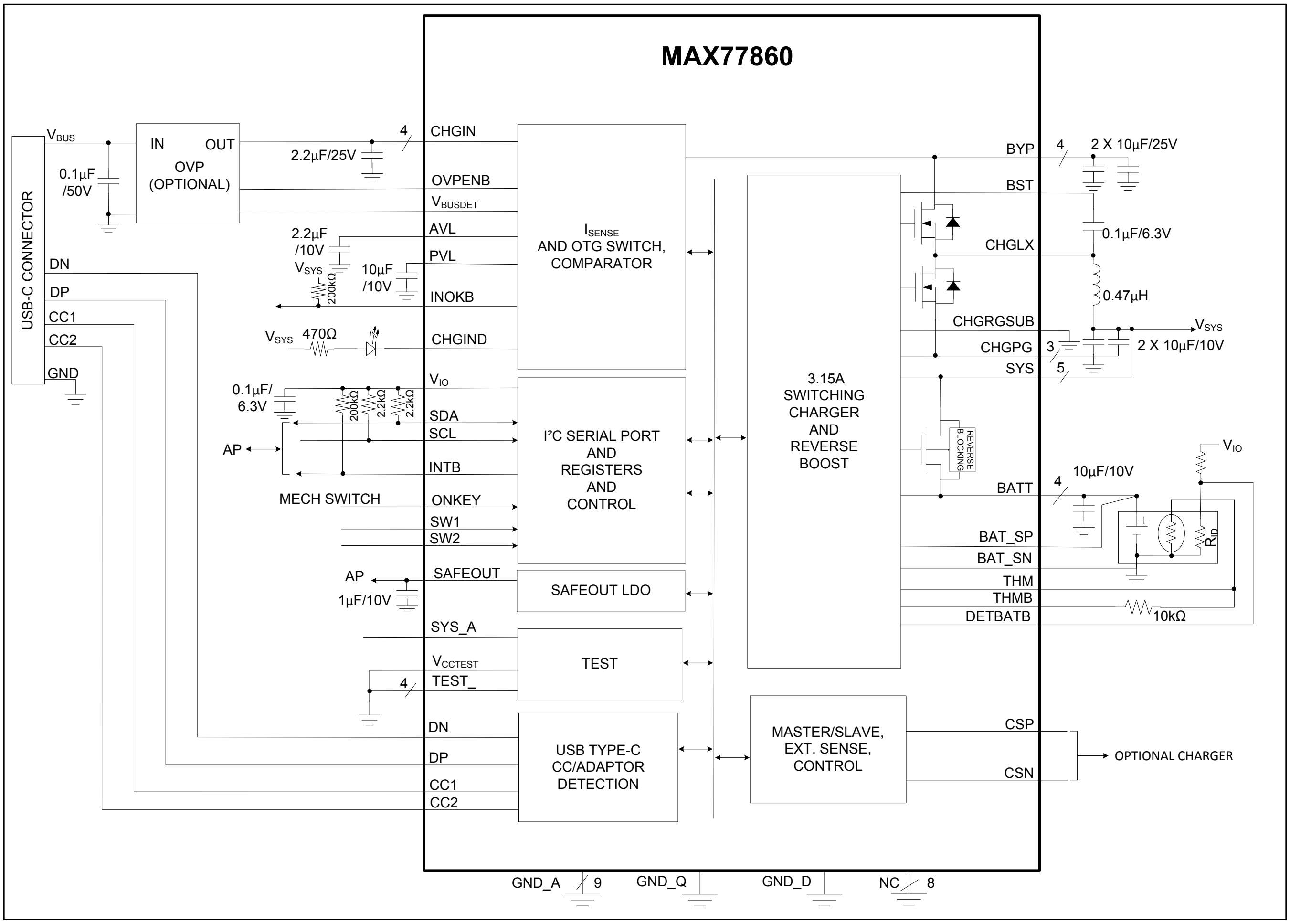
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
E6	INOKB	Charger input valid, active-low logic output flag. Open-drain output indicates when valid voltage is present at both CHGIN and SYS.	1	
E7	DETBATB	Battery Detection Active-Low Input. Connect this pin to the ID pin on the battery pack. If DETBATB is pulled below 80% of the externally applied V_{IO} voltage, this is an indication that the battery is present and the charger starts when valid CHGIN and/or WCIN power is present. If DETBATB is driven high to V_{IO} voltage or left unconnected, this is an indication that the battery is not present and the charger does not start. DETBATB is pulled high to V_{IO} pin through an off-chip pullup resistor.	1	
B2	ONKEY	ONKEY is an active-low signal with default 1000ms debounce timer. When no charging source is available at CHGIN, enable DISQIBS bit (DISIBS = 1) with I^2C to set the device in ship mode. With a healthy battery, pressing the ONKEY longer than the debounce timer re-enables the Q_{BAT} switch and the device exits ship mode.	AVL	
F6	OVPENB	Logic-low enable pin enables the external overvoltage protection IC.	1	
D7	V_{BUSDET}	Input Voltage Detection Pin. This input pin is a voltage clamped version of the input voltage and is used to trigger the device OVLO/UVLO features. Connect a 1µF ceramic capacitor between this pin and CHGPG (ground).	1	
B5	SLAVE	Input pin to indicate if slave charger is connected. Short to GND_A—no slave charger connected. Short to SYS_A—slave charger connected.		
C5	SWI1	Data Input/Output. Open-drain, 1-wire interface pin for slave 1.	1	
C6	SWI2	Data Input/Output. Open-drain, 1-wire interface pin for slave 2.		
B3	CSP	Slave-Charger Sense Current Positive Input. Option to add a 10mΩ sense resistor from CSP to CSN to have current sense information return to the master for processing. If slave charging is unused, short this pin to BATT.	1	
C3	CSN	Slave-Charger Sense Current Negative Input. Option to add a 10mΩ sense resistor from CSP to CSN to have current sense information return to the master for processing. If slave charging is unused, short this pin to BATT.		
J7	SAFEOUT	Safeout LDO Output. Default 4.9V and on when CHGIN power is valid. Bypass with a 1µF/10V ceramic capacitor to GND.	1	
E8	V_{IO}	Digital I/O Supply Input for I^2C interface	1	
F9	SDA	I^2C Serial Data	1	
E9	SCL	I^2C Serial Clock	1	
D8	INTB	Interrupt Output. Active-low, open-drain output.	1	
B1	THM	Thermistor Connection. Determine battery temperature using ratiometric measurement.	1	

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A2	THMB	Pullup voltage for THM pin pullup resistor that can be switched to save power.	1	
C9	TEST1	Test I/O Pin. Ground this pin in the application.	V_{CCTEST}	
B8	TEST2	Test I/O Pin. Ground this pin in the application.	1	
B7	TEST3	Test I/O Pin. Ground this pin in the application.	1	
B6	TEST4	Test I/O Pin. Ground this pin in the application.	1	
B9	V_{CCTEST}	Test Mux Supply. Ground this pin in the application.	1	
A7	DN	Common Negative Output 1. Connect to D- on mini/micro USB connector.	1	
A8	DP	Common Positive Output2. Connect to D+ on mini/micro USB connector.	1	
A6	CC1	Type-C CC pin 1, can be connected in parallel with USB power delivery transceiver.		
A4	CC2	Type-C CC pin 2, can be connected in parallel with USB power delivery transceiver.		
A5	V_{CONNIN}	5V power supply for supplying power to the unused CC pin if required.		
B4	$V_{CONNBTEN\_SYS}$	Output pin, used to enable external V_{CONN} boost.		
F7, F8, G7, G8, G9, H7, H8, H9	NC1–NC8	No connection. Connect to GND.		

Functional Diagrams

Functional Block Diagram



Detailed Description

Switching Charger

The MAX77860 includes a full featured switch-mode charger for a one-cell lithium ion (Li+) or lithium polymer (Li-polymer) battery. The current limit for CHGIN input is independently programmable from 0 to 4.0A in 33.3mA steps allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port. The CHGIN input current limit default is set between 100mA and 500mA (programmed default).

It also integrates a charging source detector based on signatures from USB D+/D- lines with a USB Type-C connector CC pin detector. The USB data lines are probed using a USB Battery Charging Specification revision 1.2 compliant scheme and additional proprietary charger type detection. Type-C detector supports USB Type-C DRP (dual role port) and other applications.

The synchronous switch-mode DC-DC converter can operate at either 2MHz or 4MHz switching frequency, which is ideal for portable devices due to the flexibility of using small components while eliminating excessive heat generation. The DC-DC converter can be operated in either buck or reverse-boost mode. When charging the battery, the DC-DC converter operates as a buck converter. In this mode, it operates from 3.2V to 14V input source and provides up to 3.15A charging current (programmable) to the battery. When operating in reverse-boost mode, the DC-DC converter uses energy from the main battery to boost the voltage at BYP. The boosted BYP voltage can then be used for the USB OTG function.

The IC makes the best use of the limited adapter power and the battery's power at all times to supply up to 3.15A continuous (4A peak) current from the buck to the system. Additionally, supplement mode provides additional current from the battery to the system up to $4.5A_{RMS}$, and the BATT to SYS switch has overcurrent protection (see the *Main-Battery Overcurrent Protection* section for more information). Adapter power that is not used for the system goes to charge the battery.

Maxim's proprietary process technology allows for low-$R_{DS(ON)}$ devices in a small solution size. The total dropout resistance from adapter power input to the battery is 0.15Ω (typ) assuming that the inductor has 0.04Ω of ESR. This 0.15Ω typical dropout resistance allows for charging a battery up to 3.15A from a 5V supply.

Safety features ensure reliable charging, such as charge timer, watchdog, junction thermal regulation, over/under voltage protection, short circuit protection, etc., are also implemented on the IC.

Features

- Single-Cell Switch-Mode Battery Charger
  - Adapter/USB Input
  - Up to 14V Adapter Charging (The OVLO level of the external input switch connected to CHGIN should be set lower than MAX77860 OVLO.)
  - Up to 4.0A Input Current Limit (programmable)
- Battery Charge Current (up to 3.15A)
  - CC, CV, and Die Temperature Control
  - Support for External Battery Disconnect FET
  - Support for Battery Discharge Overcurrent protection up to 6_{ARMS} (programmable)
- Reverse Boost Capability
  - Supports USB-OTG Accessories
  - Up to 5.1V/2A
  - Programmable OCP Threshold
- Support for USB Battery Charger rev 1.2 Detection
  - Data Contact Detection (DCD)
  - Detects all USB defined sources
    - Standard USB Port
    - Charging Downstream Port

    - Dedicated Charging Port
  - Adapter Type Detection
  - Manual Restart of Charger Detection
- Support USB Type-C (rev 1.1) Including:
  - USB Type-C
  - Integrated V_{CONN} Switch
  - CC Pin
    - Supports 20V Pull (through 10k min external resistor) Source Requirement
    - Dead Battery Clamp Allowing for Unpowered Upstream Facing Port (UFP) Identification
- Single Safeout LDO
- I^2C Serial Interface

USB Data Contact Detection

The USB plugs are designed so that when the plug is inserted into the receptacle, the power pins make contact before the data pins. The result is that V_{CHGIN} makes contact before the data pins make contact.

To ensure that the data pins have made contact, BC 1.2 makes it optional to detect when the data pins have made contact. To detect when the data pins have made contact, the data pins are prebiased so at least one of the data pins changes state. Therefore, when a change in data pin state is detected, the charger proceeds to identify the type of attached port.

DP and DN

The internal USB full speed/low speed transceiver is brought out to the bi-directional data pins DP and DN. These pins are ESD protected up to ±15kV. Connect these pins to a USB “B”/costume connector through external 20Ω series resistors. The IC provides an automatic switchable 1.5kΩ pullup resistor for D- (low speed) and D+ (high speed).

Adapter Detection

When an adapter is present on the V_{CHGIN}, the IC examines the device that is inserted to identify the type of adapter. The possible adapter types are:

- Dedicated charger
- Non-compliant dedicated chargers
- Charger downstream port (host or hub)
- USB 2.0 (host or hub) low power
- USB 2.0 (host or hub) high power

Each of these devices have different current capabilities as shown in Table 1.

Table 1. Supported Adapter Types

ADAPTER TYPE	OUTPUT VOLTAGE	OUTPUT CURRENT
Dedicated Charger	4.75V to 5.25V at I_{load} < 500mA 2.0V to 5.25V at I_{load} ≥ 500mA	500mA to Imax
Charger Downstream Port	4.75V to 5.25V at I_{load} < 500mA	500mA to 900mA for low-speed and full-speed
	2.0V to 5.25V at I_{load} ≥ 500mA	500mA to 1.5A for low-speed and full-speed
Apple 500mA	4.75V to 5.25V at I_{load} < 500mA	500mA maximum
Apple 1A	4.75V to 5.25V at I_{load} < 1A	1A maximum
Apple 2A	4.75V to 5.25V at I_{load} < 2A	2A maximum
Apple 12W	4.75V to 5.25V at I_{load} < 2.4A	2.4A maximum
Samsung 2A	4.75V to 5.25V at I_{load} < 2A	2A maximum
USB 2.0 Low Power	4.25V to 5.25V	100mA maximum

Table 1. Supported Adapter Types (continued)

USB 2.0 High Power	4.75V to 5.25V	500mA maximum

Charging Status Indicator

The IC has a charging status indicator to notify the user of various charging states as shown in Figure 1.

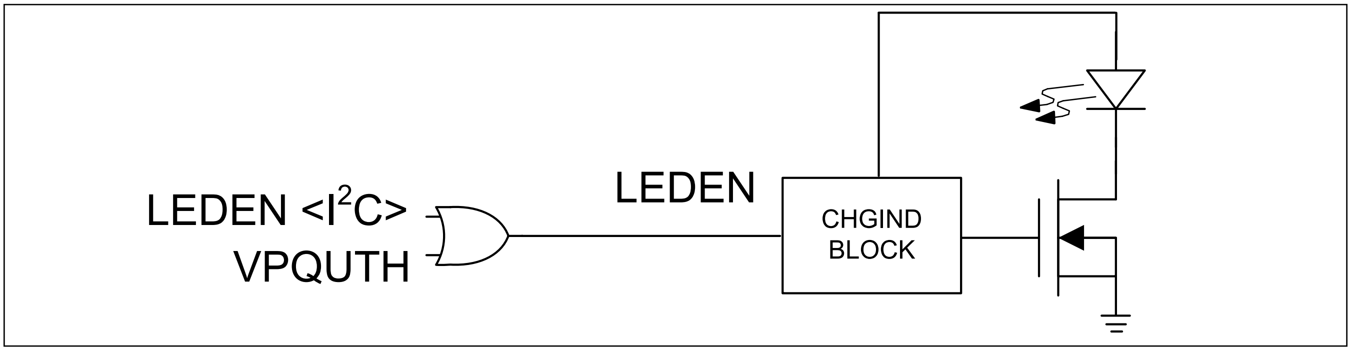


Figure 1. Charging Status Indicator

Dead Battery State

When the battery is dead and below prequal threshold, LED0 is set up to blink with 50ms ON time in 1s period. LEDEN<I^{2}C> bit is enabled by default.

Prequal Battery State

When the battery is dead and below prequal threshold, LED0 is set up to blink with 50ms ON time in 1s period. The LEDEN<I^{2}C> bit is enabled by default.

Fast-Charge Battery State

When the battery is in fast-charge state, CHGIND LED is set up to be enabled 100%. The LEDEN<I^{2}C> bit can be programmed to disable, but is enabled by default.

Fast-Charge Constant Voltage State

When the battery is in fast-charge state, CHGIND LED is set up to be enabled 100%. The LEDEN<I^{2}C> bit can be programmed to disable, but is enabled by default.

Topoff State

When the battery is in topoff-charge state, CHGIND LED is set up to blink with 50% ON time in 1s. The LEDEN<I^{2}C> bit can be programmed to disable, but is enabled by default.

Done State

When the battery is in done-charge state, CHGIND LED is set up to be disabled.

External Input OVP Driver

The driving circuit of external OVP on the input side is taken from the IC charger. The use of this feature is as follows:

- Blocking FET from input transient voltage during USB insertion/removal event.
- The polarity of the driving signal logic can be OTP programmable.

Input Current Limit

The default settings of the CHGIN_ILIM and MODE control bits are such that when a charge source is applied to CHGIN, the IC turns its DC-DC converter on in BUCK mode, limits V_{SYS} to V_{BATREG}, and limits the charge source current to 500mA. All control bits are reset on global shutdown.

Input-Voltage Regulation Loop and Adaptive Input Current Limit (AICL)

An input-voltage regulation loop ensures proper charger operation even when it is attached to power sources with poor transient load responses. The loop improves performance with relatively high resistance charge sources that exist when long cables are used or devices are charged with noncompliant USB hub configurations. Additionally, this input-voltage regulation loop improves performance with current limited adapters. If the ICs input current limit is programmed above the current limit threshold of given adapter, the input voltage loop allows the IC to regulate at the current limit of the adapter. Finally, the input-voltage regulation loop allows the IC to perform well with adapters that have poor transient load response times.

The input-voltage regulation loop automatically reduces the input current limit in order to keep the input voltage at V_{CHGIN_REG}. If the input current limit is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA, typ) and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off. The input-voltage regulation loop automatically reduces the input current limit to keep the input voltage at V_{CHGIN_REG} (programmable). If the input current limit is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA, typ) and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off.

After operating with the input-voltage regulation active, a BYP_I interrupt is generated, BYP_OK is cleared, and BYP_DTLS = 0b1xxx. To optimize input power when working with a current limited charge source, monitor the BYP_DTLS while decreasing the input current limit. When the input current limit is set below the limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage is allowed to rise. For example, optimum use of input-voltage regulation with an adapter programmed to 0.5A current limit and having a cable resistance between 300mΩ and 3Ω.

Battery Detect Input Pin (MDETBATB)

DETBATB is tied to the ID pin of the battery pack. If DETBATB is pulled below 80% of V_{IO} pin voltage, this is an indication that the main battery is present and the battery charger starts upon valid CHGIN. If DETBATB is left unconnected or equal to V_{IO} voltage, this indicates that the battery is not present and the charger does not start upon valid CHGIN, see Figure 4. DETBATB is internally pulled to BATT through an external resistor. The DETBATB status bit is valid when BATT is not present.

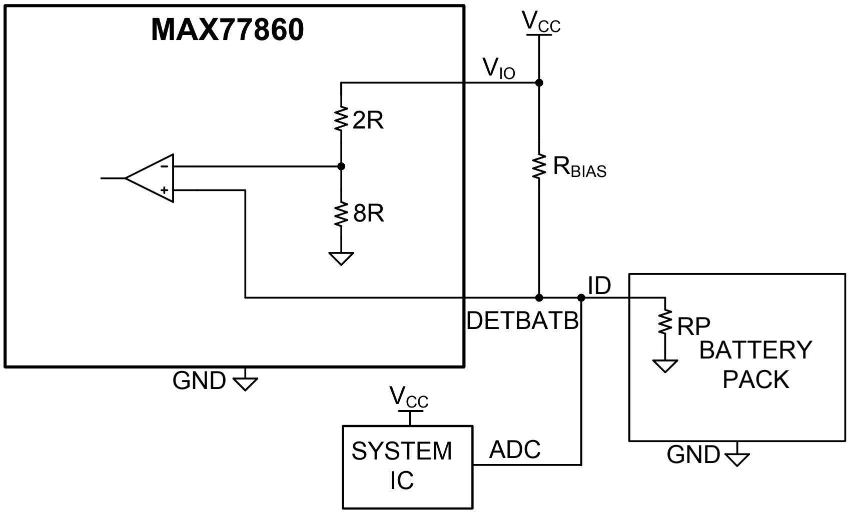


Figure 2. DETBATB Internal Circuitry and System Diagram

Charge States

The IC utilizes several charging states to safely and quickly charge batteries as shown in Figure 3. An exaggerated view of a Li+/Li-Poly battery is shown in Figure 4 when there is no system load and the die and battery are close to room temperature as it progresses through the following charge states:

1. Prequalification
2. Fast-charge
3. Topoff
4. Done

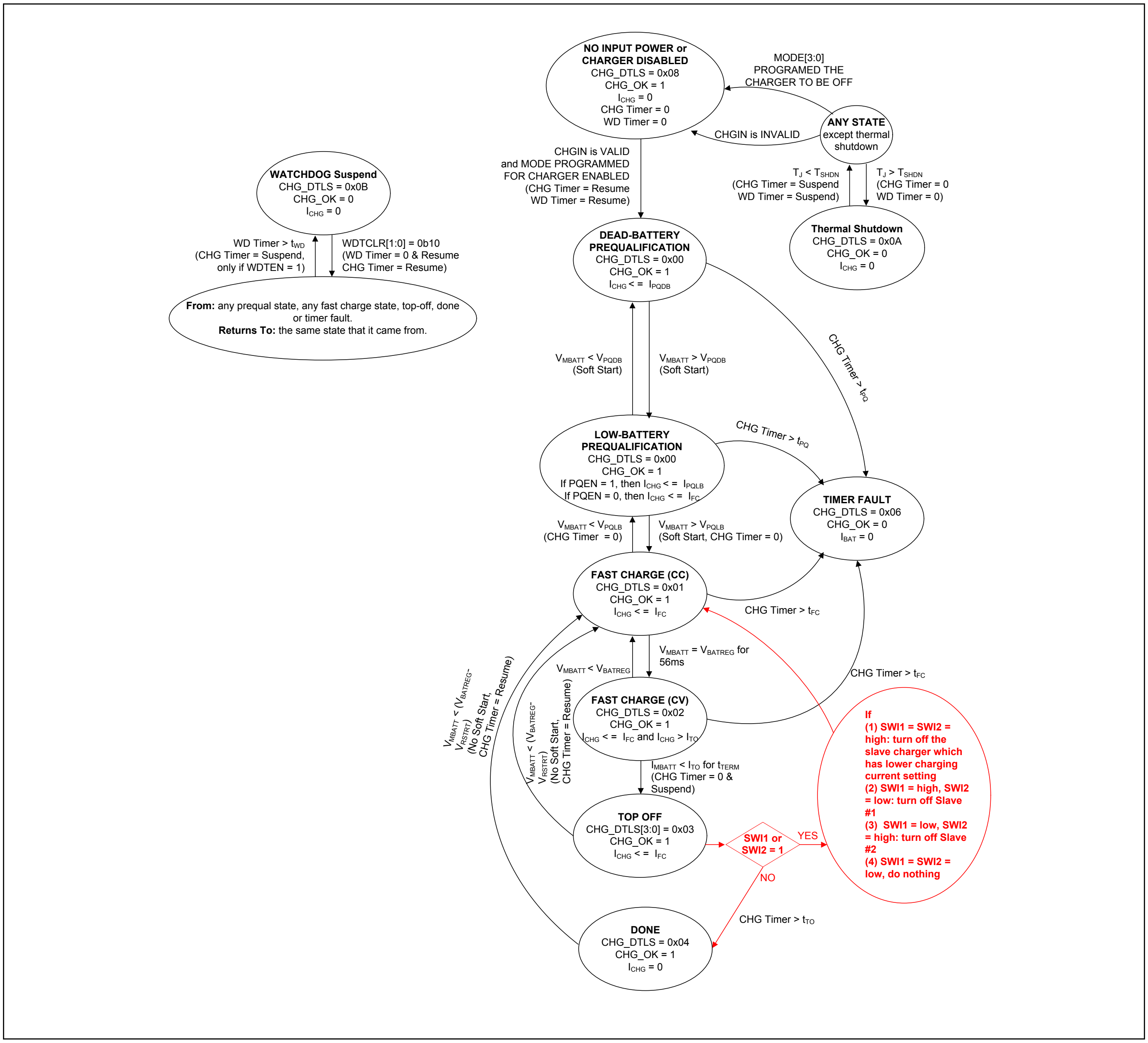
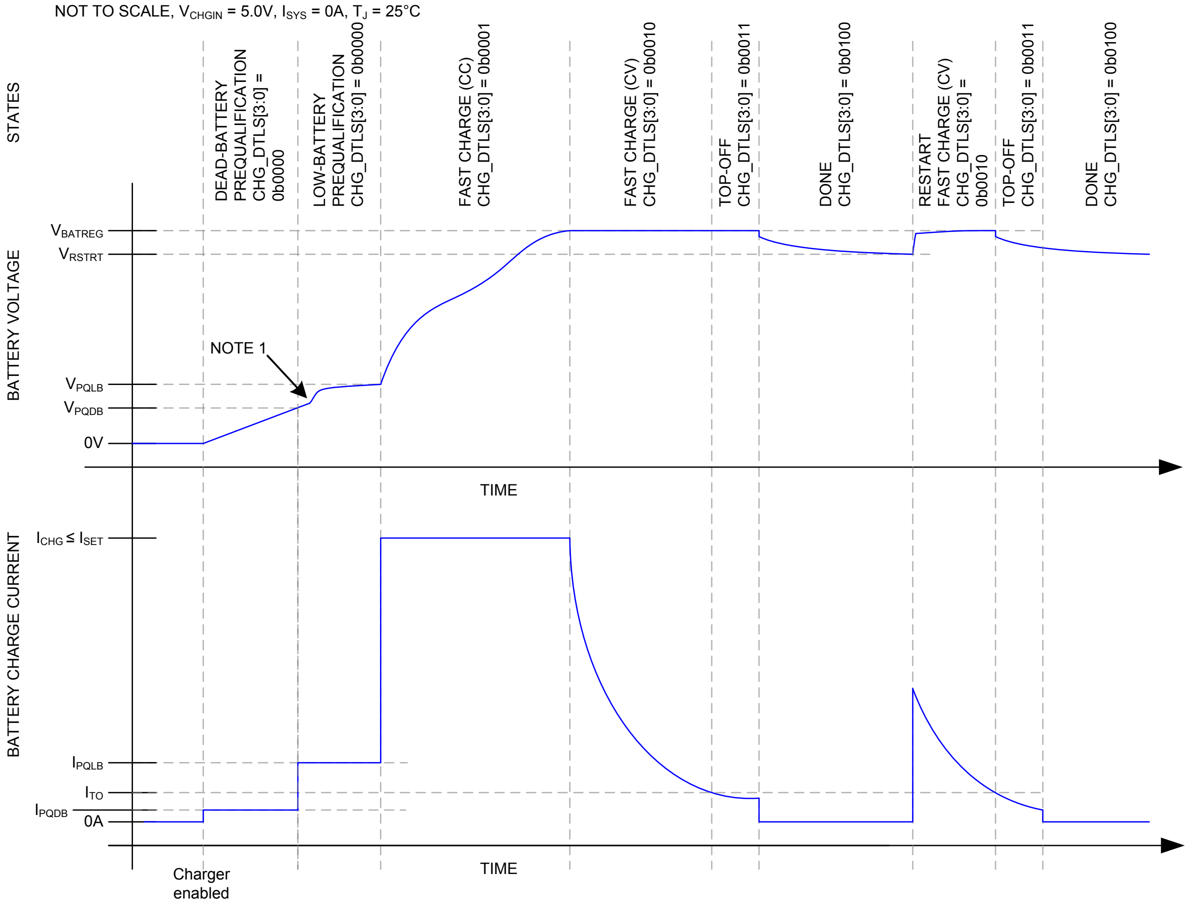


Figure 3. Charger State Diagram



NOTE 1: A typical Li+/Li-Poly has an internal battery pack protection circuit that opens the battery connection when the battery's cell voltage is lower than a dead battery threshold ($V_{DB.FALLING}$~2.5V). To get the pack protection to close again, the charger charges the battery capacitor with I_{PQDB} until the voltage exceeds V_{PQDB}. Then the charger charges the battery capacitor with I_{PQLB}. When the battery capacitor's voltage exceeds $V_{DB.RISING}$~2.6V, then the battery pack protection circuit closes which connects the cell to the charger. $V_{DB.FALLING}$ and $V_{DB.RISING}$ are not determined by the charger – they are properties of the battery.

Figure 4. Li+/Li-Poly Charge Profile

Dead-Battery Prequalification State

As shown in Figure 3, the dead-battery prequalification state occurs when the main-battery voltage is less than V_{PQDB}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS is set to 0x00. In the dead-battery prequalification state, charge current into the battery is I_{PQDB}.

The following events cause the state machine to exit this state:

- Main battery voltage rises above V_{PQDB} and the charger enters the “Low-Battery Prequalification” state.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that the dead-battery prequalification state works with battery voltages down to zero volts. The low zero volt operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically, a packs internal protection circuit opens if the battery has experienced an overcurrent, undervoltage, or overvoltage event. When a battery with an “open” internal pack protector is used with this charger, the low-battery prequalification mode current flows into the 0V battery. This current raises the pack’s terminal voltage to the point where the internal pack protection switch closes.

Note that a normal battery typically stays in the low-battery prequalification state for several minutes or less. Therefore, a battery that stays in low-battery prequalification state for longer than t_{PQ} might be experiencing a problem.

Fast-Charge Constant Current State

As shown in Figure 3, the fast-charge constant current (CC) state occurs when the main-battery voltage is greater than the low-battery prequalification threshold and less than the battery regulation threshold ($V_{PQLB} < V_{BATT} < V_{BATREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS = 0x01.

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above V_{BATREG}, the charger enters the "Fast Charge (CV)" state.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

The battery charger dissipates the most power in the fast-charge constant current state.This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced.

Topoff State

As shown in Figure 3, the topoff state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the topoff state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS = 0x03. In the topoff state, the battery charger tries to maintain V_{BATREG} across the battery and typically the charge current is less than or equal to I_{TO}.

The smart power selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.

- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the topoff time (t_{TO}), the charger enters the "Done" state.
- If $V_{BATT} < V_{BATREG} – V_{RSTRT}$, the charger goes back to the “Fast-Charge (CC)” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Done State

As shown in Figure 3, the battery charger enters its done state after the charger has been in the topoff state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is cleared, and CHG_DTLS = 0x04.

The following events cause the state machine to exit this state:

- If $V_{BATT} < V_{BATREG} – V_{RSTRT}$, the charger goes back to the “Fast-Charge (CC)” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<< 100μA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CV state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 3, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC}, which is programmable with FCHGTIME. Finally, the time that the charger is in the topoff state is t_{TO}, which is programmable with TO_TIME. Upon entering the timer fault state, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

In the timer fault state, the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and reinserted to exit the timer fault state (see the “ANY STATE” bubble in the upper right of Figure 3).

The IC provides seven (7) power states and one (1) no power state (see register description CHG_CNFG_00 [3:0]). Under power limited conditions, the power path feature maintains SYS and USB-OTG loads at the expense of battery charge current. In addition, the battery supplements the input power when required. Transitions between power states are initiated by detection/removal of valid power sources, OTG events, and undervoltage conditions. Details of the BYP and SYS voltages are provided for each state.

1. NO INPUT POWER, MODE = undefined. No input adapter or battery is detected. The charger and system is off. Battery is disconnected and charger is off.
2. BATTERY-ONLY, MODE = 0x00. Adapter input is invalid, outside the input voltage operating range (Q_{CHGIN} = off). Battery is connected to power the SYS load (Q_{BAT} = on), and boost is ready to power OTG (boost = standby), see Figure 5.

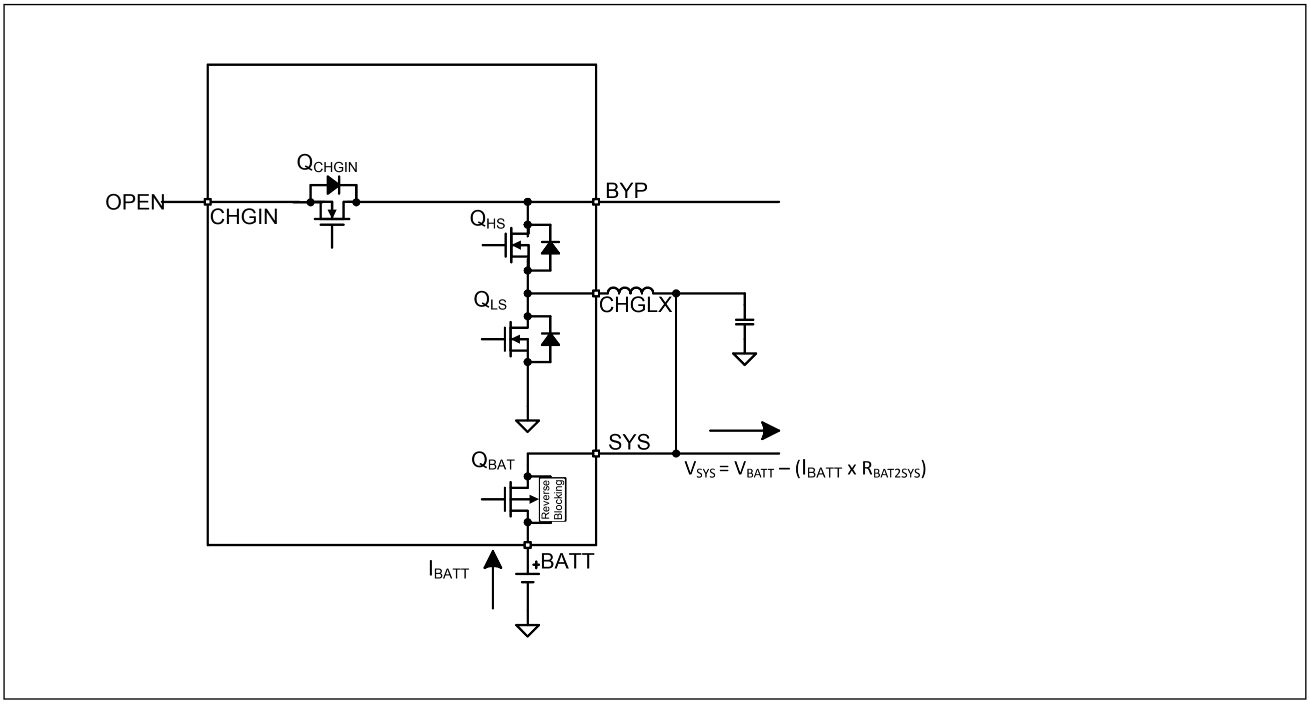


Figure 5. Battery Only

3. BATTERY-BOOST, MODE = 0x08: Adapter input is invalid outside the input voltage operating range (Q_{CHGIN} = off). Battery is connected to power the SYS load (Q_{BAT} = on) and charger is operating in boost mode (boost = on), see Figure 6.

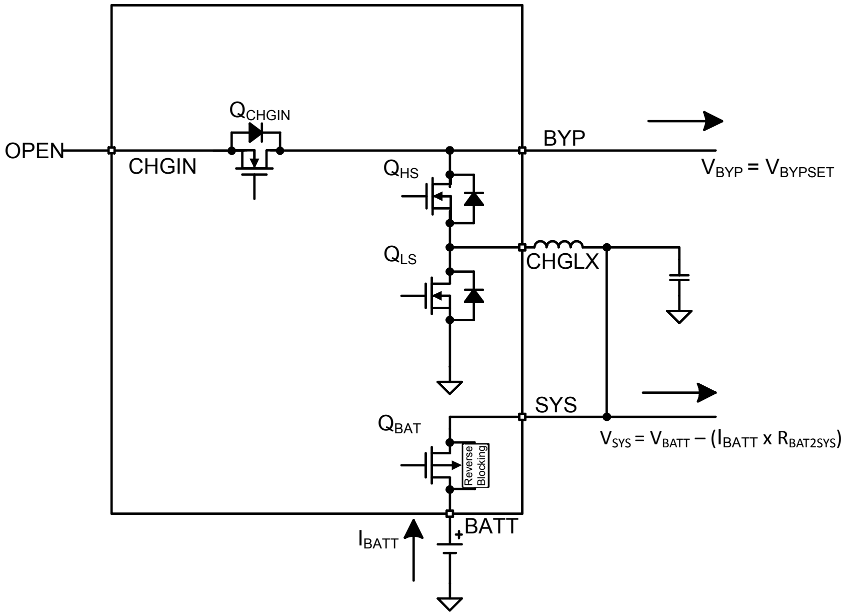


Figure 6. Battery-Boost

4. BATTERY-BOOST (OTG), MODE = 0x0A: OTG is active (Q_{CHGIN} = on). Battery is connected to support SYS and OTG loads (Q_{BAT} = on) and charger is operating in boost mode (boost = on), see Figure 7.

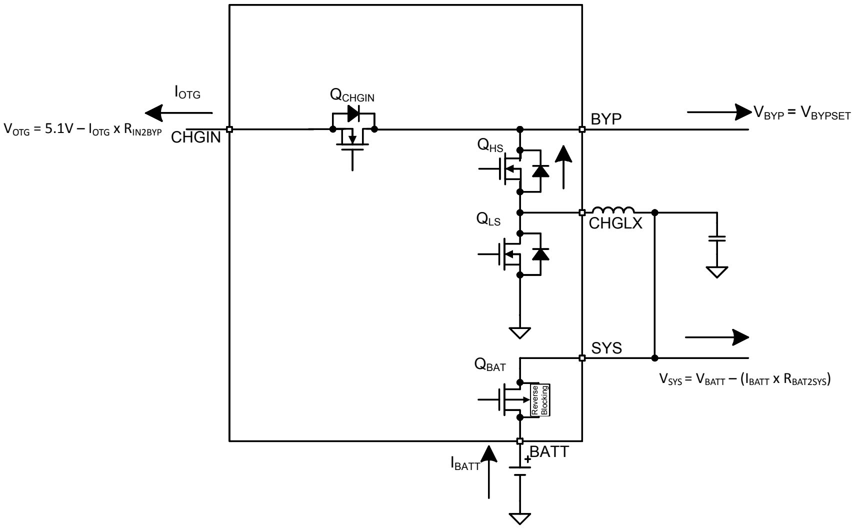


Figure 7. Battery-Boost (OTG)

5. NO CHARGE-BUCK, MODE = 0x0C: Adapter is detected within the input voltage operating range (Q_{CHGIN} = on). Battery is disconnected (Q_{BAT} = off) and charger is operating in buck mode powering SYS node, see Figure 8.

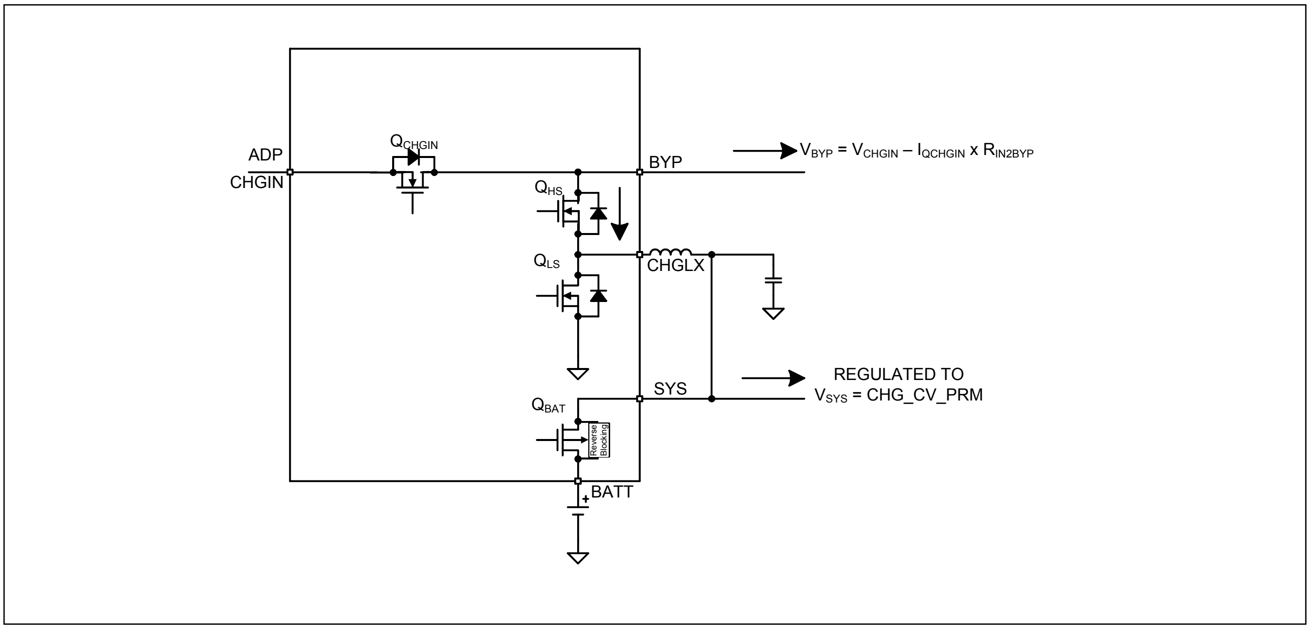


Figure 8. No Charge-Buck

6. CHARGE-BUCK, MODE = 0x0D: Adapter is detected within the input voltage operating range (Q_{CHGIN} = on). Battery is connected in charge mode (Q_{BAT} = on) and charger is operating in buck mode, see Figure 9.

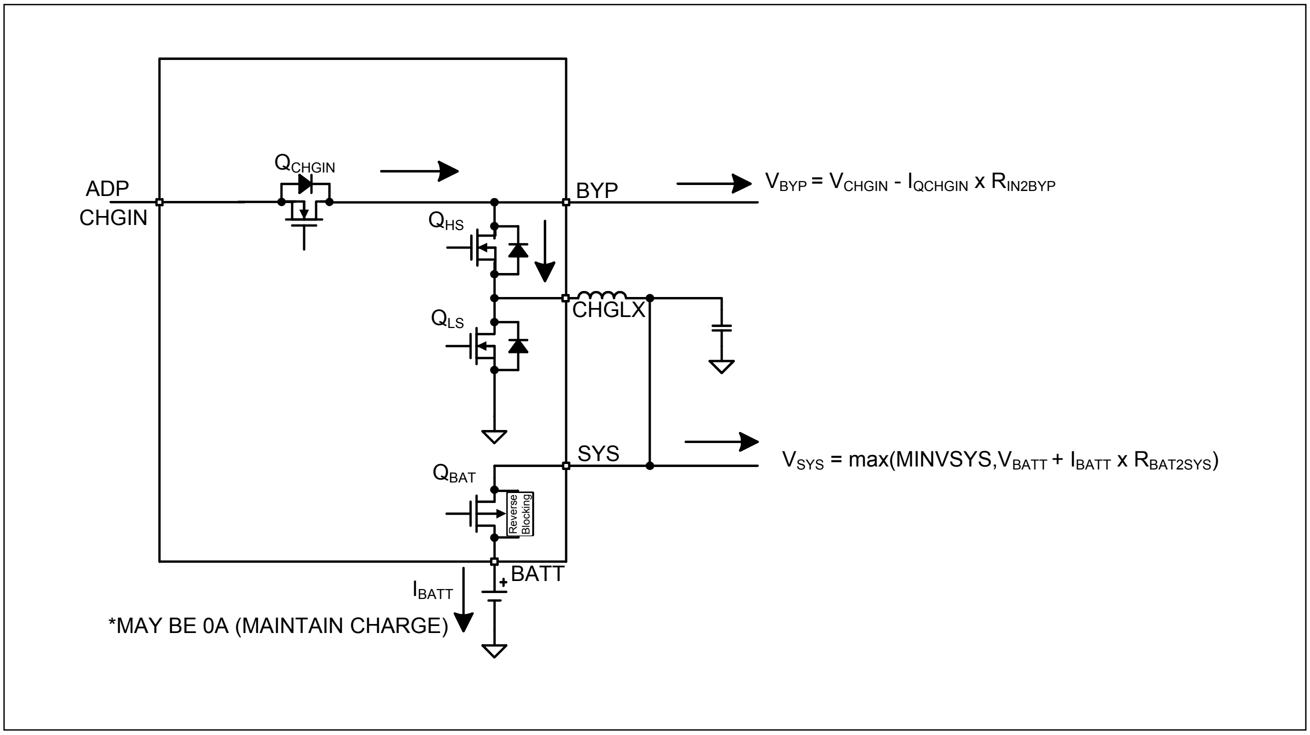


Figure 9. Charge-Buck

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 3, the watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

If the watchdog timer expires while the charger is in dead-battery prequalification, low-battery prequalification, fast charge CC or CV, topoff, done, or timer fault, the charging stops, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer has expired, the charger may be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer has expired.

Thermal Shutdown State

In the IC, the thermistor is monitored to turn off the charger during battery temperature fault events. The battery regulation voltage and current limits are not adjusted. As shown in Figure 3, the thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) is higher than the device's thermal shutdown threshold (T_{SHDN}) or below 0°C. When T_J is close to T_{SHDN}, the charger folds back the input current limit to 0A so the charger and inputs are effectively off as shown in Figure 10. Upon entering this state, CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x0A.

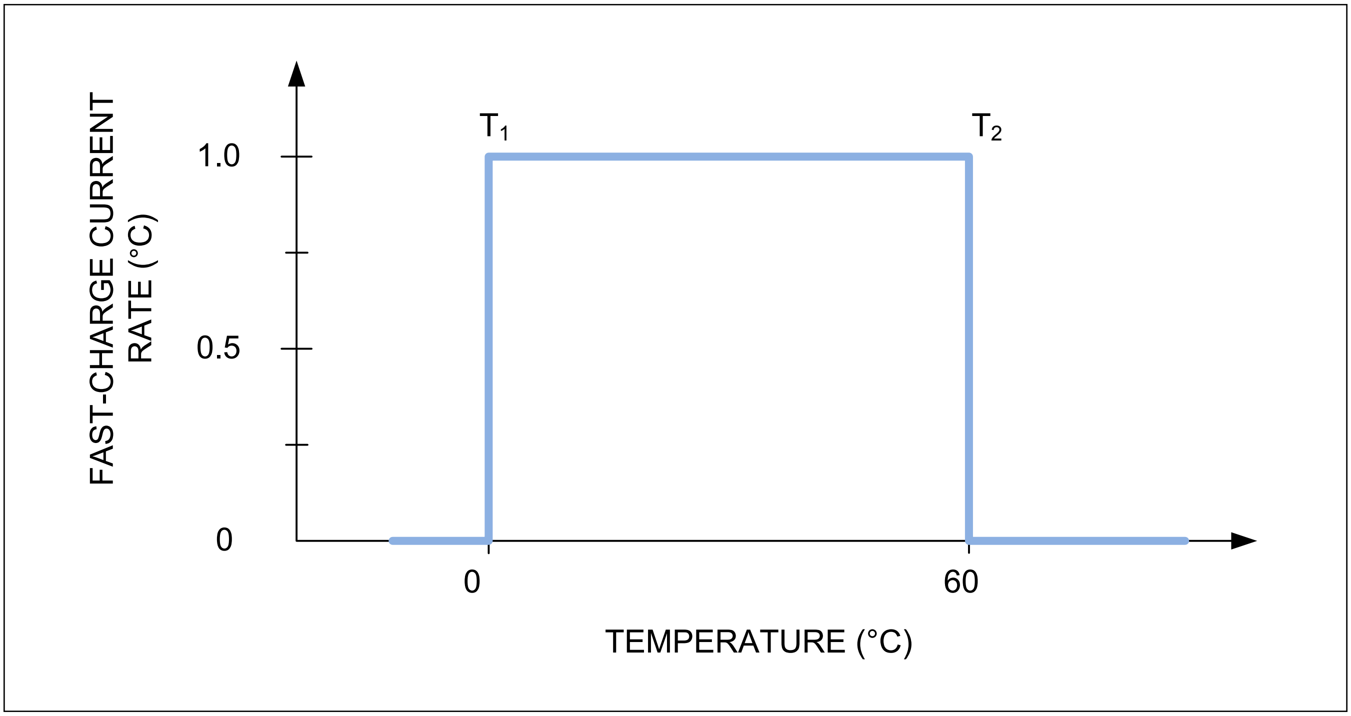


Figure 10. Thermal Shutdown Regions

In the thermal shutdown state, the charger is off and timers are suspended. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state.

Main Battery Differential Voltage Sense

As shown in Figure 11, BAT_SP and BAT_SN are differential remote sense lines for the main battery. To improve accuracy and decrease charging times, the battery charger voltage sense is based on the differential voltage between BAT_SP and BAT_SN.

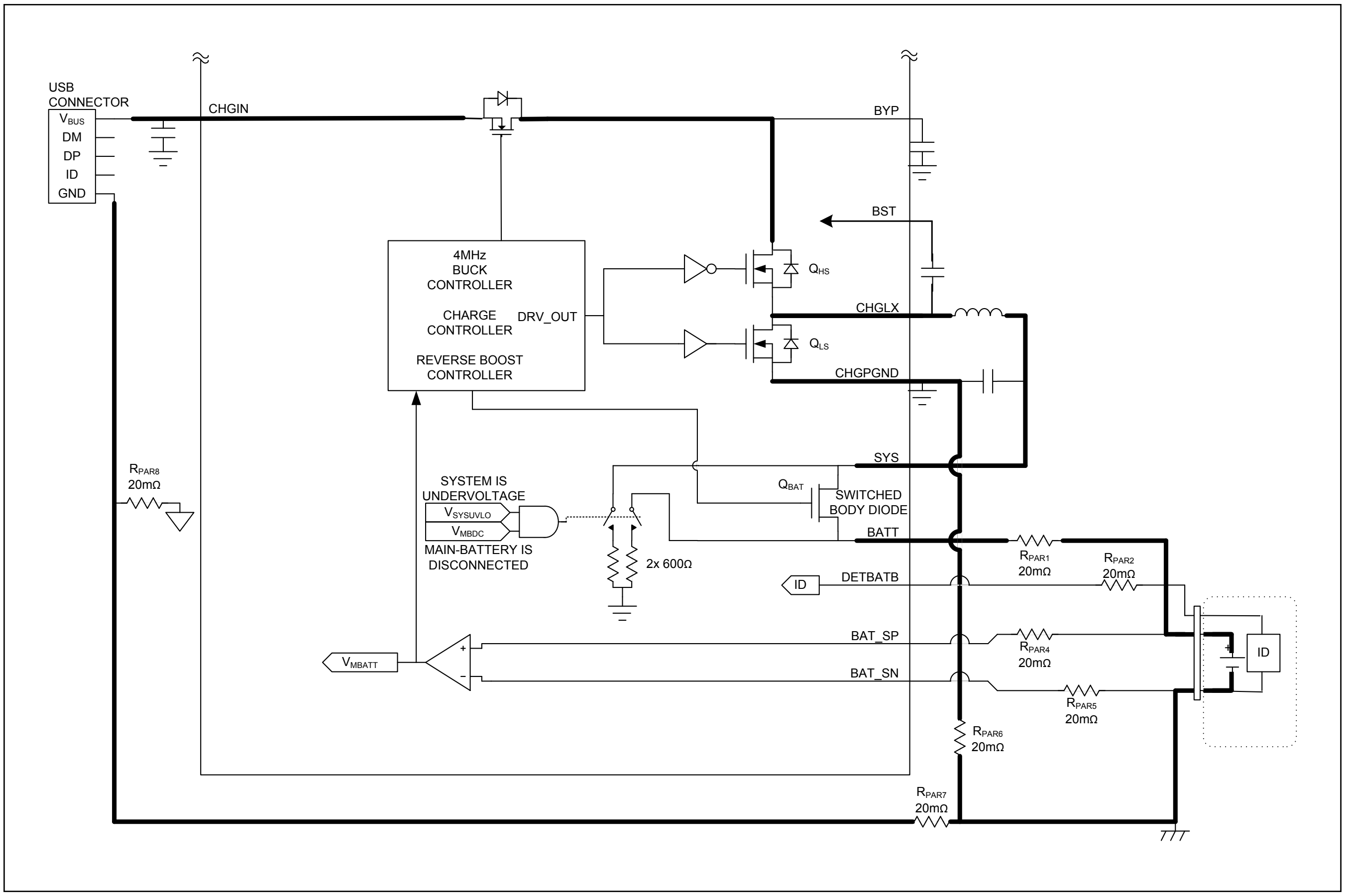


Figure 11. Schematic with Parasitic Capacitances

Figure 11 shows the high-current paths of the battery charger along with some example parasitic resistances. A Maxim battery charger without the remote sensing function would typically measure the battery voltage between BATT and GND. In the case of Figure 11, a charge current of 1A measuring from BATT to GND leads to a V_{BATT} that is 40mV higher than the real voltage because of R_{PAR1} and R_{PAR7} (I_{CHG} x (R_{PAR1} + R_{PQR7}) = 1A x 40mΩ = 40mV). Since the charger thinks the battery voltage is higher than it actually is, it enters fast-charge CV state sooner and the effective charge time may be extended by 10 minutes (based on real lab measurements). This charger with differential remote sensing does not experience this type of problem because BAT_SP and BAT_SN sense the battery voltage directly. To get the maximum benefit from these sense lines, connect them as close as possible to the main battery connector.

OTG Mode

The DC-DC converter topology of the IC allows it to operate as a forward buck converter or reverse boost converter. The modes of the DC-DC converter are controlled with MODE, and DIS_CD_CTRL (BIT7 of CHG_CNFG_00) has to be enabled. When MODE = 0x09 or 0x0A, the DC-DC converter operates in reverse boost mode allowing it to source current to CHGIN. The two modes allow current to be sourced from CHGIN and are commonly referred to as OTG modes (the term OTG is based off of the Universal Serial Bus's on-the-go concept).

When MODE = 0x09 or 0x0A, the DC-DC converter operates in reverse boost mode, regulates V_{BYP} to $V_{BYP.OTG}$ (5.1V, typ), and the switch from BYP to CHGIN is closed. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM. The four OTG_ILIM options allow for supplying 500mA or 1500mA to an external load. When the OTG mode is selected, the unipolar CHGIN transfer function measures current going out of CHGIN. When OTG mode is not selected, the unipolar CHGIN transfer function measures current going into CHGIN.

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$, then a BYP_I interrupt is generated, BYP_OK = 0, and BYP_DTLS = 0bxxx1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off. The BYP to CHGIN switches automatically retry in ~468ms. If the overload at CHGIN persists, then the switch toggles on and off with ~52ms on and ~416ms off. Hence, the OTG has an ON duty cycle ~ 11%.

In the IC, the OTG ON duty cycle can be optionally changed to ~ 1.57% with 1.67ms ON time and 104ms OFF time. This option is enabled by OTG_DC in BIT5 of CHG_CNFG_06.

Master-Slave Charging

The IC is designed to support two additional slave chargers making it capable of providing a combined charging current of 9A (3A from MAX77860 and 3A from each slave). The slave charger(s) are only enabled during the CC/CV portion, and are disabled during other modes.

The user is able to set slave charging current by accessing the SLAVE_CC register in the IC using I^2C. The IC eventually controls the slave charger using the S-Wire_I interface.

The IC protects the battery by choosing the minimum current between SLAVE_CC and charging current commanded by MAXCHARGE. To disable this protection feature, the user may set Dis_Slave_AutoUpdate to overwrite slave charging current according to SLAVE_CC.

The IC also gives two options to sense battery current for fuel gauge usage. The user may indicate their option using the slave pin.

1. Internal sense using internal FET.
    - Connect slave pin to GND.
    - This method should be used when no slave charger is required.
    - Saves cost of 1 external R_{SENSE}.
2. External sense using external RSENSE.
3. Connect the slave pin to SYS.

This method should be used when slave charger(s) are required.

S-Wire I Timing

Figure 12 shows the timing of S-Wire transfer on SWI.

1. SWI goes high to indicate the start of S-WIRE_I transmission.
2. T_{wait_int} is the enable delay for S-Wire_I commands after SWI goes high, also indicates slave to turn ON.
3. A collection of pulses is transferred as a programming command for any of the three converters.
    a) A low pulse is defined by $T_{sL.}$
    b) A high pulse is defined by $T_{sH.}$
    c) The desired programming command depends on the number of pulses.
    d) The number of pulses is determined by the number of rising edge.
4. Holding SWI high for T_{stop} to indicate the end of current programming command.
5. Multiple programming commands can be repeated at any time after T_{wait_int}.
6. Holding SWI low for T_{off_dly} to indicate the end of S-WIRE transmission, also indicates slave to turn OFF.
7. SWI1 and SWI2 transmission is purposefully staggered to avoid having both slave chargers turn ON at the same time (Figure 13).

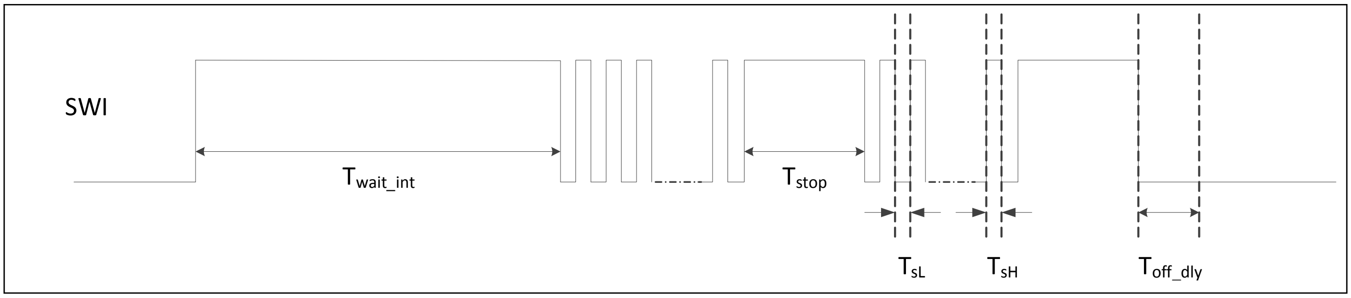


Figure 12. S-Wire Timing Diagram

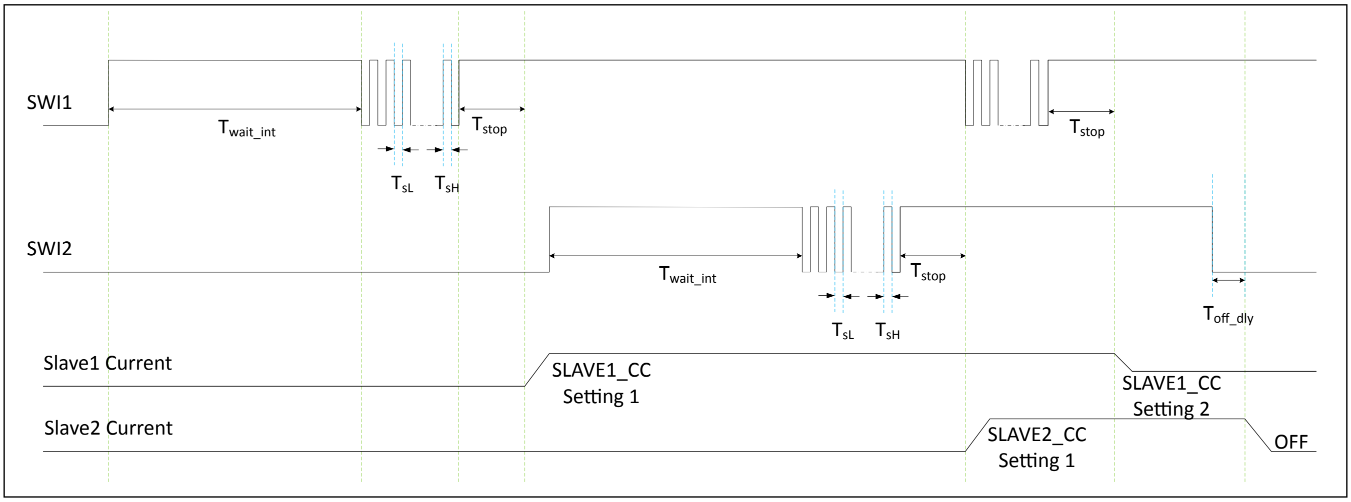


Figure 13. SW1 and SW2 Transmission

S-Wire Interrupt (Slave Fault Detection)

When a fault condition occurs at slave charger, the fault is reported to the IC and the IC interrupts the AP for slave charger fault condition. The following IC registers are for slave charger faults.

Interrupt Registers

Table 2. Top Level Interrupt

I²C SLAVE ADDRESS (WRITE)	REGISTER ADDRESS (HEX)	REGISTER NAME	RESET VALUE	BIT7	BIT6	BIT5	BIT4
0xCC	0x22	INTSRC	0x00	RSVD	SLAVE_INT	B2SOVRC_INT	FLED_INT
0xCC	0x23	INTSRCMASK	0xFF	RSVD	SLAVE_INT_MASK	B2SOVRC_INT_MASK	FLED_INT_MASK

BIT3	BIT2	BIT1	BIT0
CHGRDET_INT	FG_INT	TOP_INT	CHGR_INT
CHGRDET_INT_MASK	FG_INT_MASK	TOP_INT_MASK	CHGR_INT_MASK

Table 3. Functional Register

I²C SLAVE ADDRESS (WRITE)	REGISTER ADDRESS (HEX)	REGISTER NAME	RESET VALUE	BIT7	BIT6	BIT5	BIT4
0xD2	0x80	SWI_INT	0x00	RSVD	RSVD	RSVD	RSVD
0xD2	0x81	SWI_INT_MASK	0xFF	RSVD	RSVD	RSVD	RSVD

Table 3. Functional Register (continued)

BIT3	BIT2	BIT1	BIT0
RSVD	CV_I	SLAVE2_I	SLAVE1_I
RSVD	CV_M	SLAVE2_M	SLAVE1_M

Programming the SLAVE Charging Current

The slave charging current is programmable through the S-Wire_I interface in 64-steps of 25mA per step. Slave current should respond only after Tstop completed.

The IC has two pins, e.g., SWI1 and SWI2 to cater to two slaves. SWI1 and SWI2 commands are staggered to avoid both slaves from turning ON at the same time to avoid causing excessively high in-rush current.

ONKEY

ONKEY is an active-low signal with default 1s debounce timer ONKEYTDEB for ship mode release. When no charging source is available at CHGIN, enable DISQIBS bit (DISIBS = 1) with I^2C to set the device in ship mode. Q_{BAT} switch is disabled and SYS is isolated from BAT. With a healthy battery, pressing the ONKEY for longer than ONKEYTDEB re-enables the Q_{BAT} switch and the device exits ship mode.

When the charging source is available at CHGIN, pressing the ONKEY longer than ONKEYTD_long resets V_{SYS} rail. The IC enters buck-off and Q_{BAT} off mode for around 1s (system OFF). After that, Q_{BAT} is automatically turned on and then buck on (system ON). The details are shown in Figure 14.

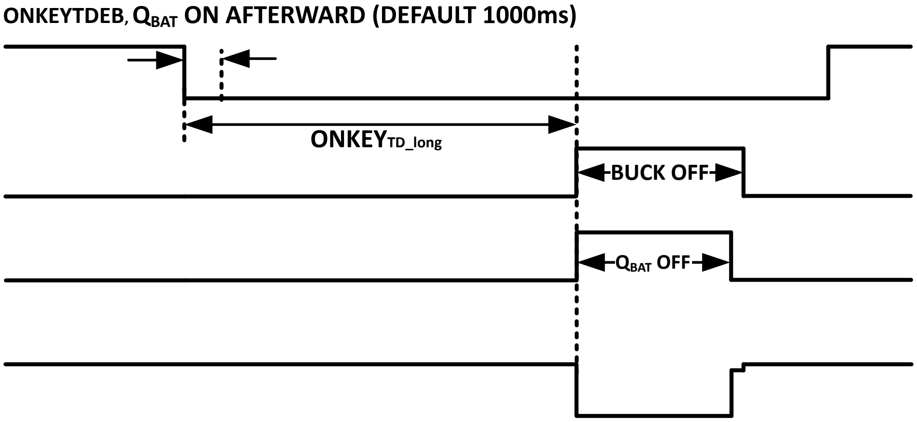


Figure 14. ONKEY Timing Diagram

Main Battery Overcurrent Protection Due to Fault

The IC protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur in a smartphone for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The main battery overcurrent protection feature is enabled with B2SOVRC. Disabling this feature reduces the main battery current consumption by I_{MBOVRC}.

When the main battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{MBOVRC}, a BAT_I interrupt is generated, BAT_OK is cleared, and BAT_DTLS reports and overcurrent condition. Typically, when the system's processor detects this overcurrent interrupt it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent, then it can disable the BATT to SYS discharge path (B2S switch) by driving DISIBS bit to a logic high.

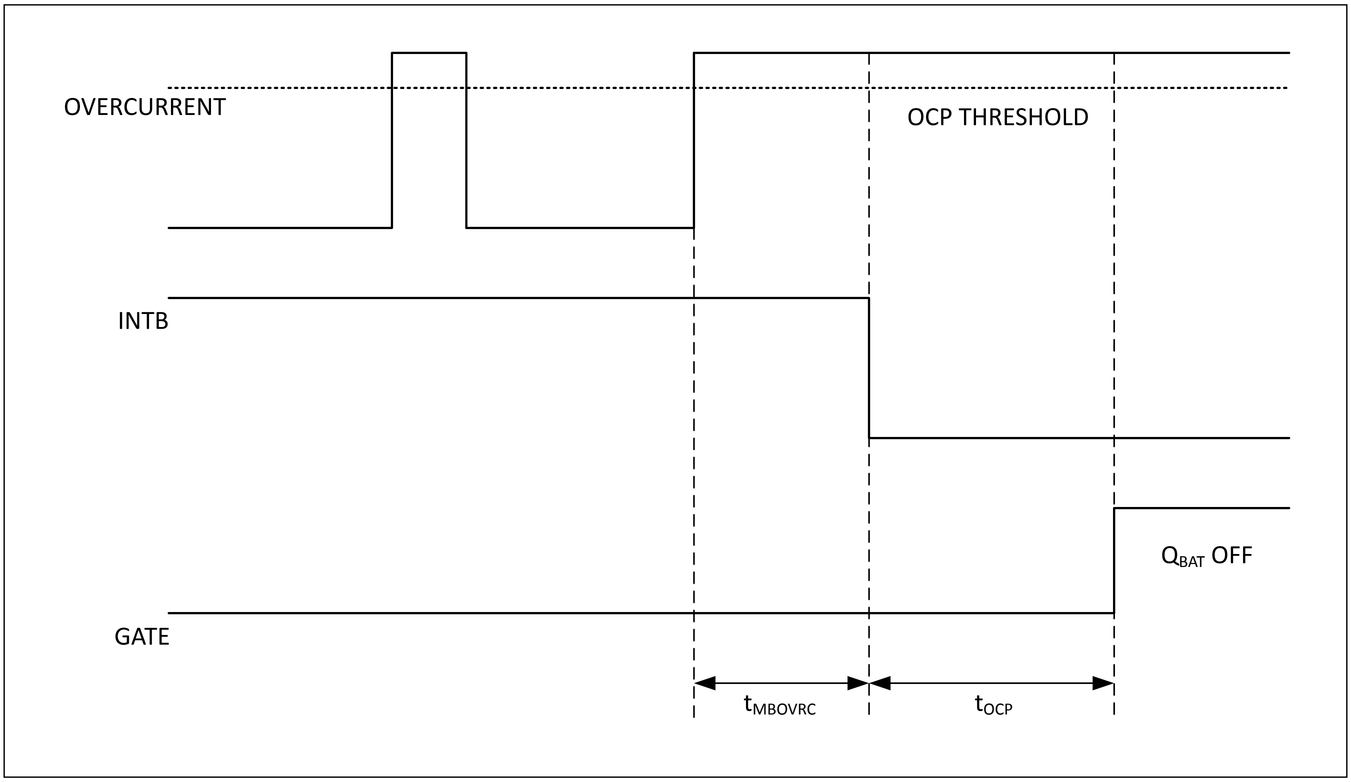


Figure 15. Overcurrent Protection Timing Diagram

There are three different scenarios of how the IC responds to setting the DISIBS bit high depending on the available power source and the state of the charger.

1) The IC is only powered from BATT and DISIBS bit is set.

1. Q_{BAT} switch opens.
2. SYS collapses and is allowed to go to 0V.
3. DISIBS holds state.
4. To exit from this state, the user has to plug in a valid input charger, then SYS is powered up and the system wakes up.

2) The IC is powered from BATT and CHGIN, the charger buck is not switching, and DISIBS bit is set.

1. Same as above.
2. To exit from this state, the user has to plug in a valid input charger, then SYS is powered up and the system wakes up.

3) The IC is powered from BATT and CHGIN, the charger buck is switching, and DISIBS bit is set.

1. DISIBIS bit is ignored.

SAFEOUT LDO

The SAFEOUT LDO is a linear regulator that provides programmable output voltages of 3.3V, 4.85V, 4.9V, and 4.95V through I^2C register. It can be used to supply low voltage rated USB systems. The SAFEOUT linear regulator turns on when CHGIN ≥ 3.2V regardless if charger is enabled or disabled. SAFEOUT is disabled when CHGIN is greater than the overvoltage threshold. The SAFEOUT LDO integrates high-voltage MOSFET to provide 20V protection at their inputs, which are internally connected to the charger input at CHGIN. SAFEOUT is default ON at 4.9V.

On-Chip ADC

Features

- In normal operating mode, ADC is used to convert voltage, current, and temperature to a digital code.
- Programmable single conversion or continuous conversion (every 1s).
- Optional averaging filter for each channel (channel 0 to 5) with fixed sampling conversion = 3.9kHz, and 2-bit selection to have 2, 4, 8, or 16 points averaging uniform for all channels.
- Optional offset compensation for channel 1 (V_{BUS} current), channel 3 (V_{BATT} current), and channel 4 (I_{REXT} current).

All settings should be programmed before ADC is enabled. Should user need to change the setting, ADC should be disabled first, change the settings and re-enabled back ADC.

Channels available for ADC conversion:

- Channel 0: V_{BUS} voltage, catered for two different voltage ranges programmable by bit $V_{BUS\_HV\_RANGE}$
  - $V_{BUS\_HV\_RANGE}$ = 0 : Range = 2.7V to 6.3V, with LSB = 14mV
  - $V_{BUS\_HV\_RANGE}$ = 1 : Range = 6.3V to 14.7V, with LSB = 33mV
- Channel 1: V_{BUS} current
  - Range = 0A to 4.1A, with LSB = 16mA
- Channel 2: V_{BATT} voltage
  - Range = 2.1V to 4.9V, with LSB = 11mV
- Channel 3: V_{BATT} current
  - Range = 0A to 3.1A, with LSB = 12mA
- Channel 4: I_{REXT} current
  - Range = -10A to +10A, with LSB = 78mA (2's complement)
- Channel 5: Temperature sensing in terms of (THMV/THMB) ratio
  - Range = 20% to 80%, with LSB = 0.24%

Single Mode and Continuous Mode

When turning on ADC, choose either of these two modes:

1. Single mode: ADC turns on only once. When finished converting the required channels, it shuts down automatically and waits for user input to turn on.
2. Continuous mode: ADC turns on every 1s to convert the required channels. After it finishes converting, analog circuits are turned off. The digital controller still requests CLK to count for 1s, then turns on the ADC again to do the next conversion.

Averaging Filter

To improve noise immunity for the ADC, the averaging filter function is added. The user is able to choose between 0, 2, 4, 8, and 16 points of averaging. Once the number of points is selected, it is applied to all the channels with filter function enabled. Averaging filters of CH0~CH7 can be enabled or disabled independently. When enabled, ADC turns on every 256μs to take measurement of the filter-enabled channel(s) until 2, 4, 8, or 16 points are done.

USB Type-C

The IC implements USB Type-C and USB BC 1.2 detection. The Type-C block implements a spec compliant DRP with V_{CONN} support allowing easy integration with an external USB PD solution. The BC 1.2 block is integrated into the Type-C state machine such that the BC 1.2 is subordinate to Type-C detection thus solving any possible interaction issues during separate block operations.

Benefits and Features

Supports full USB Battery Charging rev1.2 detection with the following features:

- Data Contact Detection (DCD)
- Detects all USB defined sources:
  - Standard USB port
  - Charging downstream port
  - Dedicated charging port

- Detects Apple power adaptors
- Samsung 2A
- New 3A DCP (requires a compatible power adapter)
- Manual restart of charger detection

Supports full USB Type-C Release1.1 with the following features:

- USB Type-C
  - Dual role port (DRP)
  - Supports standalone operation
  - Supports USB PD V_{CONN} swap
  - Supports USB PD power role swap
  - Disable mode
  - Error mode

- Integrated V_{CONN} Switch
  - 0.75Ω to either CC1 or CC2
  - External V_{CONN} source up to 5.5V
  - Bidirectional blocking

- CC Pin
  - Supports 20V pull (through 10k min ext resistor) source requirement
  - Dead battery clamp allowing for unpowered UFP identification

Register Layout Specifications

Register Map and Detailed Descriptions

The IC has a total of three slave addresses. The slave addresses for top, charger, master/slave, ADC and USB Type-C are listed below. The least significant bit is the read/write indicator (1 for read, 0 for write).

Slave Address of MAX77860:

- Clogic, SAFEOUT LDO (0xCCh/0xCDh)
- Charger, master/slave, ADC (0xD2h/0xD3h)
- USB Type-C (0x4Ah/0x4Bh)

Register Reset Conditions in R Column:

- Type S: Registers are reset each time when SYS < POR (1.55V, typ)
- Type O: Registers are reset each time when SYS < SYS UVLO (2.55V, max), or SYS > SYS OVLO, or die temp > +165°C (or IC transitions from on to off state)

Note: "RSVD" or "Reserved" means reserved: The bit is reserved for future usage.

Top Level I^{2}C Register

Table 4. PMIC Register (0x20)

NAME		FUNCTION	ADDR	TYPE	RESET
PMIC ID		PMIC ID	0x00	O	0x60
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:4	R	ID	0110	ID of MAX77860	
3:0	R	ID	0000		

Table 5. Interrupt Source (0x22)

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRC		Interrupt Source	0x22	S	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R	RSVD	0	Reserved	
6	R	SLAVE_INT	0	Slave Interrupt 0 = No slave interrupt 1 = Slave interrupt detected	
5	R	B2SOVRC_INT	0	Battery to SYS Overcurrent Interrupt 0 = No B2SOVRC interrupt 1 = B2SOVRC interrupt detected	
4	R	RSVD	1	Reserved	
3	R	USBC_INT	0	USB Type-C Interrupt 0 = No interrupt detected in USB Type-C block 1 = Interrupt detected in USB Type-C block	
2	R	RSVD	0	Reserved	
1	R	SYS_INT	0	SYS Interrupt 0 = No SYS interrupt detected 1 = SYS interrupt detected	
0	R	CHGR_INT	0	Charger Interrupt 0 = No interrupt detected in charger block 1 = Interrupt detected in charger block	

Table 6. Interrupt Source Mask (0x23)

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRCMASK		Interrupt Source Mask	0x23	S	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	RSVD	1	Reserved	
6	R/W	SLAVE_INT_MASK	1	Slave Interrupt Mask 0 = Slave interrupt is not masked 1 = Slave interrupt is masked	
5	R/W	B2SOVRC_INT_MASK	1	Battery to SYS Overcurrent Interrupt Mask 0 = B2SOVRC interrupt is not masked 1 = B2SOVRC interrupt is masked	
4	R/W	RSVD	1	Reserved	
3	R/W	USBC_INT_MASK	1	USB Type-C Interrupt Mask 0 = USB Type-C interrupt is not masked 1 = USB Type-C interrupt is masked	
2	R/W	RSVD	1	Reserved	

Table 6. Interrupt Source Mask (0x23) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
INTSRCMASK		Interrupt Source Mask	0x23	S	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
1	R/W	SYS_INT_MASK	1	SYS Interrupt Mask 0 = SYS interrupt is not masked 1 = SYS interrupt is masked	
0	R/W	CHGR_INT_MASK	1	Charger Interrupt 0 = Charger interrupt is not masked 1 = Charger interrupt is masked	

Table 7. SYSTEM Interrupt (0x24)

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTSRC		SYS Interrupt Source	0x24	S	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/C	RSVD	0	Reserved	
6	R/C	TSHDN_INT	0	Temp Shutdown Interrupt 0 = No T_{SHDN} interrupt; 1 = T_{SHDN} interrupt is detected	
5	R/C	SYSOVLO_INT	0	SYS OVLO Interrupt 0 = No SYSOVLO interrupt 1 = SYSOVLO interrupt is detected	
4	R/C	SYSUVLO_INT	0	SYS UVLO Interrupt 0 = No SYSUVLO interrupt 1 = SYSUVLO interrupt is detected	
3	R/C	LOWSYS_INT	0	LOWSYS Interrupt 0 = No LOWSYS interrupt 1 = LOWSYS interrupt is detected	
2	R/C	RSVD	0	Reserved	
1	R/C	T140C_INT	0	+140°C Interrupt 0 = No +140°C interrupt 1 = +140°C interrupt is detected; die temp > +140°C	
0	R/C	T120C_INT	0	+120°C Interrupt 0 = No +120°C interrupt 1 = +120°C interrupt is detected; die temp > +120°C	

Table 8. SYSTEM Interrupt Source Mask (0x26)

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTMASK		System Interrupt mask	0x26	S	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	RSVD	1	Reserved	
6	R/W	TSHDN_INT_MASK	1	Temp Shutdown Interrupt Mask 0 = T_{SHDN} interrupt is not masked 1 = T_{SHDN} interrupt is masked	
5	R/W	SYSOVLO_INT_MASK	1	SYS OVLO Interrupt Mask 0 = SYSOVLO interrupt is not masked 1 = SYSOVLO interrupt is masked	
4	R/W	SYSUVLO_INT_MASK	1	SYS UVLO Interrupt Mask 0 = SYSUVLO interrupt is not masked 1 = SYSUVLO interrupt is masked	

Table 8. SYSTEM Interrupt Source Mask (0x26) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
SYSINTMASK		System Interrupt mask	0x26	S	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
3	R/W	LOWSYS_INT_MASK	1	LOWSYS Interrupt Mask 0 = LOWSYS interrupt is not masked 1 = LOWSYS interrupt is masked	
2	R/W	RSVD	1	Reserved	
1	R/W	T140C_INT_MASK	1	+140°C Interrupt Mask 0 = T140C interrupt is not masked 1 = T140C interrupt is masked	
0	R/W	T120C_INT_MASK	1	120°C Interrupt Mask 0 = T120C interrupt is not masked 1 = T120C interrupt is masked	

Table 9. SAFEOUT Control Register (0xC6)

NAME		FUNCTION	ADDR	TYPE	RESET
SAFEOUTCTRL		SAFEOUT Linear regulator control	0xC6	O	0x75
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	INT_LDO_EN	0	Internal 2.5V LDO Enable Bit 0 = Disable internal 2.5V LDO 1 = Enable internal 2.5V LDO	
6	R/W	ENSAFEOUT	1	SAFEOUTLDO Enable Bit 0 = Disable SAFEOUT LDO 1 = Enable SAFEOUT LDO	
5	R/W	RSVD	1	Reserved	
4	R/W	ACTDISSAFEO	1	SAFEOUTLDO Active Discharge Enable bit 0 = No active discharge 1 = Active discharge	
3:2	R/W	RSVD	01	Reserved	
1:0	R/W	SAFEOUT[1:0]	01	SAFEOUTLDO Output Voltage Setting 00 = 4.85V; 01 = 4.90V (Default) 10 = 4.95V; 11 = 3.30V	

Charger Registers

Charger Register Details

The ICs charger has convenient default register settings and a complete charger state machine that allows it to be used with minimal software interaction. Software interaction with the register map enhances the charger by allowing a high degree of configurability. An easy-to-navigate interrupt structure and in-depth status reporting allows software to quickly track the changes in the charger's status.

Register Protection

The CHG_CNFG_01, CHG_CNFG_02, CHG_CNFG_03, CHG_CNFG_04, CHG_CNFG_05, and CHG_CNFG07 registers contain settings for static parameters that are associated with a particular system and battery. These "static" settings are typically set once each time the system's microprocessor runs its boot-up initialization code, then they are not changed again until the microprocessor reboots. CHGPROT allows for blocking the "write" access to these "static" settings to protect them from being changed unintentionally. This protection is particularly useful for critical parameters such as the battery charge current CHG_CC and the battery charge voltage CHG_CV_PRM.

Determine the following registers bit settings by considering the characteristics of the battery. Maxim recommends that CHG_CC be set to the maximum acceptable charge rate for your battery. Typically, there is no need to actively adjust the CHG_CC setting based on the capabilities of the source at CHGIN, system load, or thermal limitations of the PCB. The smart power selector intelligently manages all these parameters to optimize the power distribution:

- Charger Restart Threshold (CHG_RSTRT)
- Fast-Charge Timer (t_{FC}) (FCHGTIME)
- Fast-Charge Current (CHG_CC)
- Topoff Time (TO_TIME)
- Topoff Current (TO_ITH)
- Battery Regulation Voltage (CHG_CV_PRM)

Determine the following register bit settings by considering the characteristics of the system:

- Low-Battery Prequalification Enable (PQEN)
- Minimum System Regulation Voltage (MINVSYS)
- Junction Temperature Thermal Regulation Loop Setpoint (REGTEMP)

Interrupt, Mask, Okay, and Detail Registers

The battery charger section of the IC provides detailed interrupt generation and status for the following subblocks:

- Charger Input
- Charger State Machine
- Battery
- Bypass Node

State changes on any subblock report interrupts through the CHG_INT register. Interrupt sources are masked from affecting the hardware interrupt pin when bits in the CHG_INT_MASK register are set. The CHG_INT_OK register provides a single-bit status indication of whether the interrupt generating subblock is okay or not. The full status of interrupt generating subblock is provided in the CHG_DETAILS_00, CHG_DETAILS_01, CHG_DETAILS_02, and CHG_DETAILS_03 registers. Note that CHG_INT, CHG_INT_MASK, and CHG_INT_OK use the same bit position for each interrupt generating block to simplify software development.

Interrupt bits are automatically cleared upon reading a given interrupt register. When all pending CHG_INT interrupts are cleared, the top level interrupt bit is deasserted.

Table 10. Charger Interrupt (0xB0)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT		Charger interrupt	0xB0	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
0	R/C	BYP_I	0	Bypass Node Interrupt 0 = The BYP_OK bit has not changed since the last time this bit was read. 1 = The BYP_OK bit has changed since the last time this bit was read.	
1	R/C	BAT2SOC_I	0	BAT to SYS Overcurrent Interrupt 0 = The BAT2SOC_OK bit has not changed since the last time this bit was read. 1 = The BAT2SOC _OK bit has changed since the last time this bit was read.	
2	R/C	BATP_I	0	Battery Presence Interrupt 0 = The BATP_OK bit has not changed since the last time this bit was read. 1 = The BATP_OK bit has changed since the last time this bit was read.	

Table 10. Charger Interrupt (0xB0) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT		Charger interrupt	0xB0	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
3	R/C	BAT_I	0	Battery Interrupt 0 = The BAT_OK bit has not changed since the last time this bit was read. 1 = The BAT_OK bit has changed since the last time this bit was read.	
4	R/C	CHG_I	0	Charger Interrupt 0 = The CHG_OK bit has not changed since the last time this bit was read. 1 = The CHG_OK bit has changed since the last time this bit was read.	
5	R/C	TOPOFF_I	0	TOPOFF Interrupt 0 = The TOPOFF_OK bit has not changed since the last time this bit was read. 1 = The TOPOFF_OK bit has changed since the last time this bit was read.	
6	R/C	CHGIN_I	0	CHGIN Interrupt 0 = The CHGIN_OK bit has not changed since the last time this bit was read. 1 = The CHGIN_OK bit has changed since the last time this bit was read.	
7	R/C	AICL_CHGINI_I	0	AICL_CHGINI Interrupt 0 = The AICL_CHGINI_OK bit has not changed since the last time this bit was read. 1 = The AICL_CHGINI_OK bit has changed since the last time this bit was read.	

Table 11. Charger Interrupt Mask (0xB1)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT_MASK		Charger interrupt mask	0xB1	O	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
0	R/W	BYP_M	1	Bypass Interrupt Mask 0 = Unmasked 1 = Masked	
1	R/W	BAT2SOC_M	1	Battery to SYS Overcurrent Mask 0 = Unmasked 1 = Masked	
2	R/W	BATP_M	1	Battery Presence Interrupt Mask 0 = Unmasked 1 = Masked	
3	R/W	BAT_M	1	Battery Interrupt Mask 0 = Unmasked 1 = Masked	
4	R/W	CHG_M	1	Charger Interrupt Mask 0 = Unmasked 1 = Masked	

Table 11. Charger Interrupt Mask (0xB1) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT_MASK		Charger interrupt mask	0xB1	O	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
5	R/W	TOPOFF_M	1	TOPOFF Interrupt Mask 0 = Unmasked 1 = Masked	
6	R/W	CHGIN_M	1	CHGIN Interrupt Mask 0 = Unmasked 1 = Masked	
7	R/W	AICL_CHGINI_M	1	AICL_CHGINI Interrupt Mask 0 = Unmasked 1 = Masked	

Table 12. Charger Status (0xB2)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_INT_OK		Charger status	0xB2	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
0	R	BYP_OK	0	Single-Bit Bypass Status Indicator (See BYP_DTLS for more information.) 0 = Something powered by the bypass node has hit current limit, i.e., BYP_DTLS ≠ 0x00. 1 = The bypass node is okay, i.e., BYP_DTLS = 0x00.	
1	R	BAT2SOC_OK	0	Battery-to-SYS Overcurrent Status Indicator (See BAT2SOC_DTLS for more information.) 0 = Battery to SYS has not hit overcurrent limit. 1 = Battery to SYS has hit overcurrent limit.	
2	R	BATP_OK	0	BAT Present Status Indicator 0 = Main battery is not present. 1 = Main battery is present.	
3	R	BAT_OK	0	Single-Bit Battery Status Indicator (See BAT_DTLS for more information.) 0 = The battery has an issue or the charger has been suspended, i.e., BAT_DTLS ≠ 0x03 or 0x04. 1 = The battery is okay, i.e., BAT_DTLS = 0x03 or 0x04.	
4	R	CHG_OK	0	Single-Bit Charger Status Indicator (See CHG_DTLS for more information.) 0 = The charger has suspended charging or TREG = 1, i.e., CHG_DTLS≠0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08. 1 = The charger is okay or the charger is off, i.e., CHG_DTLS = 0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08.	
5	R	TOPOFF_OK	0	Single-Bit TOPOFF Indicator (See CHG_DTLS for more information.) 0 = The charger is not in TOPOFF state. 1 = The charger is in TOPOFF state.	
6	R	CHGIN_OK	0	Single-Bit CHGIN Input Status Indicator (See CHGIN_DTLS for more information.) 0 = The CHGIN input is invalid, i.e., CHGIN_DTLS ≠ 0x03. 1 = The CHGIN input is valid, i.e., CHGIN_DTLS = 0x03.	
7	R	AICL_CHGINI_OK	0	AICL_CHGINI_OK 0 = AICL or/and CHGINI mode. 1 = Not in AICL mode and not in CHGINI mode.	

Table 13. Charger Details 00 (0xB3)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00	Charger details 00	0xB3	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	BATP_DTLS	0	Battery Detection Details 0 = Battery presence. 1 = No battery presence.
1	R	OVPDRV_DTLS	0	OVPDRV FET Details 0 = External OVP FET off. 1 = External OVP FET on.
2	R	VBUSDET_DTLS	0	V_{BUSDET} Details 0 = V_{BUSDET} above 5.8V (100mV hysteresis). 1 = V_{BUSDET} below 5.7V.
3	R	RSVD	0	Reserved
4	R	RSVD	0	Reserved
6:5	R	CHGIN_DTLS	00	CHGIN Details: ● 0x00 = V_{BUS} is invalid. $V_{CHGIN} < V_{CHGIN_}$UVLO and input voltage regulation loop is not active. ● 0x01 = V_{BUS} is invalid. $V_{CHGIN} < V_{MBATT} + V_{CHGIN2SYS}$ and, $V_{CHGIN} > V_{CHGIN\_UVLO}$ or input voltage regulation loop is active. ● 0x02 = V_{BUS} is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$. ● 0x03 = V_{BUS} is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ or input voltage regulation loop is active, $V_{CHGIN} > V_{MBATT} + V_{CHGIN2SYS}$, $V_{CHGIN} < V_{CHGIN\_OVLO}$.
7	R	RSVD	0	Reserved

Table 14. Charger Details 01 (0xB4)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_DTLS_01</td><td>Charger details 01</td><td>0xB4</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>3:0</td><td>R</td><td>CHG_DTLS</td><td>0000</td><td colspan="2">Charger Details:
● 0x00 = Charger is in dead-battery prequalification or low-battery prequalification mode, CHG_OK = 1, $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$.
● 0x01 = Charger is in fast-charge constant current mode, CHG_OK = 1, $V_{MBATT} < V_{BATREG}$, $T_J < T_{JSHDN}$.
● 0x02 = Charger is in fast-charge constant voltage mode, CHG_OK = 1, $V_{MBATT} = V_{BATREG}$, $T_J < T_{JSHDN}$.
● 0x03 = Charger is in topoff mode, CHG_OK = 1, $V_{MBATT} \geq V_{BATREG}$, $T_J < T_{JSHDN}$.
● 0x04 = Charger is in done mode, CHG_OK = 0, $V_{MBATT} > V_{BATREG}$-V_{RSTRT}, $T_J < T_{JSHDN}$.
● 0x05 = Reserved.
● 0x06 = Charger is in timer-fault mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{MBATT} < V_{BATPQ}$, $T_J < T_{JSHDN}$.
● 0x07 = Charger is in thermistor suspend mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$. If BAT_DTLS = 0b001 then $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$.
● 0x08 = Charger is off, charger input invalid and/or charger is disabled, CHG_OK = 1.
● 0x09 = Reserved.
● 0x0A = Charger is off and $T_J > T_{JSHDN}$, CHG_OK = 0.
● 0x0B = Charger is off because the watchdog timer expired, CHG_OK = 0.
● 0x0C-0x0F = Reserved.</td></tr>
</table>

Table 14. Charger Details 01 (0xB4) (continued)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_DTLS_01</td><td>Charger details 01</td><td>0xB4</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>6:4</td><td>R</td><td>BAT_DTLS</td><td>000</td><td colspan="2">Battery Details:
● 0x00 = No battery and the charger is suspended.
● 0x01 = $V_{MBATT} < V_{PQLB}$. This condition is also reported in the CHG_DTLS as 0x00.
● 0x02 = The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery, or something else. Charging has suspended and the charger is in timer fault mode. This condition is also reported in the CHG_DTLS as 0x06.
● 0x03 = The battery is okay and its voltage is greater than the minimum system voltage ($V_{SYSMIN} < V_{MBATT}$), Q_{BAT} is on and V_{SYS} is approximately equal to V_{MBATT}.
● 0x04 = The battery is okay but its voltage is low: $V_{PQLB} < V_{MBATT} < V_{SYSMIN}$. Q_{BAT} is operating like an LDO to regulate V_{SYS} to V_{SYSMIN}.
● 0x05 = The battery voltage is greater than the battery overvoltage flag threshold (V_{BATOVF}) or it has been greater than this threshold within the last 6ms. V_{BATOVF} is set to 240mV above the V_{BATREG} target as programmed by CHG_CV_PRM. If BATOV persistS more than 56ms, charging is suspended and the DC-DC operates in buck only. Note that this flag is only generated when there is a valid input or when the DC-DC is operating as a boost.
● 0x06 = The battery is overcurrent or it has been overcurrent for at least 37.5ms since the last time this register has been read.
● 0x07 = Reserved.
In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no-battery, then overvoltage, then timer fault, then below prequel.</td></tr>
<tr><td>7</td><td>R</td><td>TREG</td><td>0</td><td colspan="2">Temperature Regulation Status
0 = The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available.
1 = The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.</td></tr>
</table>

Table 15. Charger Details 02 (0xB5)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_02	Charger details 02	0xB5	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R	BYP_DTLS	000	Bypass Node Details. All bits in this family are independent from each other. They are grouped together only because they are all related to the health of the BYP node and any change in these bits generates a BYP_I interrupt. BYP_DTLS0 = OTGILIM = 0bxx1 BYP_DTLS1 = BSTILIM = 0bx1x BYP_DTLS2 = BCKNegILIM = 0b1xx ******************************** ● 0bx00 = The bypass node is okay. ● 0bxx1 = The BYP to CHGIN switch (OTG switch) current limit was reached within the last 28ms. ● 0bx1x = The BYP reverse boost converter has hit its current limit—this condition persists for 28ms. ● 0b1xx = The BYP buck converter has hit the max negative demand current limit—this condition persists for 446µs.
3	R	AICL_DTLS	0	AICL Mode Details: 0 = Not in AICL mode; 1 = In AICL mode
4	R	CHGINI_DTLS	0	CHGINI Mode Details: 0 = Not in CHGINI mode; 1 = In CHGINI mode
7:5	R	RSVD	000	Reserved

Table 16. Charger Configuration 00 (0xB7)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00		Charger configuration 00	0xB7	O	0x05
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
3:0	R/W	MODE	0101	Power Selector Configuration ● 0x00 = 0b0000 = charger = off, OTG = off, buck = off, boost = off. The FET_DRV switch (Q_{BAT}) is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability. ● 0x01 = 0b0001 = same as 0b0000. ● 0x02 = 0b0010 = same as 0b0000. ● 0x03 = 0b0011 = same as 0b0000. ● 0x04 = 0b0100 = charger = off, OTG = off, buck = on, boost = off. When there is a valid input, the buck converter regulates the system voltage to be V_{BATREG}. ● 0x05 = 0b0101 = charger = on, OTG = off, buck = on, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. ● 0x06 = 0b0110 = same as 0b101. ● 0x07 = 0b0111 = same as 0b101. ● 0x08 = 0b1000 = charger = off, OTG = off, buck = off, boost = on. The FET_DRV switch (Q_{BAT}) is on to allow the battery to support the system and the charger's DC-DC operates as a boost converter. The BYP voltage is regulated to V_{BYPSET}. CHGIN to BYP FET is off. OVPDRV FET is off. ● 0x09 = 0b1001 = same as 0b1000. ● 0x0A = 0b1010 = charger = off, OTG = on, buck = off, boost = on. The FET_DRV switch (Q_{BAT}) is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. CHGIN to BYP FET is on allowing it to source current up to $I_{CHGIN.OTG.MAX}$. The boost target voltage is 5.1V ($V_{BYP.OTG}$) and V_{BYPSET} is ignored. ● 0x0B = reserved. ● 0x0C = 0b1100 = charger = off, OTG = off, buck = on, boost = on. When there is a valid input, the system is supported by that input: V_{SYS} = 4.2V. When the input is invalid, the boost is on with a target voltage equal to V_{BYPSET}. ● 0x0D = 0b1101 = charger = on, OTG = off, buck = on, boost = on. When there is a valid input, the system is supported by that input: V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. When input is invalid, the boost is on with a target voltage that is equal to V_{BYPSET}. ● 0x0E = 0b1110 = charger = off, OTG = on, buck = on, boost = on. V_{SYS} = 4.2V and QCHGIN is on allowing it to source current up to $I_{CHGIN.OTG.MAX}$. Boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$) and V_{BYPSET} is ignored. ● 0x0F = 0b1111 = charger = on, OTG = on, buck = on, boost = on. V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS.QCHGIN}$ is on allowing it to source current up to $I_{CHGIN.OTG.MAX}$. Boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$) and the V_{BYPSET} is ignored.	

Table 16. Charger Configuration 00 (0xB7) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00		Charger configuration 00	0xB7	O	0x05
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
4	R/W	WDTEN	0	Watchdog Timer Enable Bit. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. 0 = Watchdog timer disabled. 1 = Watchdog timer enabled.	
5	R/W	SPREAD	0	Spread Spectrum Feature 0 = Disabled 1 = Enabled **Note:** Feature is operational both for 9V and 12V CHGIN input voltage. Feature is not guaranteed to be operational for 5V CHGIN input voltage. When feature is not operational, it can be kept enabled without side effects.	
6	R/W	DISIBS	0	MBATT to SYS FET Disable Control 0 = MBATT to SYS FET is controlled by the power path state machine. 1 = MBATT to SYS FET is forced off.	
7	R/W	DIS_USBC_CTRL	0	Disable USB Type-C Control Over Charger 0 = Enabled 1 = Disabled	

Table 17. Charger Configuration 01 (0xB8)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_01		Charger configuration 01	0xB8	O R/W (protected with CHGPROT)	0xD8
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
2:0	R/W	FCHGTIME	000	Fast-Charge Timer Duration (t_{FC}) 0x00 = Disable; 0x01 = 4 hrs; 0x02 = 6 hrs; 0x03 = 8 hrs; 0x04 = 10 hrs; 0x05 = 12 hrs; 0x06 = 14 hrs; 0x07 = 16 hrs	
3	R/W	FSW	1	Switching Frequency Option 0 : 4MHz; 1 : 2MHz	
5:4	R/W	CHG_RSTRT	01	Charger Restart Threshold 0x00 = 100mV below the value programmed by CHG_CV_PRM. 0x01 = 150mV below the value programmed by CHG_CV_PRM. 0x02 = 200mV below the value programmed by CHG_CV_PRM. 0x03 = Disabled	
6	R/W	LSEL	1	Inductor Selection 0 : 0.47µH (for 4MHz option only) 1 : 1µH (for 2MHz and 4MHz options)	
7	R/W	PQEN	1	Low-Battery Prequalification Mode Enable 0 = Low-battery prequalification mode is disabled. 1 = Low-battery prequalification mode is enabled.	

Table 18. Charger Configuration 02 (0xB9)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_02</td><td>Charger configuration 02</td><td>0xB9</td><td>O
R/W (protected with CHGPROT)</td><td>0x09</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>5:0</td><td>R/W</td><td>CHG_CC</td><td>001001
(450mA)</td><td colspan="2">Fast Charge Current Selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.10A (0x00) to 3.0A (0x3C) in 50mA step.
Note: The first three codes are all 100mA.
<table>
<tr><th>Bits</th><th>(mA)</th><th>Bits</th><th>(mA)</th><th>Bits</th><th>(mA)</th><th>Bits</th><th>(mA)</th></tr>
<tr><td>0x00</td><td>100</td><td>0x10</td><td>800</td><td>0x20</td><td>1600</td><td>0x30</td><td>2400</td></tr>
<tr><td>0x01</td><td>100</td><td>0x11</td><td>850</td><td>0x21</td><td>1650</td><td>0x31</td><td>2450</td></tr>
<tr><td>0x02</td><td>100</td><td>0x12</td><td>900</td><td>0x22</td><td>1700</td><td>0x32</td><td>2500</td></tr>
<tr><td>0x03</td><td>150</td><td>0x13</td><td>950</td><td>0x23</td><td>1750</td><td>0x33</td><td>2550</td></tr>
<tr><td>0x04</td><td>200</td><td>0x14</td><td>1000</td><td>0x24</td><td>1800</td><td>0x34</td><td>2600</td></tr>
<tr><td>0x05</td><td>250</td><td>0x15</td><td>1050</td><td>0x25</td><td>1850</td><td>0x35</td><td>2650</td></tr>
<tr><td>0x06</td><td>300</td><td>0x16</td><td>1100</td><td>0x26</td><td>1900</td><td>0x36</td><td>2700</td></tr>
<tr><td>0x07</td><td>350</td><td>0x17</td><td>1150</td><td>0x27</td><td>1950</td><td>0x37</td><td>2750</td></tr>
<tr><td>0x08</td><td>400</td><td>0x18</td><td>1200</td><td>0x28</td><td>2000</td><td>0x38</td><td>2800</td></tr>
<tr><td>0x09</td><td>450</td><td>0x19</td><td>1250</td><td>0x29</td><td>2050</td><td>0x39</td><td>2850</td></tr>
<tr><td>0x0A</td><td>500</td><td>0x1A</td><td>1300</td><td>0x2A</td><td>2100</td><td>0x3A</td><td>2900</td></tr>
<tr><td>0x0B</td><td>550</td><td>0x1B</td><td>1350</td><td>0x2B</td><td>2150</td><td>0x3B</td><td>2950</td></tr>
<tr><td>0x0C</td><td>600</td><td>0x1C</td><td>1400</td><td>0x2C</td><td>2200</td><td>0x3C</td><td>3000</td></tr>
<tr><td>0x0D</td><td>650</td><td>0x1D</td><td>1450</td><td>0x2D</td><td>2250</td><td>0x3D</td><td>3050</td></tr>
<tr><td>0x0E</td><td>700</td><td>0x1E</td><td>1500</td><td>0x2E</td><td>2300</td><td>0x3E</td><td>3100</td></tr>
<tr><td>0x0F</td><td>750</td><td>0x1F</td><td>1550</td><td>0x2F</td><td>2350</td><td>0x3F</td><td>3150</td></tr>
</table>
Note: The thermal foldback loop can reduce the battery charger’s target current by ATJREG.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>OTG_ILIM</td><td>00</td><td colspan="2">CHGIN Output Current Limit in OTG Mode ($I_{CHGIN.OTG.LIM}$). When MODE = 0x09 or 0x0A, the CHGIN current limit is set as follows:
00 = 500mA (default); 01 = 900mA; 10 = 1200mA; 11 = 1500mA</td></tr>
</table>

Table 19. Charger Configuration 03 (0xBA)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_03</td><td>Charger configuration 03</td><td>0xBA</td><td>O
R/W (protected with CHGPROT)</td><td>0xDA</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>2:0</td><td>R/W</td><td>TO_ITH</td><td>010
(150mA)</td><td colspan="2">Topoff Current Threshold
The charger transitions from its fast-charge constant voltage mode to its topoff mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report topoff mode. This transition also starts the topoff time as programmed by TO_TIME.
0x00 = 100mA; 0x01 = 125mA; 0x02 = 150mA (default); 0x03 = 175mA; 0x04 = 200mA; 0x05 = 250mA; 0x06 = 300mA; 0x07 = 350mA</td></tr>
</table>

Table 19. Charger Configuration 03 (0xBA) (continued)

5:3	R/W	TO_TIME	011 (30min)	Topoff Timer Setting 0x00 = 0 min; 0x01 = 10 min; 0x02 = 20 min; 0x03 = 30 min 0x04 = 40 min; 0x05 = 50 min; 0x06 = 60 min; 0x07 = 70 min
7:6	R/W	ILIM	11	Program Buck Peak Current Limit 00 : Support I_{CHG} = 3.00A; 01 : Support I_{CHG} = 2.75A 10 : Support I_{CHG} = 2.50A; 11 : Support I_{CHG} = 2.25A

Table 20. Charger Configuration 04 (0xBB)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_04</td><td>Charger configuration 04</td><td>0xBB</td><td>O
R/W (protected with CHGPROT)</td><td>0x80</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>5:0</td><td>R/W</td><td>CHG_CV_PRM</td><td>000000
(4.2V)</td><td colspan="2">Primary Charge Termination Voltage Setting
When the charger is enabled and the main battery temperature is < T3 if JEITA = “1” or < T4 if JEITA = ”0”, then the charger’s battery regulation voltage (V_{BATREG}) is set by CHG_CV_PRM.
<table>
<tr><th>Bits</th><th>V</th><th>Bits</th><th>V</th><th>Bits</th><th>V</th></tr>
<tr><td>0x00</td><td>4.200</td><td>0x09</td><td>4.313</td><td>0x12</td><td>4.425</td></tr>
<tr><td>0x01</td><td>4.213</td><td>0x0A</td><td>4.325</td><td>0x13</td><td>4.438</td></tr>
<tr><td>0x02</td><td>4.225</td><td>0x0B</td><td>4.338</td><td>0x14</td><td>4.450</td></tr>
<tr><td>0x03</td><td>4.238</td><td>0x0C</td><td>4.350</td><td>0x15</td><td>4.463</td></tr>
<tr><td>0x04</td><td>4.250</td><td>0x0D</td><td>4.363</td><td>0x16</td><td>4.475</td></tr>
<tr><td>0x05</td><td>4.263</td><td>0x0E</td><td>4.375</td><td>0x17</td><td>4.488</td></tr>
<tr><td>0x06</td><td>4.275</td><td>0x0F</td><td>4.388</td><td>0x18</td><td>4.500</td></tr>
<tr><td>0x07</td><td>4.288</td><td>0x10</td><td>4.400</td><td></td><td></td></tr>
<tr><td>0x08</td><td>4.300</td><td>0x11</td><td>4.413</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>7:6</td><td>R/W</td><td>MINVSYS</td><td>10
(3.6V)</td><td colspan="2">Minimum System Regulation Voltage (V_{SYSMIN})
0x00 = 3.4V; 0x01 = 3.5V; 0x02 = 3.6V; 0x03 = 3.7V</td></tr>
</table>

Table 21. Charger Configuration 05 (0xBC)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_05</td><td>Charger configuration 05</td><td>0xBC</td><td>O
R/W (protected with CHGPROT)</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>1:0</td><td>R/W</td><td>CHGIN_OVP</td><td>00
(13.7V)</td><td colspan="2">OVP Threshold Selection
00 = 13.7V (default); 01 = 10.2V; 10 = 8.0V; 11 = 5.85V</td></tr>
<tr><td>3:2</td><td>R/W</td><td>I_PREQUAL</td><td>00
(50mA)</td><td colspan="2">Prequal Current Selection
00 = 50mA (default); 01 = 100mA; 10 = 200mA; 11 = 400mA</td></tr>
<tr><td>4</td><td>R/W</td><td>CHGIN_PD_FST</td><td>0
(44kΩ)</td><td colspan="2">Enable Stronger Discharge Path in CHGIN
0 : 44kΩ; 1 : 8kΩ</td></tr>
<tr><td>5</td><td>R/W</td><td>EN_THM_PRECHG</td><td>0</td><td colspan="2">Enable long debounce time to allow THM pins precharge time. This is useful when the user connects the capacitor to THMB/THMV.
0 : Disable, thermistor debounce = 448μs
1 : Enable, thermistor debounce = 12ms</td></tr>
<tr><td>7:6</td><td>R/W</td><td>RSVD</td><td>00</td><td colspan="2">Reserved</td></tr>
</table>

Table 22. Charger Configuration 06 (0xBD)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_06		Charger configuration 06	0xBD	O	0x80
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
1:0	R/W	WDTCLR	00	Watchdog Timer Clear Bits. Writing “01” to these bits clears the watchdog timer when the watchdog timer is enabled. 0x00 = The watchdog timer is not cleared. 0x01 = The watchdog timer is cleared. 0x02 = The watchdog timer is not cleared. 0x03 = The watchdog timer is not cleared.	
3:2	R/W	CHGPROT	00	Charger Settings Protection Bits. Writing "11" to these bits unlocks the write capability for the registers who are "Protected with CHGPROT." Writing any value besides "11" locks these registers. 0x00 = Write capability is locked. 0x01 = Write capability is locked. 0x02 = Write capability is locked. 0x03 = Write capability is unlocked.	
4	R/W	MAXOTG_EN	0	MAXOTG Feature Enable Bit 0 = MaxOTG feature is disabled (default). 1 = MaxOTG feaure is enabled.	
5	R/W	OTG_DC	0	OTG Fault Duty Cycle Selection Bit 0 = 10% ON duty cycle when OTG hits current limit (default). 1 = 1% ON duty cycle when OTG hits current limit.	
6	R/W	EN_THM	0	Enable Thermistor Control in Charger 0 = No thermistor control in charger (default). 1 = Have thermistor control in charger. Charging is stopped when battery temp > 60deg or < 0deg.	
7	R/W	LEDEN	1	Charging Status Indicator LED Enable 0 = Charging status indicator LED is disabled. 1 = Charging status indicator LED is enabled.	

Table 23. Charger Configuration 07 (0xBE)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_07		Charger configuration 07	0xBE	O R/W (protected with CHGPROT)	0x30
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
1:0	R/W	BOVE	00	Early Battery Overvoltage Setting to Disable Slave Chargers 00 : Disable BOVE feature 01 : BOVE = BATV regulation 10 : BOVE = 1.3% above BATV regulation 11 : BOVE = 2.6% above BATV regulation	
2	R/W	DIS_QBATOFF	0	Disable QBATOFF in case of battery overcurrent hit limit. 0 = Charger controls Q_{BAT} switch; Q_{BAT} is turned off in case battery overcurrent occurs for 6ms. 1 = Q_{BAT} is not turned off when battery overcurrent occurs	
6:3	R/W	REGTEMP	0110	Junction Temperature Thermal Regulation Loop Set Point. The charger’s target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint. 0x00 = 85°C; 0x01 = 90°C; 0x02 = 95°C; 0x03 = 100°C; 0x04 = 105°C; 0x05 = 110°C; 0x06 = 115°C (default); 0x07 = 120°C; 0x08 = 125°C; 0x09 = 130°C	

Table 23. Charger Configuration 07 (0xBE) (continued)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_07</td><td>Charger configuration 07</td><td>0xBE</td><td>O
R/W (protected with CHGPROT)</td><td>0x30</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>R/W</td><td>WD_QBATOFF</td><td>0</td><td colspan="2">0 : When watchdog timer expires, turn off only the charger.
1 : When watchdog timer expires, turn off buck, charger, and Q_{BAT} switch.</td></tr>
</table>

Table 24. Charger Configuration 09 (0xC0)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_09</td><td>Charger configuration 09</td><td>0xC0</td><td>O</td><td>0x0F</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>6:0</td><td>R/W</td><td>CHGIN_ILIM</td><td>0x0F
(0.50A)</td><td colspan="2">Maximum Input Current Limit Selection. 7-bit adjustment from 100mA to 4.0A in 33mA steps. **Note:** The first four codes are all 100mA.
<table>
<tr><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th><th>Bits</th><th>Unit (mA)</th></tr>
<tr><td>0x00</td><td>100</td><td>0x20</td><td>1067</td><td>0x40</td><td>2133</td><td>0x60</td><td>3200</td></tr>
<tr><td>0x01</td><td>100</td><td>0x21</td><td>1100</td><td>0x41</td><td>2167</td><td>0x61</td><td>3233</td></tr>
<tr><td>0x02</td><td>100</td><td>0x22</td><td>1133</td><td>0x42</td><td>2200</td><td>0x62</td><td>3267</td></tr>
<tr><td>0x03</td><td>100</td><td>0x23</td><td>1167</td><td>0x43</td><td>2233</td><td>0x63</td><td>3300</td></tr>
<tr><td>0x04</td><td>133</td><td>0x24</td><td>1200</td><td>0x44</td><td>2267</td><td>0x64</td><td>3333</td></tr>
<tr><td>0x05</td><td>167</td><td>0x25</td><td>1233</td><td>0x45</td><td>2300</td><td>0x65</td><td>3367</td></tr>
<tr><td>0x06</td><td>200</td><td>0x26</td><td>1267</td><td>0x46</td><td>2333</td><td>0x66</td><td>3400</td></tr>
<tr><td>0x07</td><td>233</td><td>0x27</td><td>1300</td><td>0x47</td><td>2367</td><td>0x67</td><td>3433</td></tr>
<tr><td>0x08</td><td>267</td><td>0x28</td><td>1333</td><td>0x48</td><td>2400</td><td>0x68</td><td>3467</td></tr>
<tr><td>0x09</td><td>300</td><td>0x29</td><td>1367</td><td>0x49</td><td>2433</td><td>0x69</td><td>3500</td></tr>
<tr><td>0x0A</td><td>333</td><td>0x2A</td><td>1400</td><td>0x4A</td><td>2467</td><td>0x6A</td><td>3533</td></tr>
<tr><td>0x0B</td><td>367</td><td>0x2B</td><td>1433</td><td>0x4B</td><td>2500</td><td>0x6B</td><td>3567</td></tr>
<tr><td>0x0C</td><td>400</td><td>0x2C</td><td>1467</td><td>0x4C</td><td>2533</td><td>0x6C</td><td>3600</td></tr>
<tr><td>0x0D</td><td>433</td><td>0x2D</td><td>1500</td><td>0x4D</td><td>2567</td><td>0x6D</td><td>3633</td></tr>
<tr><td>0x0E</td><td>467</td><td>0x2E</td><td>1533</td><td>0x4E</td><td>2600</td><td>0x6E</td><td>3667</td></tr>
<tr><td>0x0F</td><td>500</td><td>0x2F</td><td>1567</td><td>0x4F</td><td>2633</td><td>0x6F</td><td>3700</td></tr>
<tr><td>0x10</td><td>533</td><td>0x30</td><td>1600</td><td>0x50</td><td>2667</td><td>0x70</td><td>3733</td></tr>
<tr><td>0x11</td><td>567</td><td>0x31</td><td>1633</td><td>0x51</td><td>2700</td><td>0x71</td><td>3767</td></tr>
<tr><td>0x12</td><td>600</td><td>0x32</td><td>1667</td><td>0x52</td><td>2733</td><td>0x72</td><td>3800</td></tr>
<tr><td>0x13</td><td>633</td><td>0x33</td><td>1700</td><td>0x53</td><td>2767</td><td>0x73</td><td>3833</td></tr>
<tr><td>0x14</td><td>667</td><td>0x34</td><td>1733</td><td>0x54</td><td>2800</td><td>0x74</td><td>3867</td></tr>
<tr><td>0x15</td><td>700</td><td>0x35</td><td>1767</td><td>0x55</td><td>2833</td><td>0x75</td><td>3900</td></tr>
<tr><td>0x16</td><td>733</td><td>0x36</td><td>1800</td><td>0x56</td><td>2867</td><td>0x76</td><td>3933</td></tr>
<tr><td>0x17</td><td>767</td><td>0x37</td><td>1833</td><td>0x57</td><td>2900</td><td>0x77</td><td>3967</td></tr>
<tr><td>0x18</td><td>800</td><td>0x38</td><td>1867</td><td>0x58</td><td>2933</td><td>0x78</td><td>4000</td></tr>
<tr><td>0x19</td><td>833</td><td>0x39</td><td>1900</td><td>0x59</td><td>2967</td><td>0x79</td><td>4000</td></tr>
<tr><td>0x1A</td><td>867</td><td>0x3A</td><td>1933</td><td>0x5A</td><td>3000</td><td>0x7A</td><td>4000</td></tr>
<tr><td>0x1B</td><td>900</td><td>0x3B</td><td>1967</td><td>0x5B</td><td>3033</td><td>0x7B</td><td>4000</td></tr>
<tr><td>0x1C</td><td>933</td><td>0x3C</td><td>2000</td><td>0x5C</td><td>3067</td><td>0x7C</td><td>4000</td></tr>
<tr><td>0x1D</td><td>967</td><td>0x3D</td><td>2033</td><td>0x5D</td><td>3100</td><td>0x7D</td><td>4000</td></tr>
<tr><td>0x1E</td><td>1000</td><td>0x3E</td><td>2067</td><td>0x5E</td><td>3133</td><td>0x7E</td><td>4000</td></tr>
<tr><td>0x1F</td><td>1033</td><td>0x3F</td><td>2100</td><td>0x5F</td><td>3167</td><td>0x7F</td><td>4000</td></tr>
</table></td></tr>
<tr><td>7</td><td>R/W</td><td>OVPDRV_CTL</td><td>0</td><td colspan="2">OVPDRV FET Override Software Control Bit
0 : OVPDRV FET is controlled by charger internal logic.
1 : OVPDRV is forced ON regardless of charger internal logic.</td></tr>
</table>

Table 25. Charger Configuration 10 (0xC1)

NAME		FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_10		Charger configuration 10	0xC1	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
0	R/W	DISSKIP	0	Disable Skip Mode During Buck/Charging Mode 0 = Auto buck skip mode; 1 = Disable buck skip mode.	
1	R/W	TODEB_EN	0	Enable MAX77860 Topoff Long Debouncer 0 = MAX77860 topoff deboucer is 56ms; Slave registers are not reset when master enters topoff state. 1 = MAX77860 topoff deboucer is set by register "TODEB[1:0]"; Slave registers are reset when master CHG_CC < topoff threshold for 56ms.	
3:2	R/W	TODEB[1:0]	00	Topoff long debounce timer: 00 = 112ms; 01 = 224ms; 10 = 448ms; 10 = 896ms	
7:4	R/W	RSVD	0000	Reserved	

Table 26. Charger Configuration 11 (0xC2)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_11</td><td>Charger configuration 11</td><td>0xC2</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>6:0</td><td>R/W</td><td>VBYPSET</td><td>0x00
(3V)</td><td colspan="2">Bypass Target Output Voltage in Boost Mode. 3V (0x00) to 5.75V (0x6E) in 0.025V steps. This setting is valid for the “boost only” mode (MODE = 0x08).
<table>
<tr><th>Bits</th><th>Unit (V)</th><th>Bits</th><th>Unit (V)</th><th>Bits</th><th>Unit (V)</th><th>Bits</th><th>Unit (V)</th></tr>
<tr><td>0x00</td><td>3.000</td><td>0x20</td><td>3.800</td><td>0x40</td><td>4.600</td><td>0x60</td><td>5.400</td></tr>
<tr><td>0x01</td><td>3.025</td><td>0x21</td><td>3.825</td><td>0x41</td><td>4.625</td><td>0x61</td><td>5.425</td></tr>
<tr><td>0x02</td><td>3.050</td><td>0x22</td><td>3.850</td><td>0x42</td><td>4.650</td><td>0x62</td><td>5.450</td></tr>
<tr><td>0x03</td><td>3.075</td><td>0x23</td><td>3.875</td><td>0x43</td><td>4.675</td><td>0x63</td><td>5.475</td></tr>
<tr><td>0x04</td><td>3.100</td><td>0x24</td><td>3.900</td><td>0x44</td><td>4.700</td><td>0x64</td><td>5.500</td></tr>
<tr><td>0x05</td><td>3.125</td><td>0x25</td><td>3.925</td><td>0x45</td><td>4.725</td><td>0x65</td><td>5.525</td></tr>
<tr><td>0x06</td><td>3.150</td><td>0x26</td><td>3.950</td><td>0x46</td><td>4.750</td><td>0x66</td><td>5.550</td></tr>
<tr><td>0x07</td><td>3.175</td><td>0x27</td><td>3.975</td><td>0x47</td><td>4.775</td><td>0x67</td><td>5.575</td></tr>
<tr><td>0x08</td><td>3.200</td><td>0x28</td><td>4.000</td><td>0x48</td><td>4.800</td><td>0x68</td><td>5.600</td></tr>
<tr><td>0x09</td><td>3.225</td><td>0x29</td><td>4.025</td><td>0x49</td><td>4.825</td><td>0x69</td><td>5.625</td></tr>
<tr><td>0x0A</td><td>3.250</td><td>0x2A</td><td>4.050</td><td>0x4A</td><td>4.850</td><td>0x6A</td><td>5.650</td></tr>
<tr><td>0x0B</td><td>3.275</td><td>0x2B</td><td>4.075</td><td>0x4B</td><td>4.875</td><td>0x6B</td><td>5.675</td></tr>
<tr><td>0x0C</td><td>3.300</td><td>0x2C</td><td>4.100</td><td>0x4C</td><td>4.900</td><td>0x6C</td><td>5.700</td></tr>
<tr><td>0x0D</td><td>3.325</td><td>0x2D</td><td>4.125</td><td>0x4D</td><td>4.925</td><td>0x6D</td><td>5.725</td></tr>
<tr><td>0x0E</td><td>3.350</td><td>0x2E</td><td>4.150</td><td>0x4E</td><td>4.950</td><td>0x6E</td><td>5.750</td></tr>
<tr><td>0x0F</td><td>3.375</td><td>0x2F</td><td>4.175</td><td>0x4F</td><td>4.975</td><td></td><td></td></tr>
<tr><td>0x10</td><td>3.400</td><td>0x30</td><td>4.200</td><td>0x50</td><td>5.000</td><td></td><td></td></tr>
<tr><td>0x11</td><td>3.425</td><td>0x31</td><td>4.225</td><td>0x51</td><td>5.025</td><td></td><td></td></tr>
<tr><td>0x12</td><td>3.450</td><td>0x32</td><td>4.250</td><td>0x52</td><td>5.050</td><td></td><td></td></tr>
<tr><td>0x13</td><td>3.475</td><td>0x33</td><td>4.275</td><td>0x53</td><td>5.075</td><td></td><td></td></tr>
<tr><td>0x14</td><td>3.500</td><td>0x34</td><td>4.300</td><td>0x54</td><td>5.100</td><td></td><td></td></tr>
<tr><td>0x15</td><td>3.525</td><td>0x35</td><td>4.325</td><td>0x55</td><td>5.125</td><td></td><td></td></tr>
<tr><td>0x16</td><td>3.550</td><td>0x36</td><td>4.350</td><td>0x56</td><td>5.150</td><td></td><td></td></tr>
<tr><td>0x17</td><td>3.575</td><td>0x37</td><td>4.375</td><td>0x57</td><td>5.175</td><td></td><td></td></tr>
<tr><td>0x18</td><td>3.600</td><td>0x38</td><td>4.400</td><td>0x58</td><td>5.200</td><td></td><td></td></tr>
<tr><td>0x19</td><td>3.625</td><td>0x39</td><td>4.425</td><td>0x59</td><td>5.225</td><td></td><td></td></tr>
<tr><td>0x1A</td><td>3.650</td><td>0x3A</td><td>4.450</td><td>0x5A</td><td>5.250</td><td></td><td></td></tr>
<tr><td>0x1B</td><td>3.675</td><td>0x3B</td><td>4.475</td><td>0x5B</td><td>5.275</td><td></td><td></td></tr>
<tr><td>0x1C</td><td>3.700</td><td>0x3C</td><td>4.500</td><td>0x5C</td><td>5.300</td><td></td><td></td></tr>
<tr><td>0x1D</td><td>3.725</td><td>0x3D</td><td>4.525</td><td>0x5D</td><td>5.325</td><td></td><td></td></tr>
<tr><td>0x1E</td><td>3.750</td><td>0x3E</td><td>4.550</td><td>0x5E</td><td>5.350</td><td></td><td></td></tr>
<tr><td>0x1F</td><td>3.775</td><td>0x3F</td><td>4.575</td><td>0x5F</td><td>5.375</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>7</td><td>R/W</td><td>RSVD</td><td>0</td><td colspan="2">Reserved</td></tr>
</table>

Table 27. Charger Configuration 12 (0xC3)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CHG_CNFG_12</td><td>Charger configuration 12</td><td>0xC3</td><td>O</td><td>0x44</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>3:0</td><td>R/W</td><td>B2SOVRC</td><td>0100</td><td colspan="2">BAT to SYS Overcurrent Threshold
0x00 = Disabled 0x08 = 6.5
0x01 = 3.0A 0x09 = 7.0A
0x02 = 3.5A 0x0A = 7.5A
0x03 = 4.0A 0x0B = 8.0A
0x04 = 4.5A (default) 0x0C = 8.5A
0x05 = 5.0A 0x0D = 9.0A
0x06 = 5.5A 0x0E = 9.0A
0x07 = 6.0A 0x0F = 9.0A</td></tr>
<tr><td>5:4</td><td>R/W</td><td>VCHGIN_REG</td><td>00</td><td colspan="2">CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment
The CHGIN to GND minimum turn-on threshold (V_{CHGIN_UVLO}) also scales with this adjustment.
0x00 = V_{CHGIN_REG} = 4.2V and V_{CHGIN_UVLO} = 4.5V
0x01 = V_{CHGIN_REG} = 4.6V and V_{CHGIN_UVLO} = 4.9V
0x02 = V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 5.0V
0x03 = V_{CHGIN_REG} = 4.8V and V_{CHGIN_UVLO} = 5.1V</td></tr>
<tr><td>6</td><td>R/W</td><td>CHGINSEL</td><td>1</td><td colspan="2">CHGIN/USB Input Channel Select
0 = Disabled
1 = Enabled</td></tr>
<tr><td>7</td><td>R/W</td><td>CHG_LPM</td><td>0</td><td colspan="2">Charger DC-DC Low-Power Mode
0 = Normal current capability.
1 = Set CHG_LPM to increase efficiency when the DC-DC current is less than 900mA.</td></tr>
</table>

USB Type-C Register

Table 28. BC_INT (0x00)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">BC_INT</td><td>Interrupt</td><td>0x00</td><td>S</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>R/C</td><td>VBUSDet</td><td>0</td><td colspan="2">0 : No change; 1 : New V_{BUSDet} status</td></tr>
<tr><td>6</td><td>R/C</td><td>DxOVPI</td><td>0</td><td colspan="2">0 : No change; 1 : New DxOVP status</td></tr>
<tr><td>5</td><td>R/C</td><td>DNVDATREFI</td><td>0</td><td colspan="2">0 : No change; 1 : New DN_VDAT_REF status</td></tr>
<tr><td>4</td><td>R/C</td><td>ChgTypRunFI</td><td>0</td><td colspan="2">Charge Detection Running Falling (ChgTypRun) Edge Interrupt
0 : No change; 1 : New ChgTypRunF status</td></tr>
<tr><td>3</td><td>R/C</td><td>ChgTypRunRI</td><td>0</td><td colspan="2">Charge Detection Running Rising (ChgTypRun) Edge Interrupt
0 : No change; 1 : New ChgTypRunR status</td></tr>
<tr><td>2</td><td>R/C</td><td>PrChgTypI</td><td>0</td><td colspan="2">0 : No change; 1 : New PrChgTyp status</td></tr>
<tr><td>1</td><td>R/C</td><td>DCDTmoI</td><td>0</td><td colspan="2">0 : No change; 1 : New DCDTmo status</td></tr>
<tr><td>0</td><td>R/C</td><td>ChgTypI</td><td>0</td><td colspan="2">0 : No change; 1 : New ChgTyp status</td></tr>
</table>

***Note**: Always read CC_INT (0x01) before reading BC_INT (0x00).*

Table 29. CC_INT (0x01)

NAME	FUNCTION	ADDR	TYPE	RESET
CC_INT	Interrupt	0x01	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
7	R/C	RSVD	0	Reserved
6	R/C	VSAFE0V_I	0	0 : No change; 1 : New $V_{SAFE0V0}$ status
5	R/C	DetAbrtI	0	0 : No change; 1 : New DetAbrt status
4	R/C	RSVD	0	Reserved
3	R/C	CCPinStatI	0	0 : No change; 1 : New CCPinStat status
2	R/C	CCIStatI	0	0 : No change; 1 : New CCIStat status
1	R/C	CCVcnStatI	0	0 : No change; 1 : New CCVcnStat status
0	R/C	CCStatI	0	0 : No change; 1 : New CCStat status

Table 30. BC_INTMASK (0x02)

NAME	FUNCTION	ADDR	TYPE	RESET
BC_INTMASK	Interrupt Mask	0x02	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
7	R/W	VBUSDetM	1	0 : Mask; 1 : Unmask
6	R/W	DxOVPM	1	0 : Mask; 1 : Unmask
5	R/W	DNVDATREFM	1	0 : Mask; 1 : Unmask
4	R/W	ChgTypRunFM	1	0 : Mask; 1 : Unmask
3	R/W	ChgTypRunRM	1	0 : Mask; 1 : Unmask
2	R/W	PrChgTypM	1	0 : Mask; 1 : Unmask
1	R/W	DCDTmoM	1	0 : Mask; 1 : Unmask
0	R/W	ChgTypM	1	0 : Mask; 1 : Unmask

Table 31. CC_INTMASK (0x03)

NAME	FUNCTION	ADDR	TYPE	RESET
CC_INTMASK	Interrupt Mask	0x03	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
7	R/W	RSVD	1	Reserved
5	R/W	VSAFE0V_M	1	0 : Mask; 1 : Unmask
5	R/W	DetAbrtM	1	0 : Mask; 1 : Unmask
4	R/W	RSVD	1	Reserved
3	R/W	CCPinStatM	1	0 : Mask; 1 : Unmask
2	R/W	CCIStatM	1	0 : Mask; 1 : Unmask
1	R/W	CCVcnStatM	1	0 : Mask; 1 : Unmask
0	R/W	CCStatIM	1	0 : Mask; 1 : Unmask

Table 32. BC_STATUS1 (0x04)

NAME	FUNCTION	ADDR	TYPE	RESET
BC_STATUS1	Status	0x04	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
7	R	VBUSDet	0	Status of V_{BUS} Detection 0 : $V_{BUS} < V_{VBDET}$; 1 : $V_{BUS} > V_{VBDET}$
6	R	ChgTypRun	0	Charger Detection Running Status 0 : Not running; 1 : Running
5:3	R	PrChgTyp	0	Output of Proprietary Charger Detection 000 : Unknown; 001 : Samsung 2A; 010 : Apple 0.5A; 011 : Apple 1A; 100 : Apple 2A; 101 : Apple 12W; 110 : 3A DCP (if enabled); 111 : RFU
2	R	DCDTmo	0	During charger detection, DCD detection timed out. Indicates D+/D- are open. BC1.2 detection continues as required by BC 1.2 specification but SDP most likely is found. 0 : No timeout or detection has not run. 1 : DCD timeout occurred
1:0	R	ChgTyp	0	Output of Charger Detection 00 : Nothing attached 01 : SDP, USB cable attached. 10 : CDP, Charging downstream port. Current depends on USB operating speed. 11 : DCP, Dedicated charger. Current up to 1.5A.

Table 33. BC_STATUS2 (0x05)

NAME	FUNCTION	ADDR	TYPE	RESET
BC_STATUS2	Status	0x05	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
7:2	R	RSVD	0	Reserved
1	R	DxOVP		0 : Dn and DP < DxOVP; 1 : Dn or DP > DxOVP
0	R	DNVDATREF	0	0 : Dn < V_{DAT_REF} debounce for t_{CDDeb} 1 : Dn > V_{DAT_REF} debounce for t_{CDDeb}

Table 34. CC_STATUS1 (0x06)

NAME	FUNCTION	ADDR	TYPE	RESET
CC_STATUS1	Status	0x06	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
7:6	R	CCPinStat	0	Output of Active CC Pin 00 : No determination; 01 : CC1 Active 10 : CC2 Active; 11 : RFU
5:4	R	CCIStat	0	CC Pin Detected Allowed V_{BUS} Current in UFP Mode 00 : Not in UFP mode; 01 : 500mA 10 : 1.5A; 11: 3.0A
3	R	CCVcnStat	0	Status of V_{CONN} Output 0 : V_{CONN} disabled; 1 : V_{CONN} enabled
2:0	R	CCStat	0	CC Pin State Machine Detection 000 : No connection; 001 : UFP 010 : DFP; 011 : Audio accessory 100 : Debug accessory; 101 : Error 110 : Disabled; 111 : RFU

Table 35. CC_STATUS2 (0x07)

NAME		FUNCTION	ADDR	TYPE	RESET
CC_STATUS2		Status	0x07	S	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:4	R	RSVD	0	Reserved	
2	R	VSAFE0V_S	1	0 : $V_{BUS} < V_{SAFE0V}$ 1 : $V_{BUS} > V_{SAFE0V}$	
2	R	DetAbrt	1	0 : Charger detection runs if ChgDetEn = 1 and V_{BUS} is valid for the debounce time. 1 : Charger detection is aborted by Type-C state machine. Charger does not run if ChgDetEn = 1 and V_{BUS} is valid for the debounce time. ChgDetMan allows manual run of charger detection. If charger detection is in progress, DetAbrt = 1 immediately stops the in progress detection.	
1:0	R	RSVD	0	Reserved	

Table 36. BC_CTRL1 (0x08)

NAME		FUNCTION	ADDR	TYPE	RESET
BC_CTRL1		Control	0x08	S	0x05
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:6	R/W	RSVD	0	Reserved	
5	R/W	NoAutoIBUS	0	Disabling of automatic input current limit from adapter detection. '0' = Automatic determined using adapter detection. '1' = Current limit setting controlled manually through I^2C.	
4	R/W	3ADCPDet	0	Enable detection of 3A DCP (adds detection step after BC 1.2 completes to detect presence of 3A DCP – D+/D- short with 2 series diode clamp). 0 : Not enabled; 1 : Enabled	
3:2	R/W	SfOutCtrl	1	Control Over Safeout LDO 00 : Always disabled 01 : On if a valid CHGIN voltage is present. 10 : Turns on in the following conditions: ● ChgDetEn = 1 and CHGIN is valid and ChgDetRun indicates no detection running. ● ChgDetEn = 0 and CHGIN is valid. 11 : RFU	
1	R/W	ChgDetMan	0	Force manual run of charger detection.Bit auto resets to 0. 0 : Not enabled; 1 : Request manual run of charger detection.	
0	R/W	ChgDetEn	1	Enable Charger Detection 0 : Not enabled; 1 : Enabled (Charger detection runs every time $V_{BUS} > V_{VBDET}$.)	

Table 37. BC_CTRL2 (0x09)

NAME		FUNCTION	ADDR	TYPE	RESET
BC_CTRL2		Control	0x09	Cleared on V_{BUS} Removal	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:6	R/W	RSVD	0	Reserved	
5	R/W	DN_MON_EN	0	0 = Disabled. DNVDATREF is set to 0. 1 = Enabled	

Table 37. BC_CTRL2 (0x09) (continued)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">BC_CTRL2</td><td>Control</td><td>0x09</td><td>Cleared on V_{BUS} Removal</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>4</td><td>R/W</td><td>DPDNMan</td><td>0</td><td colspan="2">0 = Resources on DP and DN are controlled by charger detection (ChgDetEn bit).
1 = Drive voltages on DP and DN according to DPDrv and DNDrv values.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>DPDrv</td><td>0</td><td colspan="2">Force Voltage on DP
00 = Ground (15k resistor to GND); 01 = 0.6V
10 = 3.3V; 11 = Open</td></tr>
<tr><td>1:0</td><td>R/W</td><td>DNDrv</td><td>0</td><td colspan="2">Force Voltage on DP
00 = Ground (15k resistor to GND); 01 = 0.6V
10 = 3.3V; 11 = Open</td></tr>
</table>

Table 38. CC_CTRL1 (0x0A)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">CC_CTRL1</td><td>Control</td><td>0x0A</td><td>S</td><td>0x19</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>R/W</td><td>CCSrcCurCh</td><td>0</td><td colspan="2">Request new pullup value to advertise a new allowed max current value while in source downstream facing port (DFP) mode.
Note: This bit resets to 0 automatically so a read always returns 0.
0 : No change request.
1 : Request value in CCSrcCur to be read.</td></tr>
<tr><td>6:5</td><td>R/W</td><td>CCSrcCur</td><td>0</td><td colspan="2">New request value for source mode pullup.
Note: This value is latched in when the CCSrcCurCh bit is written to 1. Changes to the pullup value only take place if the operation state is DFP (CCStat = 010b). The pullup value is automatically returned to 0.5A when DFP mode is exited so this value may not represent the actual pullup in use.
00 : Request change to 0.5A.
01 : Request change to 1.5A.
10 : Request change to 3.0A.
11 : Reserved</td></tr>
<tr><td>4</td><td>R/W</td><td>CCSrcSnk</td><td>1</td><td colspan="2">Allow State Machine to Enter Sink Mode (UFP) Detection
Note: USB PD role swap is allowed to enter sink mode. See the <i>Charger State Diagram</i> for details.
0 : Disable; 1 : Enabled</td></tr>
<tr><td>3</td><td>R/W</td><td>CCSnkSrc</td><td>1</td><td colspan="2">Allow State Machine to Enter Source Mode (DFP) Detection
Note: USB PD role swap is allowed to enter source mode. See the <i>Charger State Diagram</i> for details.
0 : Disable; 1 : Enabled</td></tr>
<tr><td>2</td><td>R/W</td><td>CCDbgEn</td><td>0</td><td colspan="2">Enable Detection of Type-C Debug Adapter
0 : Disabled; 1 : Enabled</td></tr>
<tr><td>1</td><td>R/W</td><td>CCAudEn</td><td>0</td><td colspan="2">Enable Detection of Type-C Audio Adapter
0 : Disabled; 1 : Enabled</td></tr>
<tr><td>0</td><td>R/W</td><td>CCDetEn</td><td>1</td><td colspan="2">Enable CC Pin Detection. Force state machine to disabled state.
0 : Disabled; 1 : Enabled</td></tr>
</table>

Table 39. CC_CTRL2 (0x0B)

NAME		FUNCTION	ADDR	TYPE	RESET
CC_CTRL2		Control	0x0B	S	0x04
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	CCForceError	0	Bit Resets to 0 After a Write (Read is always 0) 0 : No action; 1 : Force transition to ErrorRecovery state.	
6	R/W	SnkAttachedLock	0	Bit Resets to 0 After a Minimum of 1.1s 0 : Exit sink attached when V_{BUS} < V_{BDET} for more than $t_{PDDebounce}$. 1 : Locked in sink attached for a minimum of 1.1s if V_{BUS} is missing.	
5	R/W	CCSnkSrcSwp	0	USB PD Power Role Swap from Sink to Source. This bit must be written to 0 once the USB PD controller completes the power role swap sequence. 0 : No swap requested; 1 : Swap requested	
4	R/W	CCSrcSnkSwp	0	USB PD Power Role Swap from Source to Sink. This bit must be written to 0 once the USB PD controller completes the power role swap sequence. 0 : No swap requested; 1 : Swap requested	
3	R/W	CCVcnSwp	0	Signal State Machine to Swap V_{CONN} roles. Bit resets to 0 after a write (read is always 0) 0 : No change in V_{CONN} role; 1 : Force change in V_{CONN}	
2	R/W	CCVcnEn	1	Force State of V_{CONN} 0 : Force V_{CONN} off (both external boost converter and V_{CONN} switch). 1 : Automatic operation based on state machine.	
1	R/W	CCSrcRst	0	Force a reset of the state machine. Immediate transition to unattached.SRC state. Bit resets to 0 after a write (read is always 0). 0 : No reset; 1 : Request reset	
0	R/W	CCSnkRst	0	Force a reset of the State Machine. Immediate transition to unattached.SNK state. Bit resets to 0 after a write (read is always 0). 0: No reset; 1: Request reset	

Table 40. CC_CTRL3 (0x0C)

NAME		FUNCTION	ADDR	TYPE	RESET
CC_CTRL3		Control	0x0C	S	0x03
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:4	R/W	RSVD	0	Reserved	
3	R/W	CCPreferSink	0	0 : Disabled 1 : Enabled	
2	R/W	CCTrySnk	0	0 : Disabled 1 : Enabled	
1:0	R/W	CCDRPPhase	3	Percent of time device is acting as unattached.SRC when CCSNKSRC = 1 and CCSRCSNK = 1. 00 : 35%; 01 : 40%; 10 : 45%; 11 : 50%	

Table 41. CHGIN_ILIM1 (0x0D)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGIN_ILIM1		Status	0x0D	S	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	

Table 41. CHGIN_ILIM1 (0x0D) (continued)

7	R	RSVD	0	Reserved
6:0	R	CHGIN_ILIM	0	Status of charger input current limit set by charger detection HW. 7 bit adjustment from 100mA to 4.0A. Setting 0x01 to 0x03 = 100mA Setting 0x04 to 0x78 = increment 33mA steps Setting 0x78 to 0x7F = 4.0A

Table 42. CHGIN_ILIM2 (0x0E)

NAME		FUNCTION	ADDR	TYPE	RESET
CHGIN_ILIM2		Status	0x0E	S	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:4	R/W	RSVD	0	Reserved	
3	R/W	CHGIN_ILIM_GATE	0	0 : No modification of CHGIN_LIM. 1 : Limit CDP to 1.5A. ChgTyp ≥ 10 (CDP) and PrChgTyp ≥ 000 (unknown) set CHGIN_LIM to 0x2D.	
2:1	R/W	SDP_MAX_CUR	0	0x0 : No modification of CHGIN_LIM. 0x1 : Limit SDP to 500mA. ChgTyp ≥ 01 (SDP) and PrChgTyp ≥ 000 (unknown) set CHGIN_LIM to 0x0F. 0x2 : Limit SDP to 1.0A. ChgTyp ≥ 01 (SDP) and PrChgTyp ≥ 000 (unknown) set CHGIN_LIM to 0x1E. 0x3 : Limit SDP to 1.5A. ChgTyp ≥ 01 (SDP) and PrChgTyp ≥ 000 (unknown) set CHGIN_LIM to 0x2D.	
0	R/W	CDP_MAX_CUR	0	0 : No gating of CHGIN_LIM setting by BC 1.2 FSM. 1 : Gate changes in CHGIN_LIM until BC 1.2 FSM completes. ChgTypRun ≥ 0	

Master Slave

Table 43. S-Wire Interrupt (0x80)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI_INT		S-Wire interrupt	0x80	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:5	R/C	RSVD	000	Reserved	
4	R/C	SLAVE2_FAULT_I	0	SLAVE2 Fault Interrupt 0 = SLAVE Charger 2 does not have fault since the last time this bit was read. 1 = SLAVE Charger 2 has fault since the last time this bit was read.	
3	R/C	SLAVE1_FAULT_I	0	SLAVE1 Fault Interrupt 0 = SLAVE Charger 1 does not have fault since the last time this bit was read. 1 = SLAVE Charger 1 has fault since the last time this bit was read.	
2	R/C	CV_I	0	CC to CV Interrupt 0 = No CV transition since the last time this bit was read. 1 = Charger transition from CC to CV since the last time this bit was read. **Note:** This interrupt is only enabled when FGCC = 0 (fuel gauge 0x50<3>).	
1	R/C	SLAVE2_TREG_I	0	SLAVE Charger 2 Thermal Regulation Interrupt 0 = SLAVE2_S has not changed since the last time this bit was read. 1 = SLAVE2_S has changed since the last time this bit was read.	

Table 43. S-Wire Interrupt (0x80) (continued)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI_INT		S-Wire interrupt	0x80	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
0	R/C	SLAVE1_TREG_I	0	SLAVE Charger 1 Thermal Regulation Interrupt 0 = SLAVE1_S has not changed since the last time this bit was read. 1 = SLAVE1_S has changed since the last time this bit was read.	

Table 44. S-Wire Interrupt Mask (0x81)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI_INT_MASK		S-Wire interrupt Mask	0x81	O	0xFF
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:5	R/W	RSVD	111	Reserved	
4	R/W	SLAVE2_FAULT_M	1	SLAVE2 Fault Interrupt Mask 0 = SLAVE Charger 2 fault interrupt is not masked. 1 = SLAVE Charger 2 fault interrupt is masked.	
3	R/W	SLAVE1_FAULT_M	1	SLAVE1 Fault Interrupt Mask 0 = SLAVE Charger 1 fault interrupt is not masked. 1 = SLAVE Charger 1 fault interrupt is masked.	
2	R/W	CV_M	1	CV Interrupt Mask 0 = CV interrupt is not masked. 1 = CV interrupt is masked.	
1	R/W	SLAVE2_TREG_M	1	SLAVE2 Thermal Regulation Interrupt Mask 0 = SLAVE Charger 2 thermal regulation interrupt is not masked. 1 = SLAVE Charger 2 thermal regulation interrupt is masked.	
0	R/W	SLAVE1_TREG_M	1	SLAVE2 Thermal Regulation Interrupt Mask 0 = SLAVE Charger 2 thermal regulation interrupt is not masked. 1 = SLAVE Charger 2 thermal regulation interrupt is masked.	

Table 45. Slave Charger 1 CC (0x82)

NAME		FUNCTION	ADDR	TYPE	RESET
SLAVE1_CC		SLAVE1_CC_Setting	0x82	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	Dis_Slave1_AutoUpdate	0	Disable Slave Charger 1 Min Selector Between Master CC Setting and Slave1 CC Setting 0 = Min selector is on; Final Slave1 CC command to Slave1 = min (Master CC, Slave1 CC) 1 = Min selector is off; Final Slave1 CC command to Slave1 = Slave1 CC	
6	R/W	RSVD	0	Reserved	

Table 45. Slave Charger 1 CC (0x82) (continued)

5:0	R/W	SLAVE1_CC[5:0]	000000	SLAVE Charger 1 Constant Current Setting 0x00h = OFF = 0 pulse 0x01h = OFF = 1 pulse 0x02h = OFF = 2 pulses 0x03h = 100mA = 3 pulses 0x04h = 150mA = 4 pulses 0x05h = 200mA = 5 pulses . . 0x3Bh = 2950mA = 59 pulses 0x3Ch = 3000mA = 60 pulses 0x3Dh = 3000mA = 61 pulses 0x3Eh = 3000mA = 62 pulses 0x3Fh = 3000mA = 63 pulses

Table 46. Slave Charger 2 CC (0x83)

NAME		FUNCTION	ADDR	TYPE	RESET
SLAVE2_CC		SLAVE2_CC_Setting	0x83	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	Dis_Slave2_AutoUpdate	0	Disable Slave Charger 2 Min Selector Between Master CC Setting and Slave2 CC Setting 0 = Min selector is on; Final Slave2 CC command to Slave2 = min (Master CC, Slave2 CC) 1 = Min selector is off; Final Slave2 CC command to Slave2 = Slave2 CC	
6	R/W	RSVD	0	Reserved	
5:0	R/W	SLAVE2_CC[5:0]	000000	SLAVE Charger 2 Constant Current Setting 0x00h = OFF = 0 pulse 0x01h = OFF = 1 pulse 0x02h = OFF = 2 pulses 0x03h = 100mA = 3 pulses 0x04h = 150mA = 4 pulses 0x05h = 200mA = 5 pulses . . 0x3Bh = 2950mA = 59 pulses 0x3Ch = 3000mA = 60 pulses 0x3Dh = 3000mA = 61 pulses 0x3Eh = 3000mA = 62 pulses 0x3Fh = 3000mA = 63 pulses	

Table 47. S-Wire 1 Readback (0x84)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI1_READBACK		SLAVE1 CC ReadBack	0x84	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R	RSVD	0	Reserved	
6	R	RSVD	0	Reserved	
5:0	R	SWI1_READBACK[5:0]	000000	SLAVE Charger 1 Actual Constant Current Setting. This is a read only register.	

Table 48. S-Wire 2 Readback (0x85)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI2_READBACK		SLAVE2 CC ReadBack	0x84	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R	RSVD	0	Reserved	
6	R	RSVD	0	Reserved	
5:0	R	SWI2_READBACK[5:0]	000000	SLAVE Charger 2 Actual Constant Current Setting. This is a read only register.	

Table 49. S-Wire Status (0x86)

NAME		FUNCTION	ADDR	TYPE	RESET
SWI_STATUS		S-Wire Status	0x86	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:3	R	RSVD	00000	Reserved	
2	R	CV_S	0	MAX77860 Charger CV Status 0 = Charger is not in CV mode. 1 = Charger is in CV mode.	
1	R	SLAVE2_TREG_S	0	SLAVE2 Thermal Regulation Status 0 = SLAVE Charger 2 is not in thermal regulation. 1 = SLAVE Charger 2 is in thermal regulation.	
0	R	SLAVE1_TREG_S	0	SLAVE1 Thermal Regulation Status 0 = SLAVE Charger 1 is not in thermal regulation. 1 = SLAVE Charger 1 is in thermal regulation.	

ADC

Table 50. ADC_CONFIG1 (0x50)

NAME		FUNCTION	ADDR	TYPE	RESET
ADC_CONFIG1		ADC Configuration	0X50	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	$V_{BUS\_HV\_RANGE}$	0	V_{BUS} Monitoring Range (Channel 0) 0 : 2.7V–6.3V; LSB = 14mV; 1 : 6.3V–14.7V; LSB = 33mV	
6:5	R/W	ADC_Filter<1:0>	00	Averaging filter selection for all channels with filter enabled. 00: 2-Points averaging 01: 4-Points averaging 10: 8-Points averaging 11: 16-Points averaging	
4	R/W	CH4_OffsetCalEn	0	Enable offset calibration on channel 4 (R_{REXT}). 0 : Disable; 1 : Enable	
3	R/W	CH3_OffsetCalEn	0	Enable offset calibration on channel 3 (V_{BATT} current). 0 : Disable; 1 : Enable	
2	R/W	CH1_OffsetCalEn	0	Enable offset calibration on channel 1 (V_{BUS} current). 0 : Disable; 1 : Enable	
1	R/W	MEAS_ADC_CONT	0	ADC Mode 00 : Disable; 01 : Single mode; 10 : Continuous mode 11 : Continuous mode **Note:** MEAS_ADC_SINGLE is clear to 0 at the end of conversion.	

Table 51. ADC_CONFIG2 (0x51)

NAME		FUNCTION	ADDR	TYPE	RESET
ADC_CONFIG2		ADC Channel Enable	0X51	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	CH7_Enable	0	Channel 7 Enable (Test Channel) Range = 0.6V to 1.4V; LSB = 3.1mV 0 : Disable; 1 : Enable	
6	R/W	CH6_Enable	0	Channel 6 Enable (Reserved/VCM) Range = 0.6V to 1.4V; LSB = 3.1mV 0 : Disable; 1 : Enable	
5	R/W	CH5_Enable	0	Channel 5 Enable (Temperature in terms of THMV/THMB) Range = 20% to 80%; LSB = 0.24% 0 : Disable; 1 : Enable	
4	R/W	CH4_Enable	0	Channel 4 Enable (I_{REXT} Current) Range = (-10A) to (+10A); LSB = 78mA 0 : Disable; 1 : Enable	
3	R/W	CH3_Enable	0	Channel 3 Enable (V_{BATT} Current) Range = 0A to 3.1A; LSB = 12mA 0 : Disable; 1 : Enable	
2	R/W	CH2_Enable	0	Channel 2 Enable (V_{BATT} Voltage) Range = 2.1V to 4.9V; LSB = 11mV 0 : Disable; 1 : Enable	
1	R/W	CH1_Enable	0	Channel 1 Enable (V_{BUS} Current) Range = 0A to 4.1A; LSB = 16mA 0 : Disable; 1 : Enable	
0	R/W	CH0_Enable	0	Channel 0 Enable (V_{BUS} Voltage) $V_{BUS\_HV\_RANGE}$ = 0 : Range = 2.7V to 6.3V; LSB = 14mV $V_{BUS\_HV\_RANGE}$ = 1 : Range = 6.3V to 14.7V; LSB = 33mV 0 : Disable; 1 : Enable	

Table 52. ADC_CONFIG3 (0x52)

NAME		FUNCTION	ADDR	TYPE	RESET
ADC_CONFIG3		ADC Filter Enable	0X52	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7	R/W	CH7_FilterEn	0	Channel 7 Filter Enable; averaging filter point follows ADC_Filter<1:0> 0 : Disable; 1 : Enable	
6	R/W	CH6_FilterEn	0	Channel 6 Filter Enable; averaging filter point follows ADC_Filter<1:0> 0 : Disable; 1 : Enable	
5	R/W	CH5_FilterEn	0	Channel 5 Filter Enable; averaging filter point follows ADC_Filter<1:0> 0 : Disable; 1 : Enable	
4	R/W	CH4_FilterEn	0	Channel 4 Filter Enable; averaging filter point follows ADC_Filter<1:0> 0 : Disable; 1 : Enable	
3	R/W	CH3_FilterEn	0	Channel 3 Filter Enable; averaging filter point follows ADC_Filter<1:0> 0 : Disable; 1 : Enable	

Table 52. ADC_CONFIG3 (0x52) (continued)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_CONFIG3</td><td>ADC Filter Enable</td><td>0X52</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>2</td><td>R/W</td><td>CH2_FilterEn</td><td>0</td><td colspan="2">Channel 2 Filter Enable; averaging filter point follows ADC_Filter<1:0>
0 : Disable; 1 : Enable</td></tr>
<tr><td>1</td><td>R/W</td><td>CH1_FilterEn</td><td>0</td><td colspan="2">Channel 1 Filter Enable; averaging filter point follows ADC_Filter<1:0>
0 : Disable; 1 : Enable</td></tr>
<tr><td>0</td><td>R/W</td><td>CH0_FilterEn</td><td>0</td><td colspan="2">Channel 0 Filter Enable; averaging filter point follows ADC_Filter<1:0>
0 : Disable; 1 : Enable</td></tr>
</table>

Table 53. ADC_DATA_CH0 (0x53)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH0</td><td>Data for channel 0</td><td>0x53</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH0_DATA</td><td>0x00h</td><td colspan="2">Channel 0 (V_{BUS} Voltage) Data
$V_{BUS\_HV\_RANGE}$ = 0
0x00h = 2.7V
.
.
0xFFh = 6.3V (step = 14mV)

$V_{BUS\_HV\_RANGE}$ = 1
0x00h = 6.3V
.
.
0xFFh = 14.7V (step = 33mV)</td></tr>
</table>

Table 54. ADC_DATA_CH1 (0x54)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH1</td><td>Data for channel 1</td><td>0x54</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH1_DATA</td><td>0x00h</td><td colspan="2">Channel 1 (V_{BUS} Current) Data
0x00h = 0.0A
.
.
0xFFh = 4.1A (step = 16mA)</td></tr>
</table>

Table 55. ADC_DATA_CH2 (0x55)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH2</td><td>Data for channel 2</td><td>0x55</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH2_DATA</td><td>0x00h</td><td colspan="2">Channel 2 (V_{BATT} Voltage) Data
0x00h = 2.1A
.
.
0xFFh = 4.9V (step = 11mV)</td></tr>
</table>

Table 56. ADC_DATA_CH3 (0x56)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH3</td><td>Data for channel 3</td><td>0x56</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH3_DATA</td><td>0x00h</td><td colspan="2">Channel 3 (V_{BATT} Current) Data
0x00h = 0.0A
.
.
0xFFh = 3.1A (step = 12mA)</td></tr>
</table>

Table 57. ADC_DATA_CH4 (0x57)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH4</td><td>Data for channel 4</td><td>0x57</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH4_DATA</td><td>0x00h</td><td colspan="2">Channel 4 (V_{BATT} I_{REXT} Current) Data (2's Complement)
0x00h = 0A
.
0x7Fh = +10A
0x80h = -10A
.
0xFFh = 0A (step = 78.125mA)</td></tr>
</table>

Table 58. ADC_DATA_CH5 (0x58)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH5</td><td>Data for channel 5</td><td>0x58</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH5_DATA</td><td>0x00h</td><td colspan="2">Channel 5 (Temperature Sensing) Data (in terms of (THMV/THMB))
0x00h = 20%
.
0xFFh = 80% (step = 0.24%)</td></tr>
</table>

Table 59. ADC_DATA_CH6 (0x59)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH6</td><td>Data for channel 6</td><td>0x59</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH6_DATA</td><td>0x00h</td><td colspan="2">Channel 6 (Reserved) Data
0x00h = 0.6V
.
.
0xFFh = 1.4V (step = 3.1mV)
Note: Channel connected to VCM signal internally.</td></tr>
</table>

Table 60. ADC_DATA_CH7 (0x5A)

<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_DATA_CH7</td><td>Data for channel 7</td><td>0x5A</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
</table>

Table 60. ADC_DATA_CH7 (0x5A) (continued)

7:0	R	CH7_DATA	0x00h	Channel 7 (Test) Data 0x00h = 0.6V . . 0xFFh = 1.4V (step = 3.1mV) **Note:** Channel connected to TEST1 during test mode.

Table 61. ADC_OFFSET_CH1 (0x5B)

NAME		FUNCTION	ADDR	TYPE	RESET
ADC_OFFSET_CH1		Offset raw data for channel 1	0x5B	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:0	R	CH1_OFFSET	0x00h	Channel 1 (V_{BUS} Current) Offset Calibration. CH1_OFFSET<7:0> is the readback (raw) code. It can be converted to offset code by the following formula: Readback Code: Ideal Code = Offset Code, Ideal Code = 0x80h 0x00h to 0x80h = -128d : -2.048A . 0x7Eh to 0x80h = -2d : -0.032A 0x7Fh to 0x80h = -1d : -0.016A 0x80h to 0x80h = 0d : 0A 0x81h to 0x80h = 1d : 0.016A 0x82h to 0x80h = 2d : 0.032A . 0xFFh to 0x80h = 127d : 2.032A (step = 16mA)	

Table 62. ADC_OFFSET_CH3 (0x5C)

NAME		FUNCTION	ADDR	TYPE	RESET
ADC_OFFSET_CH3		Offset raw data for channel 3	0x5C	O	0x00
BIT	**MODE**	**NAME**	**RESET**	**DESCRIPTION**	
7:0	R	CH3_OFFSET	0x00h	Channel 3 (V_{BAT} Current) Offset Calibration. CH3_OFFSET<7:0> is the readback (raw) code. It can be converted to offset code by the following formula: Readback Code: Ideal Code = Offset Code, Ideal Code = 0x80h 0x00h to 0x80h = -128d : -1.536A . 0x7Eh to 0x80h = -2d : -0.024A 0x7Fh to 0x80h = -1d : -0.012A 0x80h to 0x80h = 0d : 0A 0x81h to 0x80h = 1d : 0.012A 0x82h to 0x80h = 2d : 0.024A . 0xFFh to 0x80h = 127d : 1.524A (step = 12mA)	

Table 63. ADC_OFFSET_CH4 (0X5D)

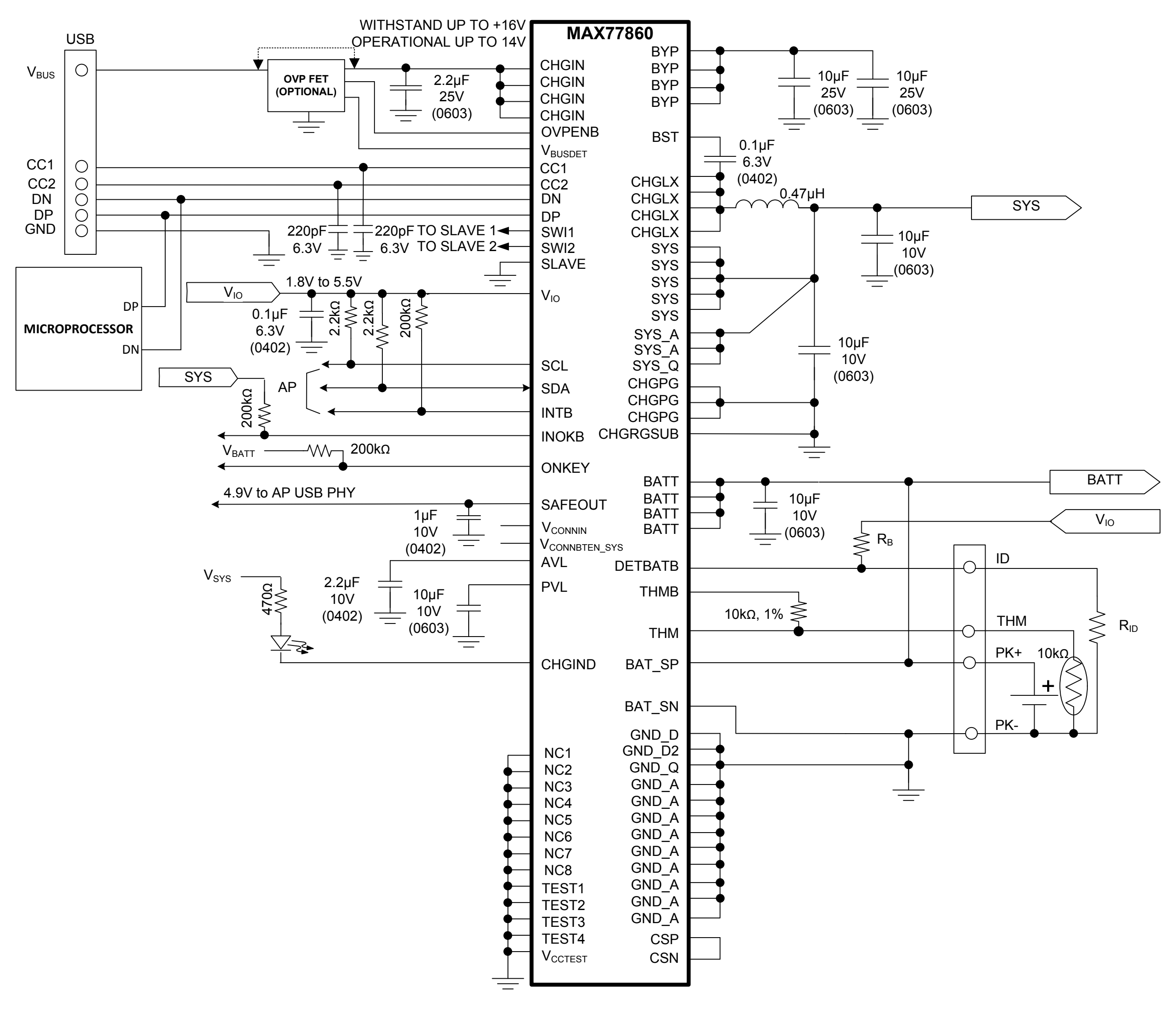
<table>
<tr><th colspan="2">NAME</th><th>FUNCTION</th><th>ADDR</th><th>TYPE</th><th>RESET</th></tr>
<tr><td colspan="2">ADC_OFFSET_CH4</td><td>Offset raw data for channel 4</td><td>0x5D</td><td>O</td><td>0x00</td></tr>
<tr><th>BIT</th><th>MODE</th><th>NAME</th><th>RESET</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:0</td><td>R</td><td>CH4_OFFSET</td><td>0x00h</td><td colspan="2">Channel 4 (V_{BATT} Current) Offset Calibration. CH4_OFFSET<7:0> is the readback (raw) code. It can be converted to offset code by the following formula:

Readback Code: Ideal Code = Offset Code, Ideal Code = 0x80h

0x00h – 0x80h = 0x00h = -128d : -10A
.
0x7Eh – 0x80h = 0x82h = -2d : -0.15625A
0x7Fh – 0x80h = 0x81h = -1d : -0.078125A
0x80h – 0x80h = 0x80h = 0d : 0A
0x81h – 0x80h = 0x7Fh = 1d : 0.078125A
0xh – 0x80h = 0x7Eh = 2d : 0.15625A
.
0x00h – 0x80h = 0x01h = 127d : 9.921875A

(step = 78.125mA)</td></tr>
</table>

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77860EWG+	-40°C to +85°C	81 WLP
MAX77860EWG+T	-40°C to +85°C	81 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/19	Initial release	—
0.1		Updated cable resistance from “300mΩ to 3Ω” to “300mΩ and 3Ω” in the Input-Voltage Regulation Loop and Adaptive Input Current Limit (AICL) section	32
1	2/19	Updated SYS Input Range section in the Electrical Characteristics table, added Pin Configuration and Pin Description table	9, 28
2	6/19	Updated *Functional Block Diagram* and *Typical Application Circuits*, corrected minor errors	1, 32, 33, 71, 87