

General Description

The MAX8830 light management IC integrates a 400mA (guaranteed) PWM DC-DC step-up converter, a 320mA white LED camera flash current sink, and four programmable LED current sinks. The internal 1MHz step-up converter features an internal switching MOSFET and synchronous rectifier to improve efficiency and minimize external component count. The camera flash output current and maximum timer is programmable through I2C. Each LED current is individually regulated to a programmable level (from off to 10mA in 32 steps) and is completely independent of each other.

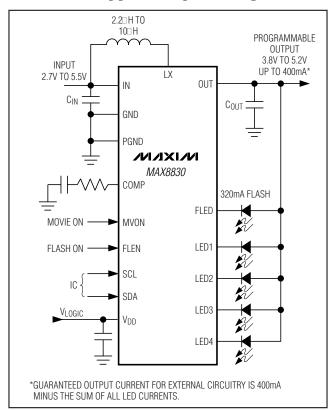
An I²C interface controls individual on/off of all outputs, step-up output voltage setting, movie/flash current, flash timer duration settings, and individual LED current sink settings.

The MAX8830 is available in a 16-bump UCSP™ package (2.5mm x 2.5mm).

Applications

Cell Phones and Smartphones PDAs and MP3 Players

Typical Operating Circuit



Features

- ♦ Step-Up DC-DC Converter
 - 400mA Guaranteed Output Current Over 90% Efficiency **On-Chip FET and Synchronous Rectifier Fixed 1MHz PWM Switching** Small 2.2µH to 10µH Inductor I²C-Programmable V_{OUT} (3.8V to 5.2V and Off in 16 Steps)
- ♦ Flash LED Current Sink

I²C-Programmable Flash Output Current (Off to 320mA in 32 Steps)

I²C-Programmable Flash Maximum Timer (0.5s, 1.0s, 1.5s, or 2.0s)

I²C-Programmable Movie Output Current (Off to 160mA in 16 Steps)

Movie Enabled by I²C or Logic Input Flash Enabled by Logic Input

Low Dropout (75mV typ)

♦ Four LED Current Sinks

Individually I²C-Programmable Output Current Off to 10mA in 32 Steps

Low LED Sink Current Dropout Voltage (30mV typ)

♦ I²C Interface

Write Address (0x94), Read Address (0x95) Individual On/Off and LED Current Settings Simple Register Mapping

- ♦ < 1µA Shutdown Current
- ♦ Open/Short LED Detection
- **♦ Thermal-Shutdown Protection**
- ♦ 16-Bump, 2.5mm x 2.5mm UCSP Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8830EWE+T	-40°C to +85°C	16 UCSP (2.5mm x 2.5mm)

⁺Denotes a lead-free package.

Pin Configuration appears at the end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

IN, OUT to GND	0.3V to +6.0V
IN, OUT to GND (maximum of 1µs)	+7.0V
V _{DD} to GND	0.3V to +4.0V
SCL, SDA, MVON, FLEN to GND	0.3V to V _{DD} + 0.3V
COMP, FLED, LED_ to GND	0.3V to V _{OUT} + 0.3V
PGND to GND	0.3V to +0.3V
Continuous I _L X Current	1A _{RMS}

Continuous Power Dissipation (T _A = +70°C	C)
16-Bump 2.5mm x 2.5mm UCSP	
(derate 105.7mW/°C above +70°C)	750mW
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	
Bump Temperature* (soldering)	+235°C

*This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = 3.6V, V_{GND} = V_{PGND} = 0V, V_{DD} = 3.0V, T_{A} = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_{A} = +25^{\circ}C$.) (Note 1)

PARAMETER	DESCR	MIN	TYP	MAX	UNITS		
IN Operating Voltage			2.7		5.5	V	
V _{DD} Operating Range			1.7		3.6	V	
V _{DD} Undervoltage Lockout (UVLO) Threshold	V _{DD} falling		1.35	1.5	1.65	V	
V _{DD} UVLO Hysteresis				50		mV	
IN UVLO Threshold	V _{IN} rising		2.25	2.45	2.65	V	
IN UVLO Hysteresis				50		mV	
Van Standby Cupply Current	SCL = SDA = V _{DD} ,	$T_A = +25^{\circ}C$		3	10		
V _{DD} Standby Supply Current	I ² C ready	T _A = +85°C		4		μΑ	
IN Ctop dlay Cypaly Cypropt	SCL = SDA = V _{DD} ,	$T_A = +25^{\circ}C$		5	15		
IN Standby Supply Current	I ² C ready	T _A = +85°C		5		μA	
INI Charteleura Caraba Caraba	All outputs off,	T _A = +25°C		0.1	5	μΑ	
IN Shutdown Supply Current	$V_{DD} = 0$	T _A = +85°C		1			
Thermal-Shutdown Hysteresis				20		°C	
Thermal-Shutdown				+160		°C	
LOGIC AND I ² C INTERFACE							
		MVON, FLEN	1.6				
Logic Input-High Voltage	$V_{DD} = 1.7V \text{ to } 3.6V$	SCL, SDA	0.7 x V _{DD}			V	
		MVON, FLEN			0.4		
Logic Input-Low Voltage	$V_{DD} = 1.7V \text{ to } 3.6V$	SCL, SDA			0.3 x V _{DD}	V	
Landa languat Ourmanat	\\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T _A = +25°C	-1	0.01	+1		
Logic Input Current	$V_{IL} = 0V \text{ or } V_{IH} = 3.6V$	T _A = +85°C		0.1		μΑ	
SDA Output Low Voltage	I _{SDA} = 3mA	•		0.03	0.4	V	
I ² C Clock Frequency					400	kHz	
Bus-Free Time Between START and STOP	tBUF		1.3			μs	
Hold Time Repeated START Condition	thd_sta		0.6	0.1		μs	
SCL Low Period	t _{LOW}		1.3	0.2		μs	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN}=3.6V, V_{GND}=V_{PGND}=0V, V_{DD}=3.0V, T_{A}=-40^{\circ}C \ to \ +85^{\circ}C, unless \ otherwise \ noted. \ Typical \ values \ are \ at \ T_{A}=+25^{\circ}C.) \ (Note \ 1)$

PARAMETER	DESCR	IPTION	MIN	TYP	MAX	UNITS
SCL High Period	thigh		0.6	0.2		μs
Setup Time Repeated START Condition	tsu_sta		0.6	0.1		μs
SDA Hold Time	thd_dat	thd_dat				μs
SDA Setup Time	tsu_dat		100	50		ns
Setup Time for STOP Condition	tsu_sto		0.6	0.1		μs
STEP-UP DC-DC CONVERTER						
IN Supply Current	1MHz switching, Vout =	5V (see Note 4)		5.5	10.0	mA
OUT Voltage Range	100mV steps		3.8		5.2	V
OLIT Voltage Appurpou	100m A	$T_A = +25^{\circ}C$	-1.5	±0.3	+1.5	0/
OUT Voltage Accuracy	IOUT = IOUTIA	$I_{OUT} = 100 \text{mA}$ $T_{A} = +85 ^{\circ}\text{C}$			+3	%
Line Regulation	$V_{IN} = 2.7V \text{ to } 4.2V$			0.1		%/V
Load Regulation	$I_{OUT} = 0$ to $400mA$			0.5		%/A
Maximum OUT Current	V _{IN} ≥ 3.2V, V _{OUT} = 5.0V		400	700		mA
nFET Current Limit				2.2		А
LX nFET On-Resistance	LX to PGND, I _{LX} = 100m	ıΑ		0.1		Ω
LX pFET On-Resistance	LX to OUT, I _{LX} = 100mA			0.15		Ω
LVLookaga	Viv. E EV	T _A = +25°C		0.1	5	
LX Leakage	$V_{LX} = 5.5V$	$T_A = +85^{\circ}C$		1		μA
Operating Frequency	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		0.75	1.00	1.25	MHz
Maximum Duty Cycle			65	75		%
Minimum Duty Cycle				4	8	%
COMP Transconductance	$V_{COMP} = 1.5V$			60		μS
COMP Discharge Resistance	During shutdown or UVL	.O, from COMP to GND		180		Ω
OUT Discharge Resistance	During shutdown or UVL	.O, from OUT to IN		10		kΩ
FLED CURRENT SINK DRIVER						
IN Supply Current	Step-up off, FLED on			0.35	0.6	mA
Maximum Current Catting	Flash (enabled by FLEN)		320		m 1
Maximum Current Setting	Movie (enabled by MVO	N or I ² C)		160		mA
		T _A = +25°C	-3.0	±0.5	+3.0	
Current Accuracy	50mA setting, Movie	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-5		+5	%
Current-Regulator Dropout	50mA setting (Note 2)	1		75		mV
	$T_A = +25^{\circ}C$	Ŭ . ,			5	
FLED Leakage in Shutdown		$T_A = +85^{\circ}C$				μΑ
Flash Duration Timer Range	In 500ms steps (Note 3)				2.0	S
Open-LED Detection Threshold	FLED enabled		0.5	100	-	mV
Shorted-LED Detection Threshold	FLED enabled			V _{OUT} -		V

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = 3.6V, V_{GND} = V_{PGND} = 0V, V_{DD} = 3.0V, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	DESCR	IPTION	MIN	TYP	MAX	UNITS
LED1-LED4 CURRENT SINK DRIVER						
IN Supply Current	Step-up off, all current s	inks on		0.2	0.5	mA
Maximum Current Setting				10		mA
	1 ED 4 1 ED 4 40 4	T _A = +25°C	-2	±0.3	+2	
Current Accuracy	LED1-LED4 = 10mA setting, V _{OUT} = V _{IN}	$T_A = 0$ °C to +85°C	-5		+5	%
	setting, VOUT - VIN	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-8		+8	
	$3/32$ setting, $T_A = +25^{\circ}C$	$3/32$ setting, $T_A = +25^{\circ}C$				
Current Regulator Dropout	10mA setting (Note 2)			30	125	mV
Landana in Obserbalasson	T _A = +25°C	T _A = +25°C			5	^
Leakage in Shutdown	T _A = +85°C	T _A = +85°C				- μΑ
Open-LED Detection Threshold	LED_ enabled	LED_ enabled				mV
Shorted-LED Detection Threshold	LED_ enabled			V _{OUT} -		V

Note 1: All devices are 100% production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design.

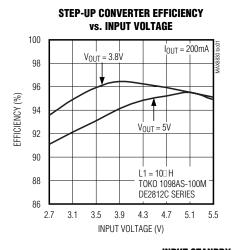
Note 2: LED current sink dropout voltage is defined as the voltage at which current drops 10% from the current level measured at 0.6V.

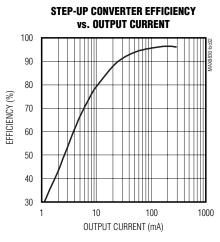
Note 3: Flash duration is from rising edge of FLEN until IFLED turns off (or returns to the movie current setting if MVON is high).

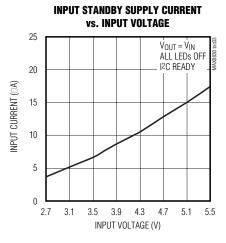
Note 4: The MAX8830 step-up converter IN supply current is tested in an open-loop configuration with no inductor. Actual closed-loop IN supply current is higher due to conduction losses in the inductor and LX nFET and pFET. These additional losses are highly dependent on inductor value and series resistance.

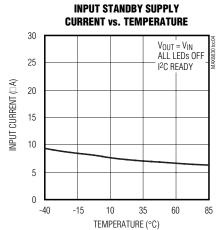
Typical Operating Characteristics

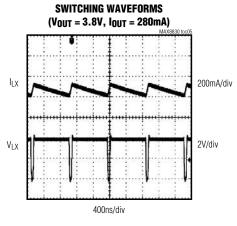
 $(V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V,$ circuit of Figure 1, $T_A = +25$ °C, unless otherwise noted.)

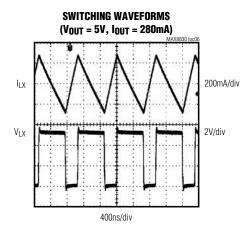


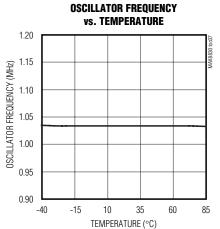






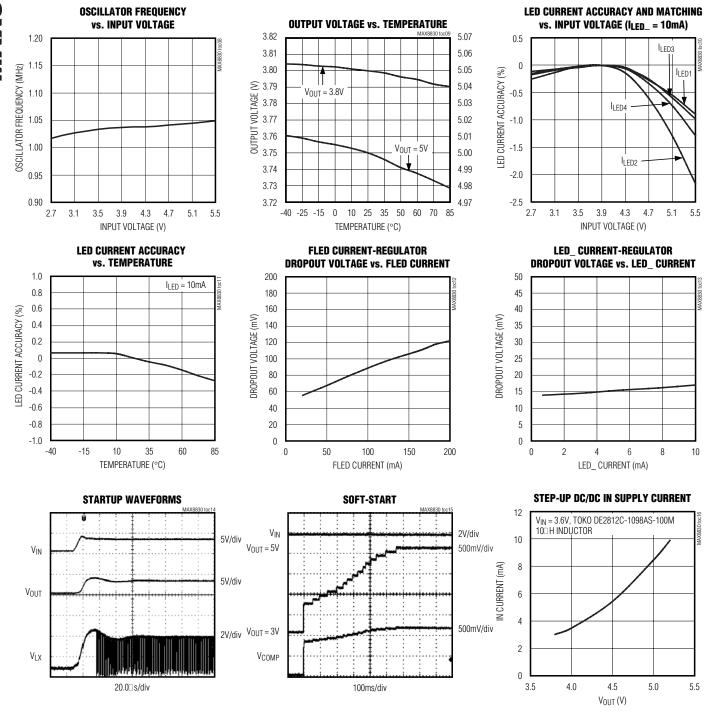






Typical Operating Characteristics (continued)

 $(V_{IN} = 3.6V, V_{OUT} = 3.8V, V_{DD} = 3.0V,$ circuit of Figure 1, $T_A = +25$ °C, unless otherwise noted.)



Pin Description

UCSP BUMP	NAME	FUNCTION
A1	FLED	Flash LED Current-Sink Regulator. Current flowing into FLED is based on the internal I ² C registers. Connect FLED to the cathode of an external flash LED or LED module. FLED is high impedance during shutdown. If unused, FLED may be shorted to ground or left unconnected.
A2	PGND	Power Ground. Connect PGND to GND and to the input capacitor ground. Connect PGND to the PCB ground plane.
А3	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drains of the internal MOSFETs. LX is high impedance in shutdown.
A4	OUT	Regulator Output. Connect OUT to the anodes of the external LEDs. OUT can also be used to supply other circuits, such as audio amplifiers. Bypass OUT to PGND with a 10µF or larger ceramic capacitor. During shutdown, V _{OUT} is one diode drop below the V _{IN} .
C1 B1 B2 D1	LED1 LED2 LED3 LED4	LED Current-Sink Regulators. Current flowing into LED_ is based on the internal I ² C registers. Connect LED_ to the cathodes of external LEDs. LED_ is high impedance during shutdown. If unused, LED_ can be shorted to ground or left unconnected.
B3	MVON	Movie On Logic Input. Connect to V _{DD} or drive with logic 1 to enable the movie mode. The FLED movie current is set in the I ² C registers. Connect to GND or drive with logic 0 to turn off the movie mode. The movie mode is also enabled through the I ² C interface.
B4	IN	Analog Supply Voltage Input. The input voltage range is 2.7V to 5.5V. Bypass IN to GND and PGND with a 10µF ceramic capacitor as close as possible to the IC. IN is high impedance during shutdown.
C2	FLEN	Flash Enable Logic Input. A transition from logic 0 to logic 1 on FLEN initiates the flash mode. The flash duration and FLED flash current are set in I ² C registers. The flash mode terminates when either FLEN transitions back to logic 0 or after the flash-duration timer expires.
C3	SCL	I ² C Clock Input. Data is read on the rising edge of SCL.
C4	COMP	Compensation Input. See the COMP Network Selection section for details.
D2	GND	Analog Ground. Connect GND to PGND and to the input capacitor ground. Connect GND to the PCB ground plane.
D3	SDA	I ² C Data Input. Data is read on the rising edge of SCL.
D4	V _{DD}	Logic Input Supply Voltage. Connect V_{DD} to the logic supply driving SCL, SDA, MVON, and FLEN. Bypass V_{DD} to GND with a 0.1 μ F ceramic capacitor. Setting V_{DD} = 0 places the part in shutdown.

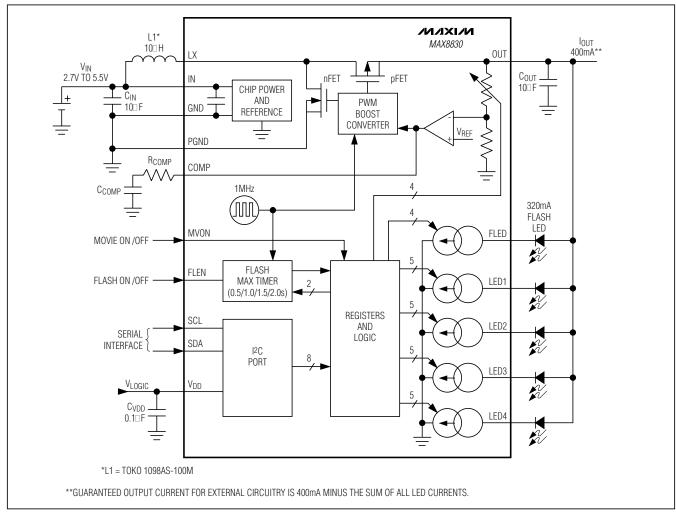


Figure 1. Block Diagram and Typical Application Circuit

Detailed Description

The MAX8830 light management IC integrates a 400mA PWM step-up DC-DC converter, a 320mA white LED camera flash current sink, and four programmable LED current sinks. An I²C interface controls individual on/off of all outputs, step-up output voltage setting, movie/ flash current and flash timer-duration settings, and individual current sink settings. Figure 1 shows the block diagram and typical application circuit.

Step-Up Converter (LX, OUT, COMP, PGND)

The MAX8830 includes a fixed-frequency, PWM step-up converter that supplies power to the LEDs and additional loads, such as audio amplifiers. The output voltage is programmable from 3.8V to 5.2V (in 100mV steps) through the I²C port. If the output voltage is not programmed, the step-up converter remains off; however, if any of the current regulators are programmed, the boost converter p-channel synchronous rectifier is turned on. The step-up converter switches an internal power MOSFET and synchronous rectifier at a constant 1MHz frequency with varying duty cycle up to 75% to maintain constant output voltage as V_{IN} and load vary. Internal circuitry prevents any unwanted subharmonic switching by forcing a minimum 4% duty cycle.

3 _______/NIXI/N

Flash Current-Sink Regulator (FLED, MVON, FLEN)

A low-dropout linear current regulator from FLED to PGND sinks current from an external flash LED cathode terminal. The FLED current is regulated to I²C-programmable levels for movie mode (up to 160mA) and flash mode (up to 320mA). The movie mode provides continuous lighting when enabled through I²C (see Table 1). The flash mode is enabled only when FLEN goes high. A flash maximum timer, programmable from 0.5s to 2.0s through I²C, limits the duration of the flash mode in case FLEN remains high. The flash mode has priority over the movie mode.

Current-Sink Regulators (LED1-LED4)

Four low-dropout linear current regulators from LED_ to GND sink current from external LED cathode terminals. The LED_ currents are individually regulated to an I²C-programmable level from off to 10mA in 32 steps, independently set for each LED_.

Undervoltage Lockout

The IC contains undervoltage lockout (UVLO) circuitry that disables the device until $V_{\rm IN}$ is greater than 2.45V (typ). Once $V_{\rm IN}$ rises above 2.45V (typ), the UVLO circuitry does not disable the IC until $V_{\rm IN}$ falls below the UVLO threshold hysteresis.

Soft-Start

The MAX8830 soft-starts by charging C_{COMP} with a $100\mu A$ current source. During this time, the internal MOSFET is switching at the minimum duty cycle. Once V_{COMP} rises above 1V, the duty cycle increases until the output voltage reaches the desired regulation level. COMP is pulled to GND with a 80Ω internal resistor during UVLO or shutdown. See the *Typical Operating Characteristics* for an example of soft-start operation.

Shutdown and Standby

The MAX8830 is in shutdown when $V_{DD} = 0$. In shutdown, supply current is reduced to $0.1\mu\text{A}$ (typ). The MAX8830 is in standby when the step-up converter and all LED outputs are turned off through I²C (and by keeping MVON and FLEN at logic 0). During this time, the I²C port remains in standby (ready) state as long as logic-high voltage is supplied to V_{DD} .

CCOMP is discharged whenever the step-up converter is turned off, allowing the device to reinitiate soft-start when it is enabled. The internal MOSFET and synchronous rectifier are also high impedance when the step-up converter is off; however, OUT is one diode drop below the input. FLED and LED_ are high impedance in shutdown, so the external LEDs are all off, but any external circuitry on OUT (such as an audio amplifier) is not disconnected, and therefore, should include its own shutdown capability.

Parallel Connection of Current-Sink Regulators

The LED current-sink regulators (FLED and LED_) can be connected in parallel in any combination to allow the use of higher current LEDs or any other desired effects. Unused current regulators may be left unconnected or shorted to ground. The LED regulators must be disabled through I²C to avoid a fault detection from an open or short.

Open/Short LED Detection

The MAX8830 includes 10 comparators to detect open or shorted LEDs on the FLED and LED1-LED4 pins. One comparator on each pin detects when the voltage falls below 100mV, indicating an open LED fault. Another comparator on each pin detects when the voltage rises above Vout - 1V, indicating a shorted LED fault. The fault-detection comparators are enabled only when the corresponding current sink is enabled (and not set to zero current). Once a fault is detected the two comparators provide a single bit output (1 = fault, 0 = no fault) corresponding to the appropriate pin. When a read command (address 0x95) is issued to the MAX8830, the status of each pin is latched into the status register (see Table 6) and subsequently written to the I²C bus by the MAX8830.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX8830. When the junction temperature exceeds +160°C, the device turns off, allowing the IC to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

I²C Serial Interface

The step-up converter OUT voltage, FLED flash current and duration, FLED movie current, and LED_ individual currents are set using the I²C serial interface. Each current level is individually programmable (including off) with a single command (see Tables 1, 2, and 3). While the flash current is set through I²C, current does not flow until the FLEN input is logic 1, as described in the Flash Current-Sink Regulator (FLED, MVON, FLEN) section. By default, the movie current is turned on when a nonzero setting is programmed through I²C. Alternately, by setting a bit in the "other" register, the movie mode current may also be gated by logic 1 at the MVON input.

The I²C serial interface consists of a serial-data line (SDA) and a serial-clock line (SCL). Standard I²C writebyte commands are used. Figure 2 shows a timing diagram for the I²C protocol. The MAX8830 is a slave-only device, relying upon a master to generate a clock signal. The master (typically a microprocessor) initiates data transfer on the bus and generates SCL to permit data transfer. A master device communicates to the MAX8830 by transmitting the proper 8-bit address (0x94) followed by the 8-bit control byte. Each 8-bit control byte consists of a command code (usually 3-bits) with the remaining bits (usually 5 bits) as data (see Table 1). Each transmit sequence is framed by a START (A) condition and a STOP (L) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

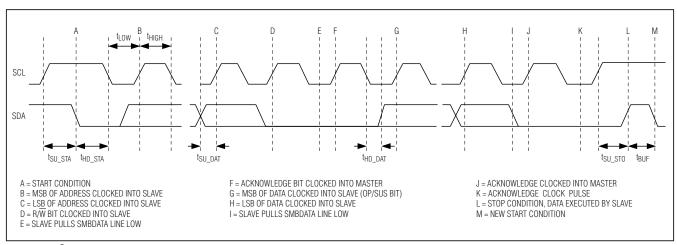


Figure 2. I²C Timing Diagram

Table 1. Control Data Byte

				SDA CON	TROL BYTE				
FUNCTION	COMMAND			DATA					
	C2	C1	C0	D4	D3	D2	D1	D0	
Step-Up OUT Voltage	0	0	0	0	3.8V to 5.2	V and off in	16 steps		
Unused	0	0	0	0	Reserved	for future use	Э		
LED1 Current	0	0	1	0	Off to 10mA in 32 steps				
LED2 Current	0	1	0	0	Off to 10m	Off to 10mA in 32 steps			
LED3 Current	0	1	1	0	Off to 10m	A in 32 step	S		
LED4 Current	1	0	0	0	Off to 10m	A in 32 step	S		
Unused	1	0	1	0	Reserved	for future use	Э		
Flash Current	1	1	0	Off to 320	mA in 32 step	os			
Movie Current	1	1	1	0	Off to 160r	nA in 16 ste	ps		
Other	1	1	1	1	0	MVON			

Note: C2 is MSB and D0 is LSB.

Table 2. Control Register Data Default Settings

				SDA CONT	ROL BYTE				
FUNCTION		COMMAND			DATA				
	C2	C1	C0	D4	D3	D2	D1	D0	
Step-Up OUT Voltage	0	0	0	0	Off (0000)				
Unused	0	0	0	0	Reserved	for future use	Э		
LED1 Current	0	0	1	0	Off (00000)				
LED2 Current	0	1	0	0	Off (00000	Off (00000)			
LED3 Current	0	1	1	0	Off (00000)			
LED4 Current	1	0	0	0	Off (00000)			
Unused	1	0	1	0	Reserved	for future use	Э		
Flash Current	1	1	0	Off (00000))				
Movie Current	1	1	1	0	Off (0000)				
Other	1	1	1	1	0	MV by I ² C (0)	0.5s (00)		

Note: C2 is MSB and D0 is LSB.

Table 3. Step-Up Voltage and LED Current Settings

	OUT \	/OLTAGE ((V) OR LED	CURREN	T (mA)				DATA		
OUT	LED1	LED2	LED3	LED4	FLASH	MOVIE	D4	D3	D2	D1	D0
OFF	OFF	OFF	OFF	OFF	OFF	OFF	0	0	0	0	0
3.8	0.63	0.63	0.63	0.63	20	20	0	0	0	0	1
3.9	0.94	0.94	0.94	0.94	30	30	0	0	0	1	0
4.0	1.25	1.25	1.25	1.25	40	40	0	0	0	1	1
4.1	1.56	1.56	1.56	1.56	50	50	0	0	1	0	0
4.2	1.88	1.88	1.88	1.88	60	60	0	0	1	0	1
4.3	2.19	2.19	2.19	2.19	70	70	0	0	1	1	0
4.4	2.50	2.50	2.50	2.50	80	80	0	0	1	1	1
4.5	2.81	2.81	2.81	2.81	90	90	0	1	0	0	0
4.6	3.13	3.13	3.13	3.13	100	100	0	1	0	0	1
4.7	3.44	3.44	3.44	3.44	110	110	0	1	0	1	0
4.8	3.75	3.75	3.75	3.75	120	120	0	1	0	1	1
4.9	4.06	4.06	4.06	4.06	130	130	0	1	1	0	0
5.0	4.38	4.38	4.38	4.38	140	140	0	1	1	0	1
5.1	4.69	4.69	4.69	4.69	150	150	0	1	1	1	0
5.2	5.00	5.00	5.00	5.00	160	160	0	1	1	1	1
	5.31	5.31	5.31	5.31	170		1	0	0	0	0
	5.63	5.63	5.63	5.63	180		1	0	0	0	1
	5.94	5.94	5.94	5.94	190		1	0	0	1	0
	6.25	6.25	6.25	6.25	200		1	0	0	1	1
	6.56	6.56	6.56	6.56	210		1	0	1	0	0
	6.88	6.88	6.88	6.88	220		1	0	1	0	1
	7.19	7.19	7.19	7.19	230		1	0	1	1	0
	7.50	7.50	7.50	7.50	240		1	0	1	1	1
	7.81	7.81	7.81	7.81	250		1	1	0	0	0
	8.13	8.13	8.13	8.13	260		1	1	0	0	1
	8.44	8.44	8.44	8.44	270		1	1	0	1	0
	8.75	8.75	8.75	8.75	280		1	1	0	1	1
	9.06	9.06	9.06	9.06	290		1	1	1	0	0
	9.38	9.38	9.38	9.38	300		1	1	1	0	1
	9.69	9.69	9.69	9.69	310		1	1	1	1	0
	10.00	10.00	10.00	10.00	320		1	1	1	1	1

Note: Defaults in bold italics.

Table 4 lists the MVON control settings; Table 5 lists flash duration settings. Table 6 shows the read (0x95) status register.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note: UCSP-A Wafer-Level Chip-Scale Package.

Table 4. MVON Control Setting

	SDA CONTROL BYTE									
FUNCTION	COMMAND			DATA						
	C2	C1	C0	D4	D3	D2	D1	D0		
Movie Enabled Through I ² C	1	1	1	1	Χ	0	Χ	Х		
Movie Enabled Through MVON Pin	1	1	1	1	Χ	1	Χ	Χ		

Note: Defaults in bold italics.

Table 5. Flash Duration Settings

	SDA CONTROL BYTE									
FUNCTION	COMMAND			DATA						
	C2	C1	C0	D4	D3	D2	D1	D0		
0.5s Flash	1	1	1	1	Χ	Χ	0	0		
1.0s Flash	1	1	1	1	Χ	Χ	0	1		
1.5s Flash	1	1	1	1	Χ	Χ	1	0		
2.0s Flash	1	1	1	1	Χ	Χ	1	1		

Note: Defaults in bold italics.

Table 6. Read (0x95) Status Register

				SDA REA	AD BYTE			
FUNCTION	DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Fault Status	Χ	Χ	Χ	FLED	LED4	LED3	LED2	LED1

Note: 1 = fault, 0 = no fault

Table 7. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	DCR (mΩ)	I _{SAT} (A)	DIMENSIONS (L _{TYP} x W _{TYP} x H _{MAX} = VOLUME)
Cooper (Coiltronics)	SD3114	2.2	110	1.74	$3.0 \times 3.0 \times 1.45 = 13 \text{mm}^3$
FDK	MIPF2520	2.2	80	1.3A	$2.5 \times 2.0 \times 1.0 = 5 \text{mm}^3$
FUK	MIPW3226	2.2	100	1.1	$3.2 \times 2.6 \times 1.0 = 8 \text{mm}^3$
TDK	VLF3012AT	2.2 10	88 360	1.0 0.49	2.8 x 2.6 x 1.2 = 9mm ³
токо	DE2812C	2.7	75	1.8	$3.0 \times 3.2 \times 1.2 = 12$ mm ³
TONO	DE2612C	10	325	0.78	$3.0 \times 3.2 \times 1.2 = 12$ mm ³

Inductor Selection

The MAX8830 is designed to use a 2.2µH to 10µH inductor. To prevent core saturation, ensure that the inductor-saturation current rating exceeds the peak inductor current for the application. Calculate the worst-case peak inductor current with the following formula:

$$I_{PEAK} = \frac{V_{OUT} \ \Box \ I_{OUT(MAX)}}{0.9 \ \Box \ V_{IN(MIN)}} + \frac{V_{IN(MIN)} \ \Box \ 0.5 \Box s}{2 \ \Box \ L}$$

Table 7 provides a list of suggested inductors.

Capacitor Selection

Bypass the input to GND and PGND using a ceramic capacitor. A ceramic capacitor with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over a wide temperature range. Place the capacitor as close as possible to the IC. The recommended minimum value for the input capacitor is $10\mu F$; however, larger value capacitors can be used to reduce input ripple at the expense of size and higher cost.

The output capacitance required depends on the maximum output current. A 10µF ceramic capacitor works well in most situations, but a 4.7µF capacitor is acceptable for lower load currents.

COMP Network Selection

The step-up converter is compensated for stability through an external compensation network from COMP to GND. See Table 8 for recommended compensation components.

Table 8. Suggested Compensation Networks

	R _{COMP} (kΩ)	C _{COMP} (pF)
2.2µH Inductor (Dynamic Loads)	4.3	2200
4.7µH Inductor (Dynamic Loads)	3	4700
10µH Inductor (Dynamic Loads)	3	6800
Only LED Loads (2.2µH to 10µH)	0 (short)	22000

PCB Layout

Due to fast switching waveforms and high-current paths, careful PCB layout is required. Connect GND and PGND directly to the ground plane. The IN bypass capacitor should be placed as close as possible to the IC. RCOMP and CCOMP should be connected between COMP and GND as close as possible to the IC. Minimize trace lengths between the IC and the inductor, the input capacitor, and the output capacitor; keep these traces short, direct, and wide. The ground connections of CIN and COUT should be as close together as possible and connected to PGND. The traces from the input to the inductor and from the output capacitor to the LEDs may be longer. A sample layout is available in the MAX8830 evaluation kit.

Pin Configuration

NAX8830						
	1	2	3	4		
А	+ O FLED	PGND	O LX	O OUT		
В	C LED2	C LED3	MVON	O IN		
С	O LED1	FLEN	SCL	COMP		
D	C LED4	GND	SDA	$\bigvee_{V_{DD}}$		
'	(SP x 2.5mm))		

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 UCSP	W162A2-1	<u>21-0202</u>

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/07	Initial release	_
1	6/08	Updated several electrical characteristics	1–4, 6, 8, 9, 11, 12, 15

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