

## 60 V, 60 mΩ single high-side switches



## Features

- 8 V to 60 V operating voltage range
- Minimum output current limitation: 0.7 A (IPS161H) or 2.5 A (IPS160H)
- Fast demagnetization of inductive load
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Ground disconnection protection
- V<sub>CC</sub> disconnection protection
- Thermal shutdown protection
- Undervoltage lock-out
- Diagnostic signalization for: open load in off-state, cut-off and junction thermal shutdown
- Designed to meet IEC 61131-2
- PowerSSO12 package

## Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Domotics
- Generic power supply switch

## Description

The IPS160H ( $I_{OUT} < 2.5$  A) and IPS161H ( $I_{OUT} < 0.7$  A) are monolithic devices which can drive capacitive, resistive or inductive loads with one side connected to ground.

The 60 V operating range and  $R_{on} = 60$  mΩ, combined with the extended diagnostic (Open Load, Over Load, Overtemperature) make the IC suitable for applications implementing the proper architectures to address higher SIL levels.

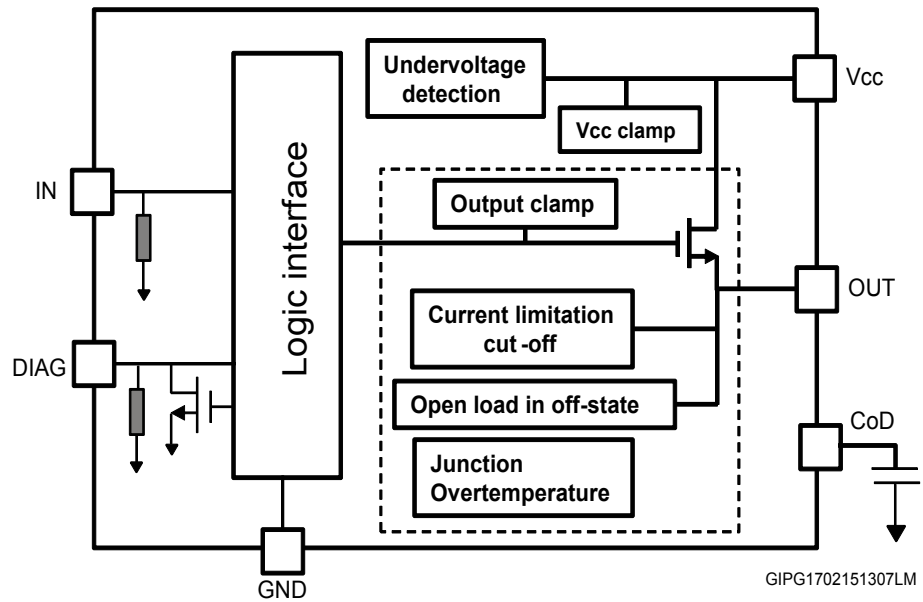
The built-in overload and thermal shutdown protections guarantee the ICs, the application and the load against electrical and thermal overstress. Furthermore, in order to minimize the power dissipation when the output is shorted, a low-dissipative short-circuit protection (cut-off) is implemented to limit the output average current value and consequent device overheating. Cut-off delay time can be set by soldering an external capacitor or disabled by a resistor on pin 4 (CoD).

The DIAG common diagnostic open drain pin reports the open load in off-state, cutoff (overload) and thermal shutdown.

Product status		
	IPS160H	
	IPS161H	
Product label		
		
Product summary		
Order code	IPS160H	IPS160HTR
	IPS161H	IPS161HTR
Package	PowerSSO12	
Packing	Tube	Tape and reel

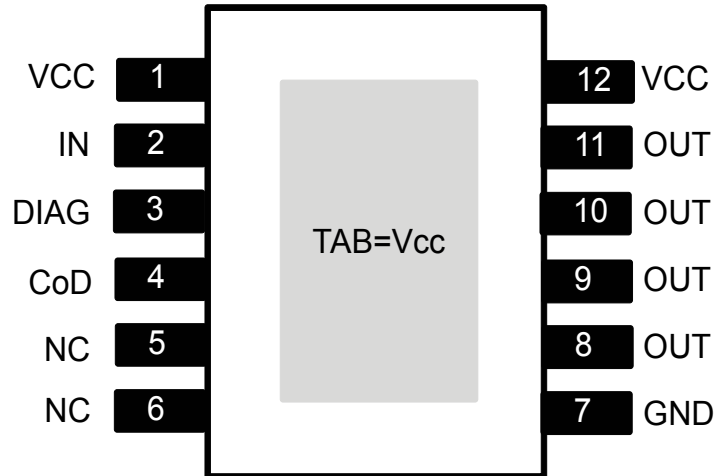
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

Figure 2. Pin connection (top view)



GIPG1702151321LM

Table 1. Pin configuration

Number	Name	Function	Type
1, 12, TAB	VCC	Device supply voltage	Supply
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin both for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Cut-off delay pin, cannot be left floating. Connected to GND by 1 kΩ resistor to disable the cut-off function. Connect to a C <sub>CoD</sub> capacitor to set the cut-off delay see <a href="#">Table 8. Protection and diagnostic</a>	Input
5, 6	NC	Not connected	
7	GND	Device ground	Ground
8, 9, 10, 11	OUT	Channel power stage output	Output

### 2.1 IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see [Table 7. Logic inputs](#).

### 2.2 OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

### 2.3 DIAG

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

## 2.4 CoD

This pin cannot be left floating and can be used to program the cut-off delay time  $t_{\text{coff}}$ , see [Table 8. Protection and diagnostic](#) through an external capacitor ( $C_{\text{CoD}}$ ). The cut-off function can be completely disabled connecting the CoD pin to GND through 1 k $\Omega$  resistor: in this condition the output channel remains in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered.

## 2.5 GND

IC ground.

## 2.6 VCC

IC supply voltage.

### 3 Reverse polarity

#### Reverse polarity

The IC can be protected against reverse polarity using two different solutions:

1. Placing a resistor  $R_{GND}$  between IC GND pin and load connection point to GND ( $R_{GND} > V_{CC}/I_{CC}$ , see Table 1. Absolute maximum rating). Note that power dissipated by  $R_{GND}$  during reverse polarity condition is  $V_{CC}^2/R_{GND}$ .
2. Placing a diode in parallel to  $R_{GND}$

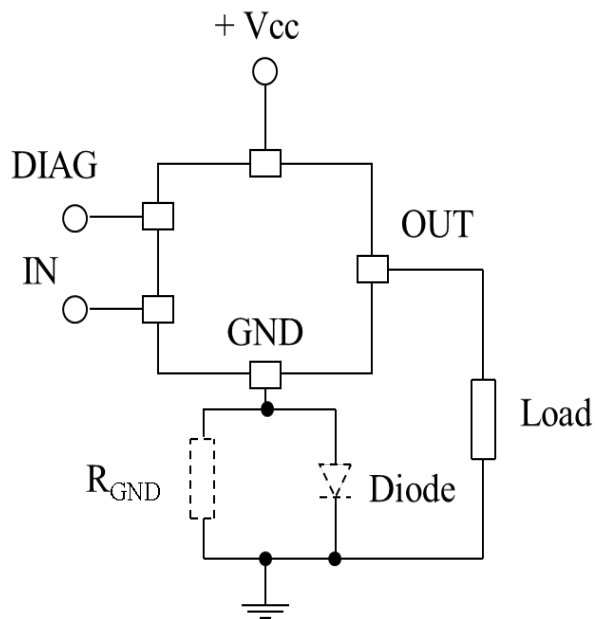
The diode must be selected such that its  $V_{RRM} > |V_{CC}|$  and power dissipation capability is higher than  $V_F \cdot I_S$  (see Table 1).

In normal operation (no reverse polarity), there is a voltage drop ( $\Delta V$ ) between GND of the device and GND of the module.

Using option 1,  $\Delta V = R_{GND} \cdot I_{CC}$ .

Using option 2,  $\Delta V = V_F @ (I_S)$ .

**Figure 3. Reverse polarity protection schematic**



## 4 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	-0.3 to 65	V
$V_{OUT}$	Output channel voltage	$V_{CC}-V_{clamp}$ to $V_{CC}+0.3$	V
$I_{IN}$	Input current	-10 to +10	mA
$V_{IN}$	IN voltage	$V_{CC}$	V
$V_{COD}$	Output cut-off voltage pin	5.5	V
$I_{COD}$	Input current on cut-off pin	-1 to +10	mA
$V_{DIAG}$	Fault voltage	$V_{CC}$	V
$I_{DIAG}$	Fault current	-5 to +10	mA
$I_{CC}^{(1)}$	Maximum DC reverse current flowing through the IC from GND to $V_{CC}$	-250	mA
$I_{OUT}$	Output stage current	Internally limited	A
$-I_{OUT}^{(1)}$	Maximum DC reverse current flowing through the IC from OUT to $V_{CC}$	5	
$E_{AS}^{(1)}$	Single pulse avalanche energy ( $T_{AMB} = 125\text{ °C}$ , $V_{CC} = 24\text{ V}$ , $I_{load} = 0.5\text{ A}$ )	3000	mJ
	Single pulse avalanche energy ( $T_{AMB} = 125\text{ °C}$ , $V_{CC} = 24\text{ V}$ , $I_{load} = 1.0\text{ A}$ )	1000	mJ
$P_{TOT}$	Power dissipation at $T_C = 25\text{ °C}^{(2)}$	Internally limited	W
$T_{STG}$	Storage temperature range	-55 to 150	°C
$T_J$	Junction temperature	-40 to 150	

1. Verified on STEVAL-IFP028V1 and STEVAL-IFP034V1 application board

2.  $(T_{JSD(MAX)}-T_C)/R_{th(JA)}$

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		1s	2s2p	2s2p (with 4 thermal vias)	
$R_{th(JC)}$	Thermal resistance junction-case	0.4	0.9	0.5	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	117	57	29	

**Note:**  $R_{th(JC)}$  is intended between the die and the bottom case surface measured by cold plate as per JESD51.  $R_{th(JA)}$  according JESD51-3 (1s) JESD51-5 (2s2p) and JESD51-7 (2s2p and thermal vias).

## 5 Electrical characteristics

(8 V < V<sub>CC</sub> < 60 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified)

**Table 4. Supply**

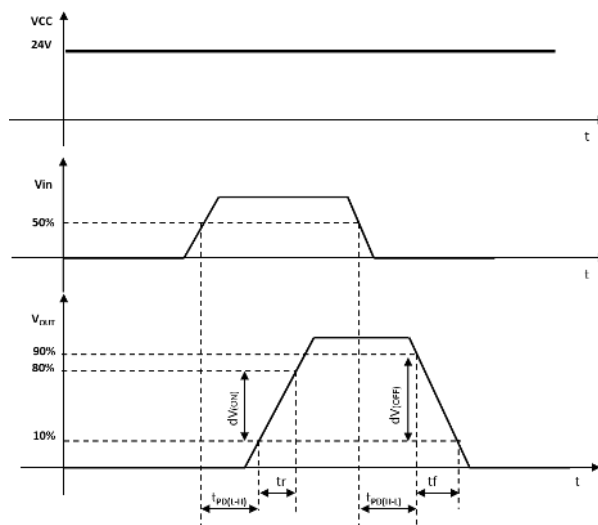
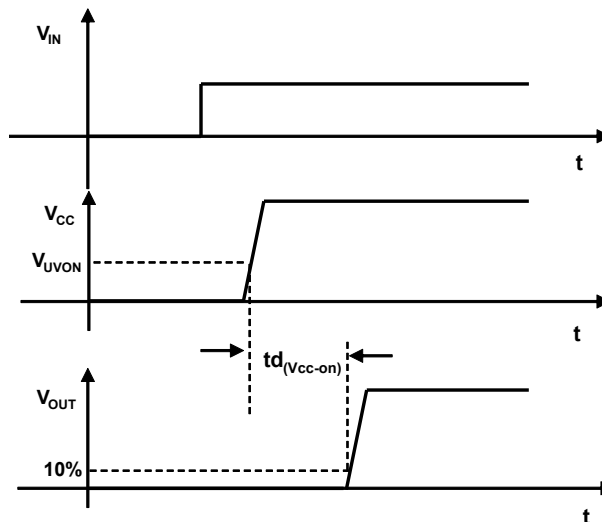
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage		V <sub>UVON</sub>		60	V
V <sub>UVON</sub>	Undervoltage on threshold		6.9		8	V
V <sub>UVOFF</sub>	Undervoltage off threshold		6.5		7.8	V
V <sub>UVH</sub>	Undervoltage hysteresis		0.15	0.5		V
I <sub>S</sub>	Supply current in off-state	V <sub>CC</sub> = 24 V		300	500	μA
		V <sub>CC</sub> = 60 V		350	600	
	Supply current in on-state	V <sub>CC</sub> = 24 V		1	1.4	mA
		V <sub>CC</sub> = 60 V		1.4	2.1	
I <sub>LGND</sub>	GND disconnection output current	V <sub>GND</sub> = V <sub>IN</sub> = V <sub>CC</sub> , V <sub>OUT</sub> = 0 V; T <sub>J</sub> = 25°C			0.5	mA
		V <sub>GND</sub> = V <sub>IN</sub> = V <sub>CC</sub> , V <sub>OUT</sub> = 0 V; T <sub>J</sub> = 125°C			0.55	

**Table 5. Output stage**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>DS(on)</sub>	On-state resistance	V <sub>CC</sub> = 24 V I <sub>OUT</sub> = 0.5 A (IPS161H), 1 A (IPS160H) @ T <sub>J</sub> = 25 °C		60	80	mΩ
		V <sub>CC</sub> = 24 V I <sub>OUT</sub> = 0.5 A (IPS161H), 1 A (IPS160H) @ T <sub>J</sub> = 125 °C			120	
V <sub>OUT(OFF)</sub>	Off-state output voltage	V <sub>IN</sub> = 0 V and I <sub>OUT</sub> = 0 A			2	V
I <sub>OUT(OFF)</sub>	Off-state output current	V <sub>CC</sub> = 24 V, V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 0 V			3	μA
		V <sub>CC</sub> = 60 V, V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 0 V			10	
I <sub>OUT(OFF-min)</sub>	Off-state output current	V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 4 V	-35		0	

**Table 6. Switching ( $V_{CC} = 24\text{ V}$ ;  $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$ ,  $R_{LOAD} = 48\text{ }\Omega$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_r$	Rise time	$I_{OUT} = 0.5\text{ A}$ , Figure 4. Timing in normal operation		10	20	$\mu\text{s}$
$t_f$	Fall time			10	20	
$t_{PD(H-L)}$	Propagation delay time off			20	35	
$t_{PD(L-H)}$	Propagation delay time on			20	35	
$t_{D(VCC-ON)}$	Power-on delay time from $V_{CC}$ rising edge	$I_{OUT} = 0.5\text{ A}$ , (see Figure 5. Propagation delay at start-up)		600	1200	

**Figure 4. Timing in normal operation**

**Figure 5. Propagation delay at start-up**




**Table 7. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input low level voltage				0.8	V
V <sub>IH</sub>	Input high level voltage		2.2			
V <sub>I(HYST)</sub>	Input hysteresis voltage			0.4		
I <sub>IN</sub>	Input current	V <sub>CC</sub> = V <sub>IN</sub> = 36 V			200	μA
		V <sub>CC</sub> = V <sub>IN</sub> = 60 V			550	

**Table 8. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>clamp</sub>	V <sub>CC</sub> active clamp	I <sub>CC</sub> = 10 mA	65.5	68.5	71.5	V
V <sub>demag</sub>	Demagnetization voltage	I <sub>OUT</sub> = 0.5 A; load = 1 mH	V <sub>CC</sub> -71.5	V <sub>CC</sub> -68.5	V <sub>CC</sub> -65.5	
V <sub>OLoff</sub>	Open load (off-state) or short to V <sub>CC</sub> detection threshold		2		4	
t <sub>BKT</sub>	Open load blanking time				200	μs
V <sub>DIAG</sub>	Voltage drop on DIAG	I <sub>DIAG</sub> = 4 mA			1	V
I <sub>DIAG</sub>	DIAG pin leakage current	V <sub>CC</sub> ≤ 36 V			110	μA
		36 V < V <sub>CC</sub> ≤ 60 V			180	
I <sub>PK</sub>	IPS161H Output current limitation activation threshold	V <sub>CC</sub> ≤ 24 V, R <sub>LOAD</sub> ≤ 10 mΩ	1.3		2.1	A
	IPS160H Output current limitation activation threshold		3.0		4.6	
I <sub>LIM</sub>	IPS161H Output current limitation		0.7		1.7	
	IPS160H Output current limitation		2.5		4.2	
t <sub>coff</sub>	Cut-off current delay time	Programmable by the external capacitor on CoD pin. Cut-off is disabled when CoD pin is connected to GND through 1 kΩ resistor. T <sub>J</sub> < T <sub>JSD</sub>	50xC <sub>CoD</sub> [nF] ± 35% <sup>(1)</sup>			μs
t <sub>res</sub>	Output stage restart delay time	T <sub>J</sub> < T <sub>JSD</sub>	32xt <sub>coff</sub> [μs] ± 40%			
T <sub>JSD</sub>	Junction temperature shutdown		150	170	190	°C
T <sub>JHYST</sub>	Junction temperature thermal hysteresis			15		

1. The formula is guaranteed in the range 10 nF ≤ C<sub>CoD</sub> ≤ 100 nF.

## 6 Output logic

Table 9. Output stage truth table

Operation	IN	OUT	DIAG
Normal	L	L	H
	H	H	H
Cut-off	L	L	L
	H	L	L
Overtemperature	L	L	L
	H	L	L
Open load	L	H (external pull-up resistor is used)	L (external pull-up resistor is used)
	H	H	H
UVLO	X	L	X
	X	L	X

## 7 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

### 7.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ( $V_{UV(off)}$ ). Normal operation restarts after  $V_{CC}$  exceeds the turn-on threshold ( $V_{UV(on)}$ ). Turn-on and turn-off thresholds are defined in [Table 4. Supply](#).

### 7.2 Overtemperature

The output stage turns off when its internal junction temperature ( $T_J$ ) exceeds the shutdown threshold  $T_{JSD}$ . Normal operation restarts when  $T_J$  comes back below the reset threshold ( $T_{JSD} - T_{JHYST}$ ), see [Table 8. Protection and diagnostic](#). The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is reported on DIAG pin.

### 7.3 Cut-off

The IC can limit the output current at the power stage by its embedded output current limitation circuit.

This circuit continuously monitor the output current and, when load is increasing, at the triggering of its activation threshold (3.8A TYP) it starts limiting to  $I_{LIM}$  limitation level (See [Protection and diagnostic](#)): while current limitation is active the IC enters an high dissipation status.

The IC implements the cut-off feature which limits the duration of the current limitation condition.

The duration of the current limitation condition ( $t_{COFF}$ ) can be set by a capacitor ( $C_{CoD}$ ) placed between CoD and GND pins. The design rule for  $C_{CoD}$  is:

$$t_{COFF[us]} \pm 35\% = 50 \times C_{CoD[nF]}$$

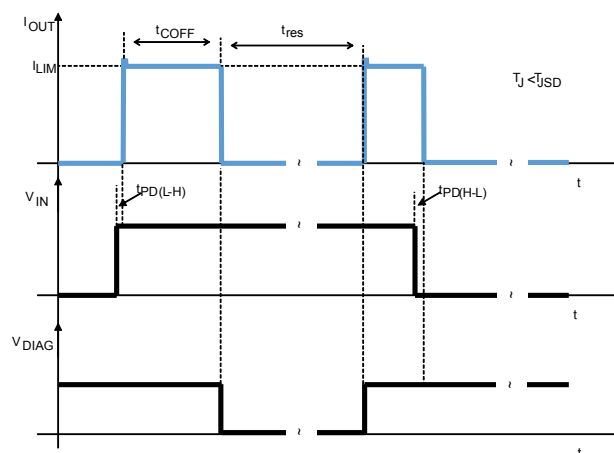
The drift of  $\pm 35\%$  is guaranteed in the range of  $10 \text{ nF} < C_{CoD} < 100 \text{ nF}$ ; lower capacitance than 10 nF can be used.

If  $I_{LIM}$  threshold is triggered, the output stage remains in the current limitation condition ( $I_{OUT} = I_{LIM}$ ) no longer than  $t_{COFF}$ . If  $t_{COFF}$  elapses, the output stage turns off and restarts after the  $t_{RES}$  restart time.

Thermal shutdown protection has higher priority than cut-off:

- IC is forced off if  $T_{JSD}$  is triggered before  $t_{COFF}$  elapses
- if  $T_{JSD}$  is triggered, IC is maintained off even after the  $t_{RES}$  has elapsed and until the  $T_J$  decreases below  $T_{JSD} - T_{JHYST}$

**Figure 6. Current limitation and cut-off**



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time  $t_{res}$ , the same behavior is reported on DIAG pin.

The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 1 k $\Omega$  resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

In case of low ambient temperature conditions ( $T_{AMB} < -20\text{ }^{\circ}\text{C}$ ) and high supply voltage ( $V_{CC} > 36\text{ V}$ ) the cut-off function needs activating in order to avoid IC permanent damages. The following table reports the suggested cut-off delay for the different operating voltage.

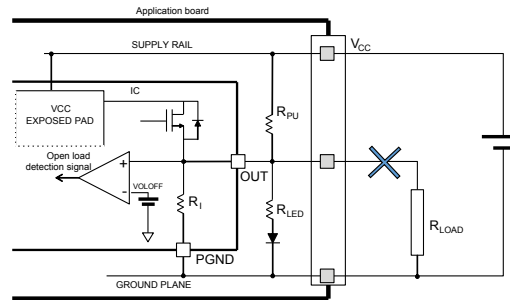
**Table 10. Minimum cut-off delay for  $T_{AMB}$  less than  $-20\text{ }^{\circ}\text{C}$**

$V_{CC}$ [V]	Cut-off delay [ $\mu\text{s}$ ]	Cut-off capacitance [nF]
36-48	100	2.2
48-60	50	1

## 7.4 Open load in off-state

The IC provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor ( $R_{PU}$ ) between OUT and VCC pins.

**Figure 7. Open load off-state**



In case of wire break and during the OFF state ( $I_N = \text{low}$ ), the output voltage  $V_{OUT}$  rises according to the partitioning between the external pull-up resistor and the internal impedance of the IC ( $130 \text{ k}\Omega < R_I < 360 \text{ k}\Omega$ ). The effect of the LED (if any) on the output pin has to be considered as well. In case of wire break and during the ON state ( $I_N = \text{high}$ ), the output voltage  $V_{OUT}$  is pulled up to  $V_{CC}$  by the low resistive integrated switch. If the load is not connected, in order to guarantee the correct open load signalization it must result:

$$V_{OUT} > V_{OLoff(max)}$$

Referring to the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times (I_{RI} + I_{LED} + I_{RL}) \quad (1)$$

therefore:

$$R_{PU} < \frac{V_{CC(min)} - V_{OLoff(max)}}{\left(\frac{V_{OLoff(max)}}{R_I(min)} + \frac{V_{OLoff(max)} - V_{LED}}{R_{LED}}\right)} \quad (2)$$

If the load is connected, in order to avoid any false signalization of the open load, it must result as follows:

$$V_{OUT} < V_{OLoff(min)}$$

By taking into account the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times \left(\frac{V_{OUT}}{R_I} + \frac{V_{OUT} - V_{LED}}{R_{LED}} + \frac{V_{OUT}}{R_L}\right) \quad (3)$$

so:

$$R_{PU} > \frac{V_{CC(max)} - V_{OLoff(min)}}{\left(\frac{V_{OLoff(min)}}{R_I(max)} + \frac{V_{OLoff(min)} - V_{LED}}{R_{LED}} + \frac{V_{OLoff(min)}}{R_L}\right)} \quad (4)$$

The fault condition is reported on the DIAG pin and the fault reset occurs when load is reconnected.

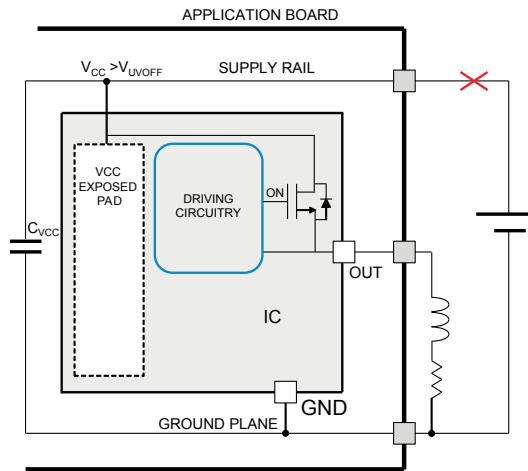
If the channel is switched on by IN pin, the fault condition is no longer detected.

When inductive load is driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when  $I_{LOAD} = 0 \text{ A}$  and the OUT pin remains floating until next turn-on. In order to avoid a fake signalization of the open load event driving inductive loads, the open load signal is masked for  $t_{BKT}$ . So, the open load is reported on the DIAG pin with a delay of  $t_{BKT}$  and if the open load event is triggered for more than  $t_{BKT}$ .

## 7.5 VCC disconnection protection

The IC is protected despite the  $V_{CC}$  disconnection event. This event is intended as the disconnection of the  $V_{CC}$  wire from the application board, see figure below. When this condition happens, the IC continues working normally until the voltage on the  $V_{CC}$  pin is  $\geq V_{UVOFF}$ . Once the  $V_{UVOFF}$  is triggered, the output channel is turned off independently on the input status. In case of inductive load, if the  $V_{CC}$  is disconnected while the output channel is still active, the IC allows the discharge of the energy still stored in the inductor through the integrated power switch.

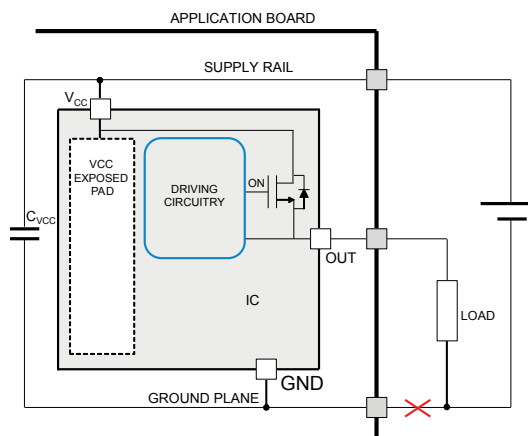
Figure 8. VCC disconnection



## 7.6 GND disconnection protection

GND disconnection is intended as the disconnection event of the application ground, see figure below. When this event happens, the IC continues working normally until the voltage between  $V_{CC}$  and GND pins of the IC results  $\geq V_{UVOFF}$ . The voltage on GND pin of the IC rises up to the supply rail voltage level. In case of GND disconnection event, a current ( $I_{LGND}$ ) flows through OUT pin. Table 7. Logic inputs reports  $I_{OUT} = I_{LGND}$  for the worst case of GND disconnection event in case of output shorted to ground.

Figure 9. GND disconnection



## 8 Active VDS clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to  $V_{\text{demag}}$ . The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at about  $V_{\text{demag}}$  until the load energy has been dissipated. The energy is dissipated both in IC internal switch and in load resistance.

Figure 10. Active clamp equivalent principle schematic

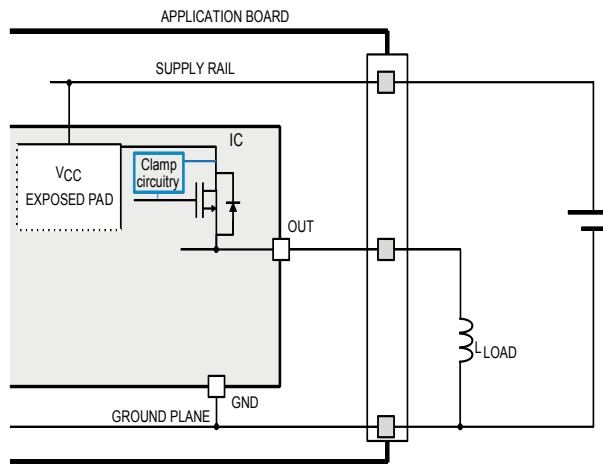
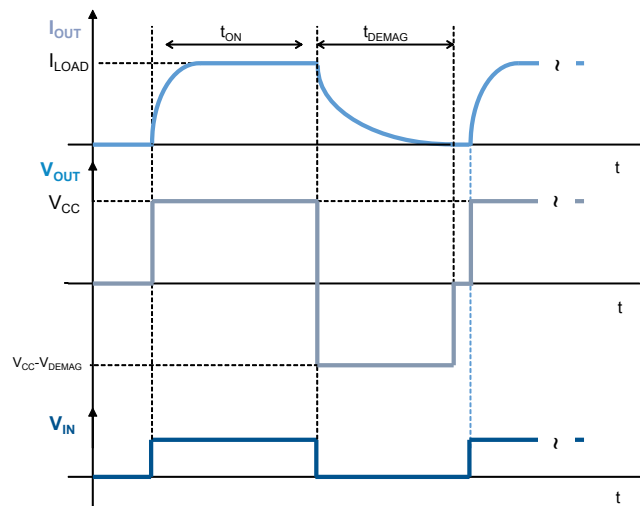
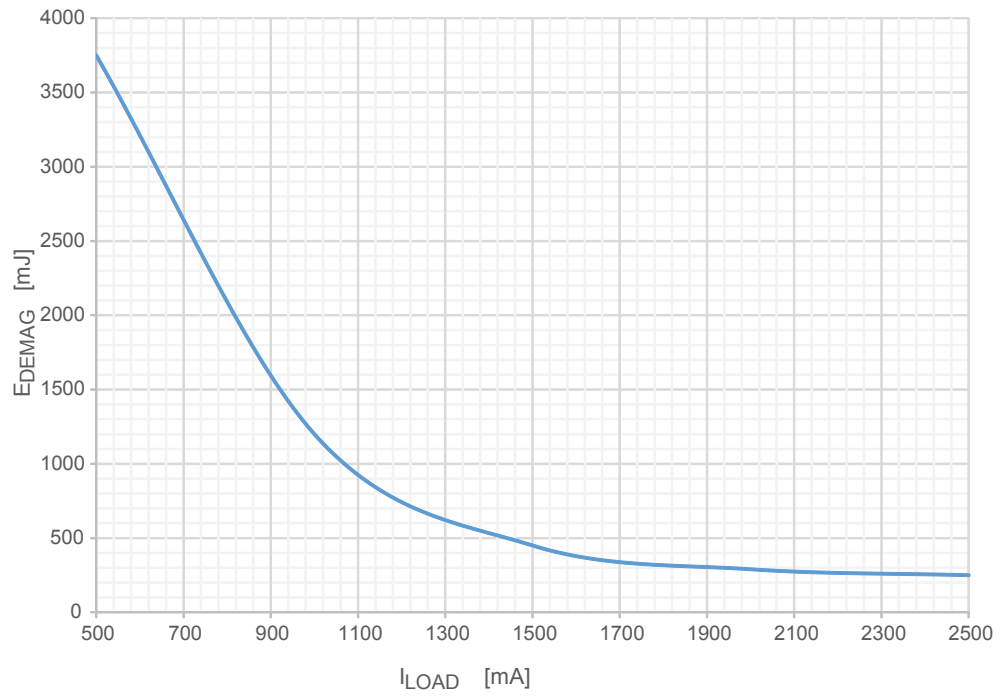


Figure 11. Fast demag waveforms



The demagnetization of inductive load causes a huge electrical and thermal stress to the IC. The curve plotted below shows the maximum demagnetization energy that the IC can support in a single demagnetization pulse with  $V_{\text{CC}} = 24 \text{ V}$  and  $T_{\text{AMB}} = 125 \text{ }^\circ\text{C}$ . If higher demagnetization energy is required then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 12. Typical demagnetization energy (single pulse) at  $V_{CC} = 24\text{ V}$  and  $T_{AMB} = 125\text{ }^{\circ}\text{C}$





## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 PowerSSO12 package information

Figure 13. PowerSSO12 package outline

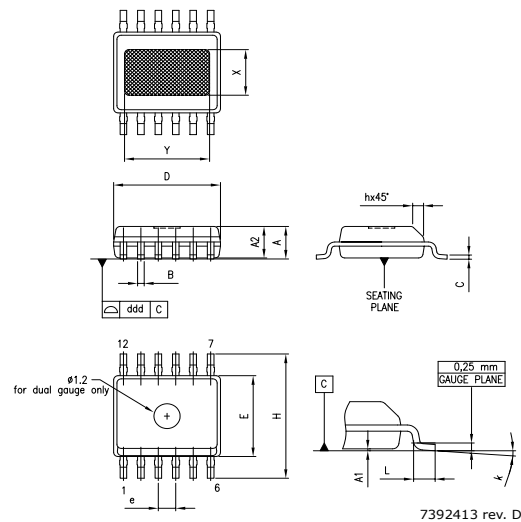


Table 11. PowerSSO12 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.55
L	0.400		1.270
k	0d		8d
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Note: Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

Figure 14. PowerSSO12 recommended footprint

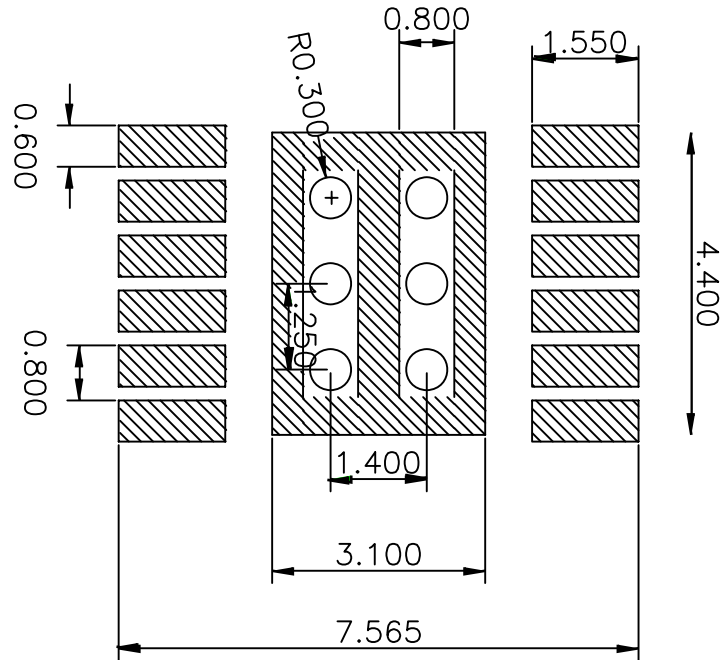


Figure 15. PowerSSO12 tape packing information [mm]

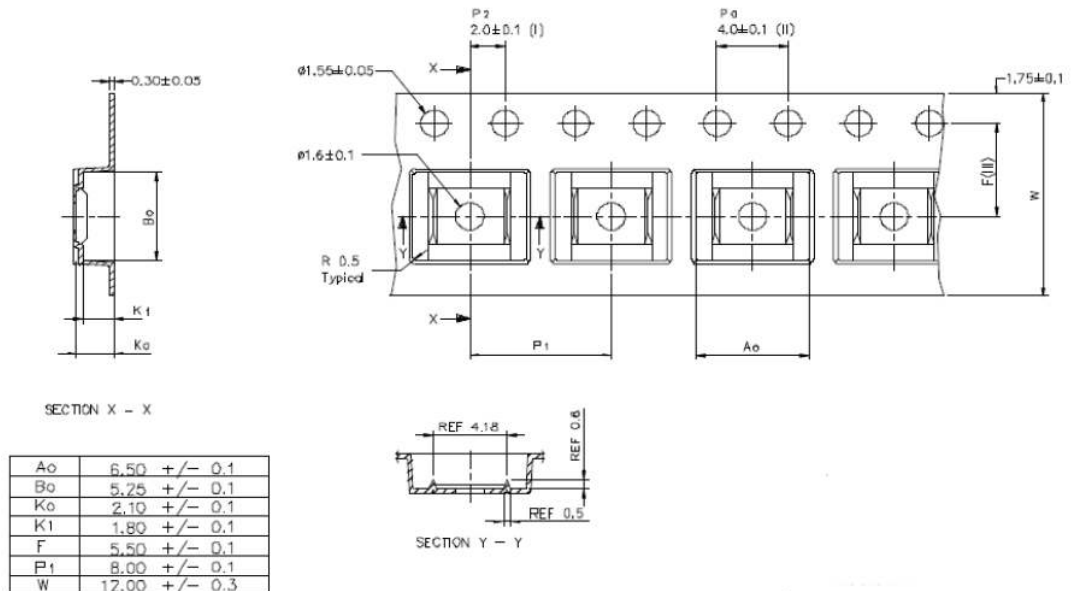
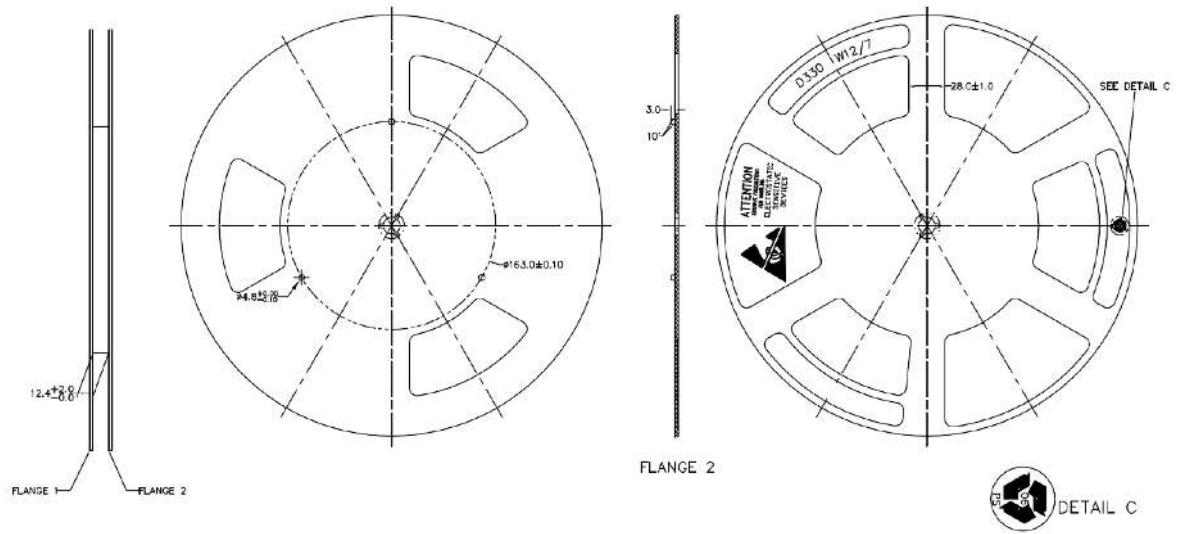


Figure 16. PowerSSO12 reel packing information [mm]



- NOTES :
1. MATERIAL : POLYSTYRENE (BLACK)
  2. ANTISTATIC COATED
  3. FLANGE WARPAGE : 3 MM MAXIMUM
  4. ALL DIMENSIONS ARE IN MM
  5. ESD - SURFACE RESISTIVITY  
-  $10^9$  TO  $10^{11}$  OHMS/SQ.
  6. GENERAL TOLERANCE :  $\pm 0.25$  MM
  7. TOTAL THICKNESS OF REEL: 18.4 MAX.
  8. MOLD NO: TX12-C7-A3

## Revision history

**Table 12. Document revision history**

Date	Revision	Changes
19-Mar-2015	1	Initial release.
04-Nov-2015	2	Minor text changes throughout the document. Added figure 7 titled "V <sub>CC</sub> disconnection", figure 10 titled: "Fast demag waveforms" and figure 11 titled "Typical demagnetization energy (single pulse) at V <sub>CC</sub> = 24 V and T <sub>AMB</sub> = 125 °C.
11-May-2016	3	Updated tables titled: "Supply", "Switching (V <sub>CC</sub> = 24 V; 125 °C > T <sub>J</sub> > -40 °C, R <sub>LOAD</sub> = 48 Ω)" and "Protection diagnostic". Changed figures titled: "t <sub>PD(L-H)</sub> and t <sub>PD(H-L)</sub> " and "Current limitation and cut-off".
20-May-2016	4	Document status promoted from preliminary to production data.
08-Mar-2018	5	Updated E <sub>AS</sub> value in <a href="#">Table 2. Absolute maximum ratings</a>
14-Dec-2018	6	Added reel packaging information in <a href="#">Section 9.1 PowerSSO12 package information</a>
02-Dec-2019	7	Updated value in <a href="#">Table 4. Supply</a> . Text change in <a href="#">Section 2.4 CoD</a> . Change to <a href="#">Figure 16</a> title.
03-Mar-2021	8	Merged IPS160H and IPS161H datasheets. Updated <a href="#">Section Description</a> and <a href="#">Section Applications</a> target.
29-Mar-2021	9	Updated I <sub>LGND</sub> max value in <a href="#">Table 4</a>
30-Jul-2021	10	Reviewed the feature list order in front page. Updated thermal data in <a href="#">Table 3</a> according to Jedec conditions
06-Dec-2022	11	Updated <a href="#">Table 6. Switching (V<sub>CC</sub> = 24 V; -40 °C &lt; T<sub>J</sub> &lt; 125 °C, R<sub>LOAD</sub> = 48 Ω)</a> : filled column Max, added t <sub>D(VCC-ON)</sub> parameter. Added figure <a href="#">Figure 5. Propagation delay at start-up</a> . Added parameter I <sub>PK</sub> (activation threshold of current activation feature) in <a href="#">table 8. Protection and diagnostic</a> . Reduced minimum and maximum values of I <sub>LIM</sub> for IPS160H in <a href="#">table 8. Protection and diagnostic</a> .

## Contents

<b>1</b>	<b>Block diagram</b> .....	<b>2</b>
<b>2</b>	<b>Pin description</b> .....	<b>3</b>
2.1	IN .....	3
2.2	OUT .....	3
2.3	DIAG .....	3
2.4	CoD .....	4
2.5	GND .....	4
2.6	VCC .....	4
<b>3</b>	<b>Reverse polarity</b> .....	<b>5</b>
<b>4</b>	<b>Absolute maximum ratings</b> .....	<b>6</b>
<b>5</b>	<b>Electrical characteristics</b> .....	<b>7</b>
<b>6</b>	<b>Output logic</b> .....	<b>10</b>
<b>7</b>	<b>Protection and diagnostic</b> .....	<b>11</b>
7.1	Undervoltage lock-out .....	11
7.2	Overtemperature .....	11
7.3	Cut-off .....	11
7.4	Open load in off-state .....	13
7.5	VCC disconnection protection .....	14
7.6	GND disconnection protection .....	14
<b>8</b>	<b>Active clamp</b> .....	<b>15</b>
<b>9</b>	<b>Package information</b> .....	<b>17</b>
9.1	PowerSSO12 package information .....	17
	<b>Revision history</b> .....	<b>20</b>

## List of tables

<b>Table 1.</b>	Pin configuration . . . . .	3
<b>Table 2.</b>	Absolute maximum ratings . . . . .	6
<b>Table 3.</b>	Thermal data . . . . .	6
<b>Table 4.</b>	Supply . . . . .	7
<b>Table 5.</b>	Output stage . . . . .	7
<b>Table 6.</b>	Switching ( $V_{CC} = 24\text{ V}$ ; $-40\text{ °C} < T_J < 125\text{ °C}$ , $R_{LOAD} = 48\ \Omega$ ) . . . . .	8
<b>Table 7.</b>	Logic inputs . . . . .	9
<b>Table 8.</b>	Protection and diagnostic . . . . .	9
<b>Table 9.</b>	Output stage truth table . . . . .	10
<b>Table 10.</b>	Minimum cut-off delay for $T_{AMB}$ less than $-20\text{ °C}$ . . . . .	12
<b>Table 11.</b>	PowerSSO12 package mechanical data . . . . .	17
<b>Table 12.</b>	Document revision history . . . . .	20

## List of figures

<b>Figure 1.</b>	Block diagram . . . . .	2
<b>Figure 2.</b>	Pin connection (top view) . . . . .	3
<b>Figure 3.</b>	Reverse polarity protection schematic . . . . .	5
<b>Figure 4.</b>	Timing in normal operation . . . . .	8
<b>Figure 5.</b>	Propagation delay at start-up . . . . .	8
<b>Figure 6.</b>	Current limitation and cut-off. . . . .	11
<b>Figure 7.</b>	Open load off-state . . . . .	13
<b>Figure 8.</b>	VCC disconnection . . . . .	14
<b>Figure 9.</b>	GND disconnection . . . . .	14
<b>Figure 10.</b>	Active clamp equivalent principle schematic . . . . .	15
<b>Figure 11.</b>	Fast demag waveforms . . . . .	15
<b>Figure 12.</b>	Typical demagnetization energy (single pulse) at $V_{CC} = 24\text{ V}$ and $T_{AMB} = 125\text{ °C}$ . . . . .	16
<b>Figure 13.</b>	PowerSSO12 package outline . . . . .	17
<b>Figure 14.</b>	PowerSSO12 recommended footprint . . . . .	18
<b>Figure 15.</b>	PowerSSO12 tape packing information [mm] . . . . .	18
<b>Figure 16.</b>	PowerSS012 reel packing information [mm] . . . . .	19

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