16-Bit, 65 MSPS, 1.8 V Analog-to-Digital Converter

Enhanced Product

AD9266-EP

FEATURES

- 1.8 V analog supply operation
- 1.8 V to 3.3 V output supply
- SNR
  - 77.6 dBFS at 9.7 MHz input
  - 76.4 dBFS at 70 MHz input
- SFDR
  - 94 dBc at 9.7 MHz input
  - 93 dBc at 70 MHz input
- Low power
  - 111 mW at 65 MSPS
- Differential input with 700 MHz bandwidth
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = −0.5/+1.0 LSB
- Interleaved data output for reduced pin-count interface
- Serial port control options
  - Offset binary, Gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1 to 8 input clock divider
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock output (DCO) with programmable clock and data alignment

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- Smart antenna systems
- Battery-powered instruments
- Handheld scope meters
- Portable medical imaging
- Ultrasound
- Radar/LIDAR
- PET/SPECT imaging

FUNCTIONAL BLOCK DIAGRAM

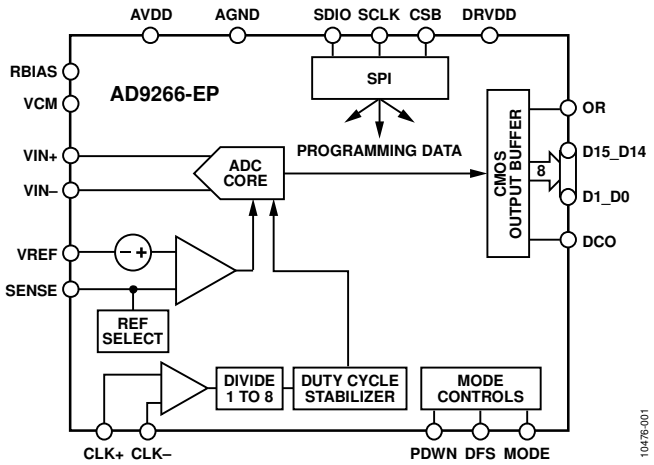

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9266-EP operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The sample-and-hold circuit maintains excellent performance at high input frequencies and is designed for low cost, low power, and ease of use.
3. A standard serial port interface supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO and data output (D15_D14 to D1_D0) timing and offset adjustments, and voltage reference modes.
4. The AD9266-EP is packaged in a 32-lead RoHS-compliant LFCSP that is pin compatible with the AD9609 10-bit ADC, the AD9629 12-bit ADC, and the AD9649 14-bit ADC, enabling a simple migration path between 10-bit and 16-bit converters sampling at 65 MSPS.

Rev. B

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GENERAL DESCRIPTION

The AD9266-EP is a monolithic, single-channel 1.8 V supply, 16-bit, 65 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 16-bit accuracy at 65 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input with a selectable internal 1-to-8 divide ratio controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The interleaved digital output data is presented in offset binary, gray code, or twos complement format. A data clock output (DCO) is provided to ensure proper latch timing with receiving logic. CMOS levels from 1.8 V through 3.3 V are supported.

The AD9266-EP is available in a 32-lead RoHS compliant LFCSP and is specified over the −55°C to +125°C temperature range.

Additional application and technical information can be found in the AD9266 data sheet.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 1.

Parameter	Temp	Min	Typ	Max	Unit
RESOLUTION	Full	16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		+0.05	±0.30	% FSR
Gain Error[1]	25°C		−1.3		% FSR
Differential Nonlinearity (DNL)[2]	Full			−0.9/+1.7	LSB
	25°C		−0.5/+1.0		LSB
Integral Nonlinearity (INL)[2]	Full			±6.5	LSB
	25°C		±2.6		LSB
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.983	0.995	1.007	V
Load Regulation Error at 1.0 mA	25°C		2		mV
INPUT-REFERRED NOISE					
VREF = 1.0 V	25°C		2.8		LSB rms
ANALOG INPUT					
Input Span, VREF = 1.0 V	25°C		2		V p-p
Input Capacitance[3]	25°C		6.5		pF
Input Common-Mode Voltage	25°C		0.9		V
Input Common-Mode Range	Full	0.5		1.3	V
REFERENCE INPUT RESISTANCE	Full		7.5		kΩ
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7		3.6	V
Supply Current					
IAVDD[2]	Full		56.3	62.2	mA
IDRVDD[2] (1.8 V)	25°C		5.2		mA
IDRVDD[2] (3.3 V)	25°C		9.3		mA
POWER CONSUMPTION					
DC Input	25°C		107		mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		111	122	mW
Sine Wave Input[2] (DRVDD = 3.3 V)	25°C		132		mW
Standby Power[4]	25°C		44		mW
Power-Down Power	25°C		0.5		mW

[1] Measured with 1.0 V external reference.
[2] Measured with a 10 MHz input frequency at rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between the differential inputs.
[4] Standby power is measured with a dc input and the CLK active.

AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		77.6		dBFS
f_{IN} = 30.5 MHz	25°C		77.4		dBFS
	Full	76.5			dBFS
f_{IN} = 70 MHz	25°C		76.4		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)					
f_{IN} = 9.7 MHz	25°C		77.4		dBFS
f_{IN} = 30.5 MHz	25°C		77.2		dBFS
	Full	76.0			dBFS
f_{IN} = 70 MHz	25°C		76.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.6		Bits
f_{IN} = 30.5 MHz	25°C		12.5		Bits
	Full	12.3			Bits
f_{IN} = 70 MHz	25°C		12.4		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 9.7 MHz	25°C		−94		dBc
f_{IN} = 30.5 MHz	25°C		−93		dBc
	Full			−80	dBc
f_{IN} = 70 MHz	25°C		−93		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		94		dBc
f_{IN} = 30.5 MHz	25°C		93		dBc
	Full	80			dBc
f_{IN} = 70 MHz	25°C		93		dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 9.7 MHz	25°C		−92		dBc
f_{IN} = 30.5 MHz	25°C		−101		dBc
	Full			−88	dBc
f_{IN} = 70 MHz	25°C		−98		dBc
TWO-TONE SFDR					
f_{IN} = 30.5 MHz (−7 dBFS), 32.5 MHz (−7 dBFS)	25°C		90		dBc
ANALOG INPUT BANDWIDTH	25°C		700		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.3		AVDD + 0.2	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
LOGIC INPUTS (SCLK/DFS, MODE, SDIO/PDWN)[1]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (CSB)[2]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		135	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage, I_{OH} = 50 µA	Full	3.29			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	3.25			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 µA	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage, I_{OH} = 50 µA	Full	1.79			V
High Level Output Voltage, I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage, I_{OL} = 1.6 mA	Full			0.2	V
Low Level Output Voltage, I_{OL} = 50 µA	Full			0.05	V

[1] Internal 30 kΩ pull-down.
[2] Internal 30 kΩ pull-up.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, DCS disabled, unless otherwise noted.

Table 4.

Parameter	Temp	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			520	MHz
Conversion Rate[1]	Full	3		65	MSPS
CLK Period—Divide by 1 Mode (t_{CLK})	Full	15.38			ns
CLK Pulse Width High (t_{CH})			7.69		ns
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1		ps rms
DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})	Full		3		ns
DCO Propagation Delay (t_{DCO})	Full		3		ns
DCO to Data Skew (t_{SKEW})	Full		0.1		ns
Pipeline Delay (Latency)	Full		8		Cycles
Wake-Up Time[2]	Full		350		µs
Standby	Full		300		ns
OUT-OF-RANGE RECOVERY TIME	Full		2		Cycles

[1] Conversion rate is the clock rate after the CLK divider.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

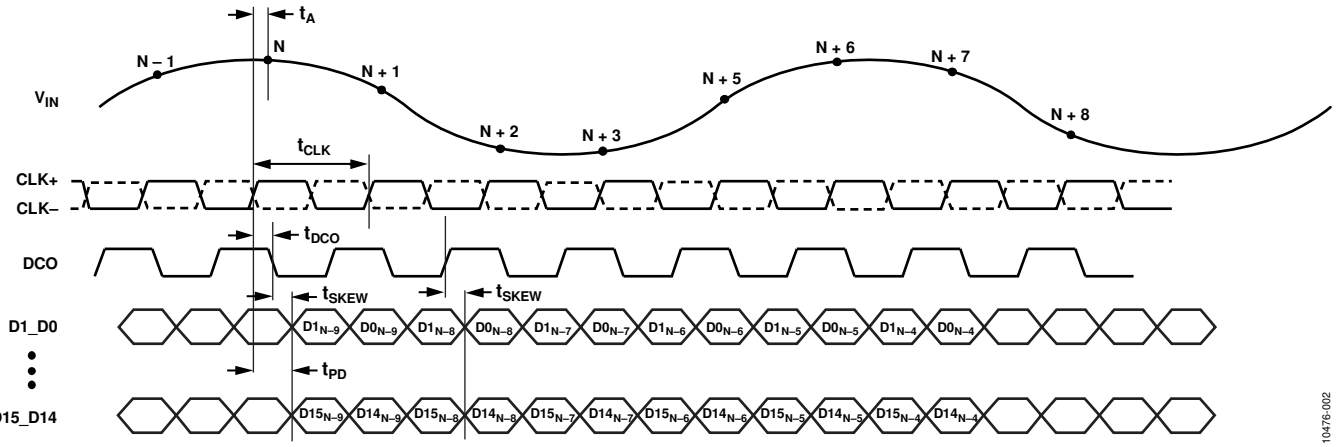


Figure 2. CMOS Output Data Timing

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +3.9 V
VIN+, VIN− to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.3 V
SDIO/PDWN to AGND	−0.3 V to DRVDD + 0.3 V
MODE/OR to AGND	−0.3 V to DRVDD + 0.3 V
D1_D0 Through D15_D14 to AGND	−0.3 V to DRVDD + 0.3 V
DCO to AGND	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	−55°C to +125°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle is the only ground connection for the chip. The exposed paddle must be soldered to the AGND plane of the circuit board. Soldering the exposed paddle to the board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
32-Lead LFCSP 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4			0.5	°C/W
	2.5	29.1			0.8	°C/W

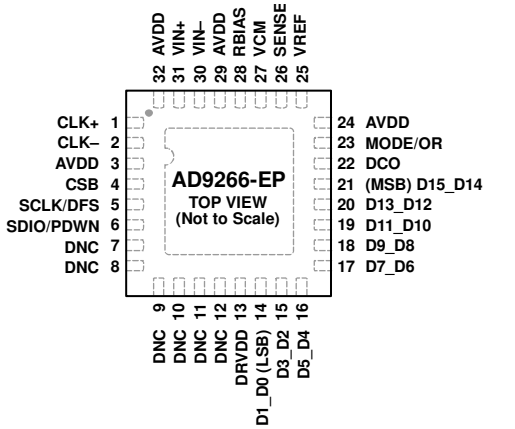
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT.
2. THE EXPOSED PADDLE IS THE ONLY GROUND CONNECTION ON THE DEVICE. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY, HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH.

10476-003

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Paddle. The exposed paddle is the only ground connection on the device. It must be soldered to the analog ground of the PCB to ensure proper functionality, heat dissipation, noise, and mechanical strength.
1, 2	CLK+, CLK–	Differential Encode Clock for PECL, LVDS, or 1.8 V CMOS Inputs.
3, 24, 29, 32	AVDD	1.8 V Supply Pin for ADC Core Domain.
4	CSB	SPI Chip Select. Active low enable, 30 kΩ internal pull-up.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). 30 kΩ internal pull-down. Data Format Select in Non SPI Mode (DFS). Static control of data output format. 30 kΩ internal pull-down. DFS high = twos complement output; DFS low = offset binary output.
6	SDIO/PDWN	SPI Data Input/Output (SDIO). Bidirectional SPI data I/O with 30 kΩ internal pull-down. Non-SPI Mode Power-Down (PDWN). Static control of chip power-down with 30 kΩ internal pull-down.
7 to 12	DNC	Do Not Connect.
13	DRVDD	1.8 V to 3.3 V Supply Pin for Output Driver Domain.
14 to 21	D1_D0 (LSB) to (MSB) D15_D14	ADC Digital Outputs.
22	DCO	Data Clock Digital Output.
23	MODE/OR	Chip Mode Select Input (MODE)/Out-of-Range Digital Output in SPI Mode (OR). Default = out-of-range (OR) digital output (SPI Register 0x2A, Bit 0 = 1). Option = chip mode select input (SPI Register 0x2A, Bit 0 = 0). Chip power-down (SPI Register 0x08, Bits[7:5] = 100b). Chip standby (SPI Register 0x08, Bits[7:5] = 101b). Normal operation, output disabled (SPI Register 0x08, Bits[7:5] = 110b). Normal operation, output enabled (SPI Register 0x08, Bits[7:5] = 111b). Out-of-range (OR) digital output only in non-SPI mode.
25	VREF	1.0 V Voltage Reference Input/Output.
26	SENSE	Reference Mode Selection.
27	VCM	Analog Output Voltage at Mid AVDD Supply. Sets common mode of the analog inputs.
28	RBIAS	Set Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
30, 31	VIN–, VIN+	ADC Analog Inputs.

OUTLINE DIMENSIONS

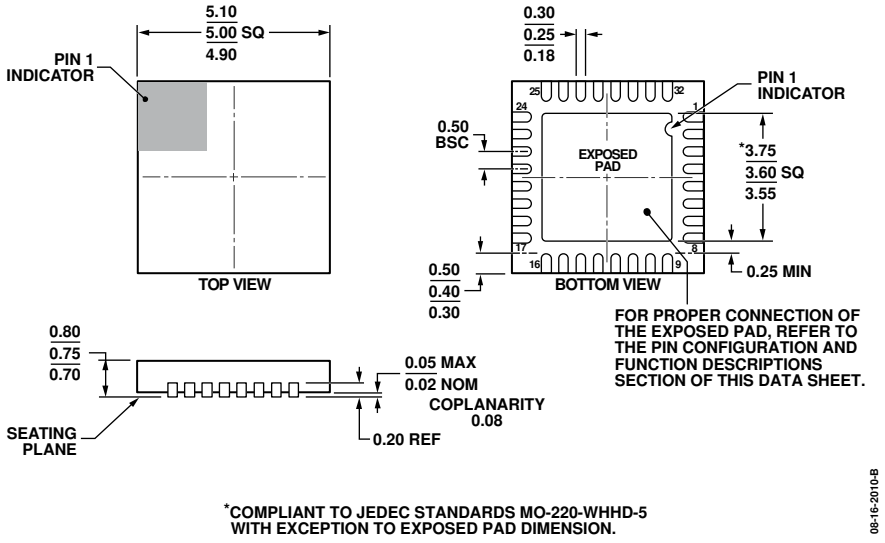


Figure 4. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad (CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9266TCPZ-65EP	−55°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
AD9266TCPZRL7-65EP	−55°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12

[1] Z = RoHS Compliant Part.

NOTES

D10476-0-3/16(B)